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<td>SmartFusion2 Security Evaluation Kit Jumper Settings</td>
<td>13</td>
</tr>
</tbody>
</table>
1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 6.0
This document is updated for Libero SoC v11.8 SP1 release changes.

1.2 Revision 5.0
Revision 5.0 was published in April 2016. Updated the document for Libero v11.7 software release (SAR 78195).

1.3 Revision 4.0
Revision 4.0 was published in November 2015. Changed AXI: MDDR ratio as 1:1 and updated Figure 3 on page 5, Figure 4 on page 6, Figure 5 on page 7, and Figure 6 on page 8 (SAR 73230).

1.4 Revision 3.0
Revision 3.0 was published in October 2015. Updated the document for Libero v11.6 software release (SAR 71692).

1.5 Revision 2.0
Revision 2.0 was published in February 2015. Updated the document for Libero v11.5 software release (SAR 64895).

1.6 Revision 1.0
Revision 1.0 was the first publication of this document in August 2014.
2 Interfacing SmartFusion2 SoC FPGA with External LPDDR Memory through MDDR Controller

This demo shows the microcontroller subsystem (MSS) double-data rate (DDR) controller accessing the external DDR SDRAM memories in the SmartFusion®2 devices. The demo has two parts:

- Demo using simulation
- Demo using the SmartFusion2 Security Evaluation Kit

In the demo design, the advanced eXtensible interface (AXI) Master in the FPGA fabric accesses the low power DDR (LPDDR) memory present in the SmartFusion2 Security Evaluation Kit board using the microcontroller subsystem DDR (MDDR) controller. A utility, SF2_MDDR_Demo is provided along with the demo deliverables. Using the utility, you can drive the AXI Master logic. The AXI Master converts the commands from the utility to AXI transactions for the MDDR controller to perform the read/write operations on the LPDDR memory.

2.1 Design Requirements

The following table lists the hardware and software design requirements.

<table>
<thead>
<tr>
<th>Design Requirements</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Hardware Requirements</strong></td>
<td></td>
</tr>
<tr>
<td>SmartFusion2 Security Evaluation Kit:</td>
<td>Rev E or later</td>
</tr>
<tr>
<td>• FlashPro4 programmer</td>
<td></td>
</tr>
<tr>
<td>• 12 V adapter</td>
<td></td>
</tr>
<tr>
<td>• USB A to Mini-B cable</td>
<td></td>
</tr>
<tr>
<td>Host PC or Laptop</td>
<td>Any 64-bit Windows Operating System</td>
</tr>
<tr>
<td><strong>Software Requirements</strong></td>
<td></td>
</tr>
<tr>
<td>Libero® SoC</td>
<td>v11.8 SP1</td>
</tr>
<tr>
<td>FlashPro programming software</td>
<td>v11.8 SP1</td>
</tr>
<tr>
<td>SoftConsole</td>
<td>v4.0</td>
</tr>
<tr>
<td>Microsoft .NET Framework 4</td>
<td></td>
</tr>
<tr>
<td>Host PC Drivers</td>
<td>USB to UART drivers</td>
</tr>
</tbody>
</table>
2.2 Demo Design

The demo design files are available for download from the following path in the Microsemi website:
http://soc.microsemi.com/download/rsc/?f=m2s_dg0568_liberov11p8_sp1_df

Design files include:

- Demo_utility
- Libero_project
  - SF2_MDDR_Demo
- Programming_file
- Source_files
- readme.txt

The following figure shows the top-level structure of the design files. For further details, see the readme.txt file.

**Figure 1 • Demo Design Files Top-Level Structure**

In the demo design, the AXI Master implemented in the FPGA Fabric accesses the LPDDR memory present in the SmartFusion2 Security Evaluation Kit board using the MDDR controller. The AXI Master logic communicates to the MDDR controller through Core AXI interface and the DDR_FIC interface. The read/write operations initiated by the SF2_MDDR_Demo utility are sent to the UART_IF block using the UART protocol. The AXI Master receives the address and the data from the UART_IF block. During a write operation, the UART_IF block sends the address and data to the AXI Master logic.

During a read operation, the UART_IF block sends the address to the AXI Master and stores the read data in two port static random-access memory (TPSRAM). When the read operation is complete, the read data is sent to the host PC through UART.
The following figure shows the top-level view of demo design.

**Figure 2 • SmartFusion2 MDDR Demo Block Diagram**

In this demo design, different blocks are configured as shown below:

- MDDR controller is configured for LPDDR memory available in the SmartFusion2 Security Evaluation Kit board. The LPDDR memory is a Micron DRAM (Part Number: MT46H32M16LF)
- DDR_FIC is configured for AXI bus interface.
- Both AXI clock and LPDDR clock are configured for 160 MHz.
- TPSRAM IP has the following configuration:
  - Write port depth: 256
  - Write port width: 64
  - Read port depth: 2048
  - Read port width: 8

See Appendix: Configuring MDDR Controller, page 23 for information on how to configure the DDR controller.

### 2.3 Demo Design Features

The SmartFusion2 MDDR demo design has the following features:

- Single AXI read or write transactions
- 16-beat burst AXI read or write transactions
- LPDDR memory model simulation using SmartDesign testbench
- Design validation using the SmartFusion2 Security Evaluation Kit board that has the LPDDR memory
- Initiation of the read or write transactions using SF2_MDDR_Demo utility
2.3.1 Demo Design Description

The demo design consists of the following SmartDesign components:

- **MDDR_Demo_top_0**: This SmartDesign handles the data transactions between the MDDR controller and LPDDR SDRAM.
- **UART_IF_0**: This SmartDesign handles the communication between the host PC and the SmartFusion2 Security Evaluation Kit board.

The following figure shows the **MDDR_Demo_top_0** and **UART_IF_0** connections.

**Figure 3**  SF2_MDDR_Demo SmartDesign

2.3.1.1 MDDR_Demo_top_0

This consists of the MDDR_Demo_0 subsystem generated using the System Builder and the AXI_IF_0 master logic. The AXI_IF_0 master logic is an RTL code that implements the AXI read and write transactions. It receives the read or write operations, burst length (RLEN and WLEN), address and data as inputs. Based on inputs received, it communicates with the LPDDR memory through the MDDR controller.
Interfacing SmartFusion2 SoC FPGA with External LPDDR Memory through MDDR Controller

The following figure shows the MDDR_Demo_top_0 SmartDesign component.

**Figure 4 • MDDR_Demo_top_0 SmartDesign Component**

2.3.1.2 UART_IF_0

The UART_IF_0 SmartDesign component handles the communication between the host PC demo utility and the AXI Master logic. The MMUART_1 block present in the MSS receives the UART signals from the host PC user interface, the ARM Cortex-M3 processor sends this user data to the DATAHANDLE_FSM block present in the FPGA fabric using the FIC_0 advanced peripheral bus (APB) slave interface. DATAHANDLE_FSM is an APB slave wrapper, which sends the received data to the UART_IF_FSM_0 block.

For a single write operation, the UART_IF_FSM_0 wrapper receives the address and data from the demo utility. For a burst write operation, the address and data are received from the demo utility and the subsequent incremental data are provided by the UART_IF_FSM_0 wrapper.

For a burst read operation, UART_IF_FSM_0 collects the address from the demo utility and sends that to the AXI_IF_0 master logic. It then receives the read data from the AXI_IF_0 master logic and stores it in the TPSRAM_0. After completion of the read burst transactions, the Cortex-M3 processor reads the TPSRAM_0 buffer through DATAHANDLE_FSM (APB wrapper) block. The received data is sent to the host PC using the MMUART_1 block.
The following figure shows the UART_IF_0 SmartDesign component.

**Figure 5 • UART_IF_0 SmartDesign Component**

### 2.4 Running the Demo Using Simulation

The demo design can be simulated using SmartDesign testbench and the LPDDR memory model (MT46H32M16LF with 512 Mb density).

The simulation is set to run the following:

- Single AXI write and read operation
- 16-beat AXI burst write and read operation

The following figure shows the AXI_LPDDR_Simulation SmartDesign testbench. The AXI_testbench provides the read or write operations, burst length, address, and data to the MDDR_Demo_top_0 SmartDesign component.
To run simulation, ensure that the following files are present in the Libero SoC project:

- dram.v
- dram_parameters.vh
- AXI_testbench.v

The default location of the files is:
<Download folder>\SF2_MDDR_Demo_DF\Libero_project\SF2_MDDR_Demo\stimulus
2.4.1 Simulation

Simulation setup configuration can be set properly using the following steps:

1. Launch the Libero SoC software.
2. Browse the SF2addy_MDDR_Demo project provided in the design file.
3. Go to Project > Project Settings > Simulation Options.
4. Ensure that the DO File tab has the configuration, as shown in the following figure.

**Figure 7 • DO File Settings**

![DO File Settings](image)

5. Ensure that the Waveforms tab has the configuration, as shown in the following figure.

**Figure 8 • Waveforms Settings**

![Waveforms Settings](image)
6. Go to Design Flow tab.
7. Right-click Simulate under Verify Pre-Synthesized Design and then select, Organize Input Files > Organize Stimulus Files, as shown in the following figure.

**Figure 9 • Invoking Organize Stimulus Files Window**

8. Ensure that the Organize Stimulus files window has the configuration, as shown in the following figure.

**Figure 10 • Organize Stimulus Files Window**
2.4.2 Running the Simulation

The following steps describe how to run the simulation:

1. Right-click **Simulate** under **Verify Pre-Synthesized Design**.
2. Click **Open Interactively**.
3. Simulation requires 900 µs to complete as mentioned in the 3rd point under **Simulation**, page 9.

The following figure shows the transcript window of the simulation.

**Figure 11 • Simulation Completed**

![Simulation Transcript](image-url)
The following figure shows the single AXI write and AXI read operation.

*Figure 12 • Single Write and Read Operation*

The following figure shows the 16-beat AXI burst write and read operation.

*Figure 13 • 16-Beat AXI Burst Write and Read*
2.5 Setting Up the Hardware Demo

The following steps describe how to setup the hardware demo:

1. Connect the jumpers on the SmartFusion2 Security Evaluation Kit, as listed in the following table.

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Pin (From)</th>
<th>Pin (To)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>J22</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J23</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J24</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J8</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J3</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
</tbody>
</table>

**CAUTION:** Ensure that the power supply switch, SW7, is switched off while connecting the jumpers.

2. Connect the Power supply to the J6 connector, switch on the power supply switch, SW7.
3. Connect the FlashPro4 programmer to the J5 connector of the SmartFusion2 Security Evaluation Kit.
4. Connect the host PC USB port to the SmartFusion2 Security Evaluation Kit board’s J18 USB connector using the USB mini-B cable.

The following figure shows the board setup for running the SmartFusion2 MDDR demo on the SmartFusion2 Security Evaluation Kit.

![SmartFusion2 Security Evaluation Kit](image)

**Figure 14 • SmartFusion2 Security Evaluation Kit**
5. Ensure that the USB to UART bridge drivers are automatically detected. This can be verified in the Device Manager of the host PC. The FTDI USB to UART converter enumerates four COM ports. For USB 2.0, note down the USB Serial Converter D COM port number to use it in the GUI. The following figure shows the USB 2.0 Serial port properties, and COM7 is connected to USB Serial Converter D. See Appendix: Finding Correct COM Port Number when Using the USB 3.0, page 27 for finding the correct COM port in USB 3.0.

Figure 15 • USB Serial 2.0 Port Properties

6. If the USB to UART bridge drivers are not installed, download and install the drivers from www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip.
2.6 Programming the Demo Design

The following steps describe how to program the demo design:

1. Download the demo design from the following link:
   http://soc.microsemi.com/download/rsc/?f=m2s_dg0568_liberov11p8_sp1_df
2. Switch **ON** the power supply switch **SW7**.
3. Launch the FlashPro software.
4. Click **New Project**.
5. In the **New Project** window, type the project name as **SF2_MDDR_Demo**.
6. Click **Browse** and navigate to the location where you want to save the project.
7. Select **Single device** as the **Programming mode**.
8. Click **OK** to save the project.

*Figure 16 • FlashPro New Project*
2.6.1 Setting Up the Device

The following steps describe how to configure the device:

1. Click Configure Device on the FlashPro GUI.
2. Click Browse and navigate to the location where the SF2_MDDR_Demo.stp file is located and select the file. The default location is:
   <download_folder>\SF2_MDDR_Demo_DF\Programming_file\.
3. Click Open. The required programming file is selected and is ready to be programmed in the device.

Figure 17 • FlashPro Project Configuration
2.6.2 Programming the Device

Click **PROGRAM** to start programming the device. Wait until Programmer Status is changed to **RUN PASSED**.

*Figure 18* • FlashPro Program Passed
2.6.3 Running the Hardware Demo

The SmartFusion2 MDDR demo comes with utility, SF2_MDDR_Demo, that runs on the host PC to communicate with the SmartFusion2 Security Evaluation Kit board. The UART protocol is used as the underlying communication protocol between the host PC and the SmartFusion2 Security Evaluation Kit board.

The following figure shows the initial screen of the SF2_MDDR_Demo utility.

Figure 19 • SF2_MDDR_Demo Utility

The SF2_MDDR_Demo utility has the following sections:

- **Serial Port Configuration**: Displays the serial port. Baud rate is fixed at 115200.
- **Data Transfer Type**: Single or Burst.
- **LPDDR SDRAM**: Provides Address and Data.
- **LPDDR Burst Read**: Displays the Burst Read Values for the corresponding address.
- **C**: Clears the existing data.
2.6.4 Steps to Run GUI

The following steps describe how to run the GUI:

1. Launch the utility. The default location is:
   `<download_folder>\SF2_MDDR_Demo_DF\Demo_Utility\SF2_MDDR_Demo.exe`.
2. Select the appropriate COM port from drop down menu. In this case, it is COM 7.
3. Click Connect. The connection status along with the COM Port and Baud rate is shown in the left bottom corner of the screen. The following figure shows the connection status of the utility.

**Figure 20 • SF2_MDDR_Demo – Connection Status**

![SF2_MDDR_Demo – Connection Status](image)

2.6.5 Performing a Single Data Transfer

For a single write or read operation, the AXI Master logic is configured to transfer a burst length of 1 (that is, 8 bytes). For a write operation, the utility sends a 32-bit address and 64-bit (8 bytes) data. The data is then written to the LPDDR SDRAM. For a read operation, the utility sends a 32-bit address and receives 64-bit data from LPDDR and is displayed in the utility.

The following steps describe how to perform a single data transfer:

1. Select the **Data Transfer Type as Single (8 bytes)**.
2. A 64-bit aligned address is required in the address field. Enter a 32-bit HEX Address in the range `0x00000000 - 0x03FFFFF8`. When a non 64-bit aligned address is provided, the GUI converts it to 64-bit aligned address and performs the write or read. See Appendix: Performing Write/Read Operation when Non 64-Bit Aligned Address is Provided, page 29 to perform write or read when non 64-bit aligned address is provided.
3. In the **Data** field, enter a 64-bit data in HEX format.
4. Click **Write**. The entered data is written to the LPDDR memory.
The following figure shows the **Address** and **Data** values entered for a Single Write operation.

**Figure 21 • Single Write Operation**

5. To verify the write operation, perform a read operation to the same address where the data was written.

6. Press **C** to clear the data present in the **Data** field. The following figure highlights the Clear button, C.

**Figure 22 • Clear Data Field**

7. Click **Read** to read the data from the LPDDR SDRAM.
The following figure shows the data read from the LPDDR SDRAM.

**Figure 23 • Single Read Operation**

8. Compare the read and write data. The write and read data being same establishes that the write and read operations to the LPDDR SDRAM were successful.

### 2.6.6 Performing Burst Data Transfer

For a burst write or read operation, the AXI Master logic is configured to transfer a burst length of 16 (that is, 128 bytes). In this demo, 16 transfers of 16-beat burst operations is implemented, that is, 16 (transfers) x 16-beat burst data = 2048 bytes data). For a write operation, the utility sends a 32-bit initial address and 64-bit (8 bytes) initial data. After the initial write operation, incremental data is written. For a read operation, the utility sends a 32-bit address and receives 2048 bytes of data from the LPDDR SDRAM and the data is displayed in the utility.

The following steps describe how to perform a burst data transfer:

1. Select the **Data Transfer Type as Burst (2048 bytes)**.
2. A 64-bit aligned address is required in the address field. Enter a 32-bit HEX Address in the range 0x00000000 - 0x03FFF7F8. When a non 64-bit aligned address is provided, the GUI converts it into 64-bit aligned address and performs the write or read operation. See Appendix: Performing Write/Read Operation when Non 64-Bit Aligned Address is Provided, page 29 to perform write or read when non 64-bit aligned address is provided.
3. In the **Data** field, enter a 64-bit data in HEX format.
4. Click **Write**. The entered data is written to the Address location specified in the Address field and then the data is incremented by 1 and written to the next address location. This is repeated 256 times to write all the 2048 bytes of data.
The following figure shows the **Address** and **Data** values entered for a Burst Write operation.

**Figure 24 • Burst Write Operation**

5. To verify the write operation, perform a read operation to the same address where the data was written.
6. Click **Read**. All the 2048 bytes of data that was written to the LPDDR was read and the read data was displayed in the **LPDDR Burst Read** panel. The following figure shows the burst read data.

**Figure 25 • Burst Read Operation**

7. Click **Exit** to exit the utility.

## 2.7 Conclusion

This demo shows how to perform Read or Write operations to LPDDR SDRAM using the SmartFusion2 MDDR controller. Options are provided to simulate the design using a SmartDesign testbench and validate the design on the SmartFusion2 Security Evaluation Kit using a GUI interface.
This section describes how to configure the MDDR controller registers using Libero SoC. The configuration options for MDDR are available at the MDDR tab of the Memories tab in System Builder.

The SmartFusion2 Security Evaluation Kit has the LPDDR memory from Micron. All values provided here are from the Micron datasheet; part number, MT46H32M16LF.

**Note:** The [Automotive Mobile Low-Power DDR SDRAM Datasheet](https://www.micron.com) is available for download from Micron website.

The following figure shows the MDDR tab.

![System Builder - Memories - MDDR Tab](image)

### 3.1 MDDR Configuration Tab

When using an external memory, the memory controller must wait for the memory to initialize (settling time) before accessing it. The SmartFusion2 Security Evaluation Kit uses the LPDDR memory. Therefore, the DDR controller has to wait at least 200 µs. Provide 200 as the value for the field, DDR memory settling time (us).

**Note:** All the values provided here are from the Micron datasheet. The parameters can be configured according to the user requirements.
3.1.1 General

This section shows the configurations of the General tab.

- **Memory Type**: LPDDR
- **Data Width**: 16
- **Address Width (bits)**
  - **Row**: 16
  - **Bank**: 2
  - **Column**: 10

The following figure shows the General tab after configuration parameters are set.

*Figure 27* • System Builder MDDR Configuration – General Tab

3.1.2 Memory Initialization

This section shows the configurations of the Memory Initialization tab.

- **Burst length**: 8
- **Burst Order**: Sequential
- **Timing Mode**: 1T
- **CAS Latency**: 3
- **Self Refresh Enabled**: NO
- **Auto Refresh Burst Count**: 8
- **Power Down Enabled**: YES
- **Stop the clock**: NO
- **Deep Power Down enabled**: NO
- **No Activity clocks for Entry**: 320
The following figure shows the Memory Initialization tab after configuration parameters are set.

*Figure 28 • System Builder MDDR Configuration – Memory Initialization Tab*

![Figure 28](image)

### Memory Timing

This section shows the configurations of the Memory Timing tab.

- **Time To Hold Reset Before INIT** – 0
- **MRD**: 4
- **RAS (Min)**: 8
- **RAS (Max)**: 8192
- **RCD**: 6
- **RP**: 7
- **REFI**: 3104
- **RC**: 12
- **XP**: 3
- **CKE**: 3
- **RFC**: 79
- **FAW**: 0
The following figure shows the **Memory Timing** tab after configuration parameters are set.

*Figure 29 • System Builder MDDR Configuration – Memory Timing Tab*
FTDI USB to UART converter enumerates the four COM ports. In USB 3.0, the four available COM ports are in Location 0. The following figure shows the USB 3.0 Serial port properties.

Figure 30 • USB 3.0 Serial Port Properties

To find out the correct COM port, program the SmartFusion2 Security Evaluation Kit board with provided programming file. Connect each available COM port and click **Write**. If wrong COM port is selected, the GUI displays the read error. Try with all four available COM ports until this message disappears.
The following figure shows the read error message.

**Figure 31 • Read Error**
Appendix: Performing Write/Read Operation when Non 64-Bit Aligned Address is Provided

When a non 64-bit aligned address is provided in the GUI, the GUI converts it into the 64-bit aligned address (0×0, 0×8, 0×10, 0×18, 0×20, 0×28, 0×30, 0×38…) and performs the write/read operation.

1. Enter the non 64-bit aligned 32-bit address in HEX format.
2. Enter the 64-bit data in HEX format.

The following figure shows the non 64-bit aligned address entered in the GUI.

Figure 32 • Non 64-Bit Aligned Address

3. Click **Write** to perform write operation. GUI converts the address into 64-bit aligned address and performs the write operation.
The following figure shows the GUI pop-up information message and converted 64-bit aligned address.

Figure 33 • Converted 64-Bit Aligned Address