The MAX24287 is a flexible, low-cost Ethernet interface conversion IC. The parallel interface can be configured for GMII, RGMII, TBI, RTBI, or 10/100 MII, while the serial interface can be configured for 1.25Gbps SGMII or 1000BASE-X operation. In SGMII mode, the device interfaces directly to Ethernet switch ICs, ASIC MACs, and 1000BASE-T electrical SFP modules. In 1000BASE-X mode, the device interfaces directly to 1Gbps 1000BASE-X SFP optical modules. The MAX24287 performs automatic translation of link speed and duplex autonegotiation between parallel MII MDIO and the serial interface. Microprocessor interaction is optional for device operation. Hardware-configured modes support SGMII master and 1000BASE-X autonegotiation without software involvement.

This device is ideal for interfacing single-channel GMII/MII devices such as microprocessors, FPGAs, network processors, Ethernet-over-SONET or -PDH mappers, and TDM-over-packet circuit emulation devices. The device also provides a convenient solution to interface such devices with electrical or optical Ethernet SFP modules.

### Applications
Any System with a Need to Interface a Component with a Parallel MII Interface (GMII, RGMII, TBI RTBI, 10/100 MII) to a Component with an SGMII or 1000BASE-X Interface
Switches and Routers
Telecom Equipment

### Ordering Information

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX24287ETK+</td>
<td>-40°C to +85°C</td>
<td>68 TQFN-EP*</td>
</tr>
</tbody>
</table>

+ Denotes a lead(Pb)-free/RoHS-compliant package.
*EP = Exposed pad.

### Highlighted Features
- Bidirectional Wire-Speed Ethernet Interface Conversion
- Can Interface Directly to SFP Modules and SGMII PHY and Switch ICs
- Serial Interface Configurable as 1000BASE-X or SGMII Revision 1.8 (4-, 6-, or 8-Pin)
- Parallel Interface Configurable as GMII, RGMII, TBI, RTBI, or 10/100 MII
- Serial Interface Has Clock and Data Recovery Block (CDR) and Does Not Require a Clock Input
- Translates Link Speed and Duplex Mode Negotiation Between MDIO and SGMII PCS
- Supports 10/100 MII or RGMII Operation with SGMII Running at the Same Rate
- Configurable for 10/100 MII DTE or DCE Modes (i.e., Connects to PHY or MAC)
- Can Also Be Configured as General-Purpose 1:10 SerDes with Optional Comma Alignment
- Supports Synchronous Ethernet by Providing a 25MHz or 125MHz Recovered Clock and Accepting a Transmit Clock
- Can Provide a 125MHz Clock for the MAC to Use as GTXCLK
- Accepts 10MHz, 12.8MHz, 25MHz or 125MHz Reference Clock
- Can Be Pin-Configured at Reset for Many Common Usage Scenarios
- Optional Software Control Through MDIO Interface
- GPIO Pins Can Be Configured as Clocks, Status Signals and Interrupt Outputs
- 1.2V Operation with 3.3V I/O
- Small, 8mm x 8mm, 68-Pin TQFN Package
1. Application Examples

a) Copper Media

b) Connect Parallel MII Component to SGMII Component

c1) Long PCB Trace Card-to-Card

c2)

d) Fiber Module
2. Block Diagram

Figure 2-1. Block Diagram

3. Detailed Features

General Features
- High-speed MDIO interface (12.5MHz slave only) with optional preamble suppression
- Can be pin-configured at reset for many common usage scenarios
- Operates from a 10, 12.8, 20, 25, or 125MHz reference clock
- Optional 125MHz output clock for MAC to use as GTXCLK

Parallel-Serial MII Conversion Features
- Bidirectional wire-speed interface conversion
- Serial Interface: 1000BASE-X or SGMII revision 1.8 (4-, 6-, or 8-Pin)
- Parallel Interface: GMII, RGMII (10, 100 and 1000Mbps), TBI, RTBI or 10/100 MII (DTE or DCE)
- 8-pin source-clocked SGMII mode
- 4-pin 1000BASE-X SerDes mode to interface with optical modules
- Connects processors with parallel MII interfaces to 1000BASE-X SFP optical modules
- Connects processors with parallel MII interfaces to PHY or switch ICs with SGMII interfaces
- Interface conversion is transparent to MAC layer and higher layers
- Translates link speed and duplex mode between GMII/MII MDIO and SGMII PCS
- Configurable for 10/100 MII DTE or DCE Modes (i.e., connects to PHY or MAC)

Synchronous Ethernet Features
- Receive path bit clock can be output on a GPIO pin to line-time the system from the Ethernet port
- Transmit path can be frequency-locked to a system clock signal connected to the REFCLK pin
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