Microsemi
POWER PRODUCTS GROUP

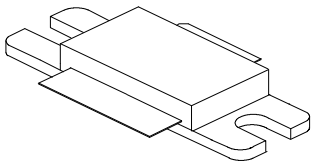
1011LD110A

110 Watts, 32 Volts
Pulsed Avionics 1030 to 1090 MHz
LDMOS FET

GENERAL DESCRIPTION

The 1011LD110A is a COMMON SOURCE N-Channel enhancement mode lateral MOSFET capable of providing 110W_{pk} of RF power from 1030MHz to 1090 MHz. The device is nitride passivated and utilizes gold metallization to ensure highest MTTF. The transistor includes input and output prematch for broadband capability. Low thermal resistance package reduces junction temperature, extends life. Integrated ESD protection makes the device robust.

CASE OUTLINE
55QZ
(Common Source)



ABSOLUTE MAXIMUM RATINGS

Voltage and Current

Drain-Source (V_{DSS})	+65V
Gate-Source (V_{GS}, V_{DS}=0)	+20V

Temperatures

Storage Temperature	-65 to +150°C
Operating Case Temperature[1]	+100°C

ELECTRICAL CHARACTERISTICS @ 25°C

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BV_{DSS}	Drain-Source Breakdown	V_{GS} = 0V, I_D = 2mA	65			V
I_{DSSF}	Drain-Source Leakage Current	V_{DS} = 32V, V_{GS} = 0V			5	µA
I_{GSSF}	Gate-Source Leakage Current	V_{GS} = 10V, V_{DS} = 0V			2	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = 10V, I_D = 3mA	2		4	V
$V_{DS(ON)}$	Drain-Source On Voltage	V_{GS} = 10V, I_D = 1A			0.25	V
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 1A		2.2		S
θ_{JC}[1]	Thermal Resistance				0.1	°C/W

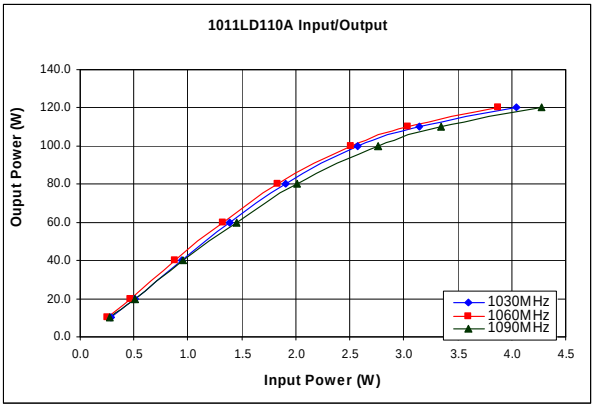
FUNCTIONAL CHARACTERISTICS @ 25°C, Vds = 32V, I_{DQ} = 250mA

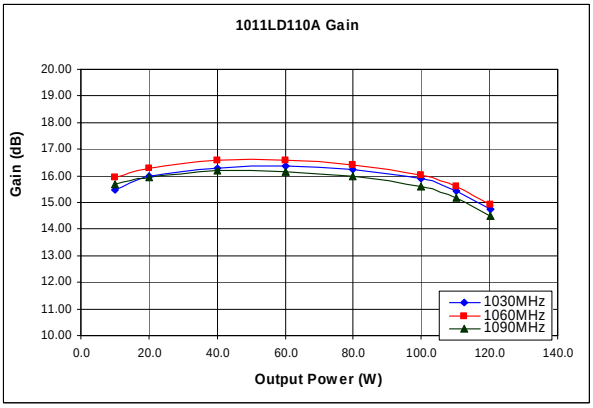
G_{PS}	Common Source Power Gain	Pulse width = 32µs, LTDC=2%	14	15		dB
Pd	Pulse Droop	F=1030/1090 MHz, P_{out} = 110W			0.5	dB
P_{1dB}	Output Power at 1dB Gain Compression	Pulse width = 32µs, LTDC=2%, F=1030/1090 MHz		110		W
η_D	Drain Efficiency	F = 1030 MHz, P_{out} = 110W	45	50		%
ψ	Load Mismatch	F = 1090 MHz, P_{out} = 110W			5:1	

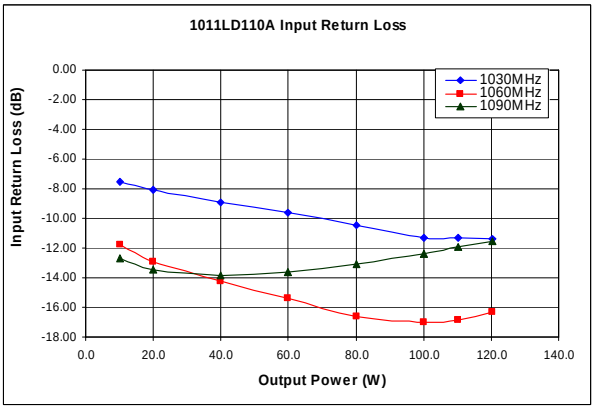
NOTES: 1. At rated output power and pulse conditions
2. Pulse Format 1: 32µs, 2% Long Term Duty Factor
3. Pulsed Bias: $I_{DQ-PULSED}$ = 6.5mA (@ 42us ON, 1.6msec)

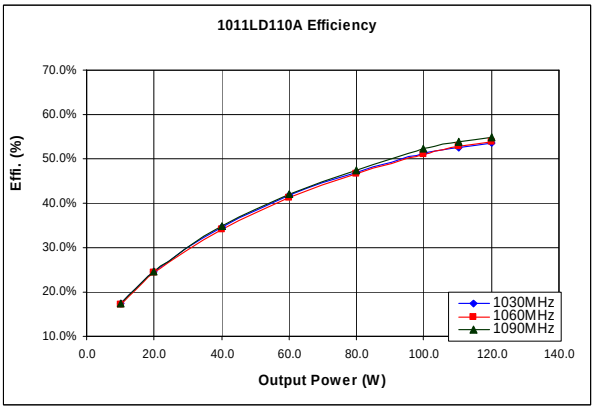
Rev. 0 – Apr. 2007

Typical Performance (1030MHz ~ 1090MHz)

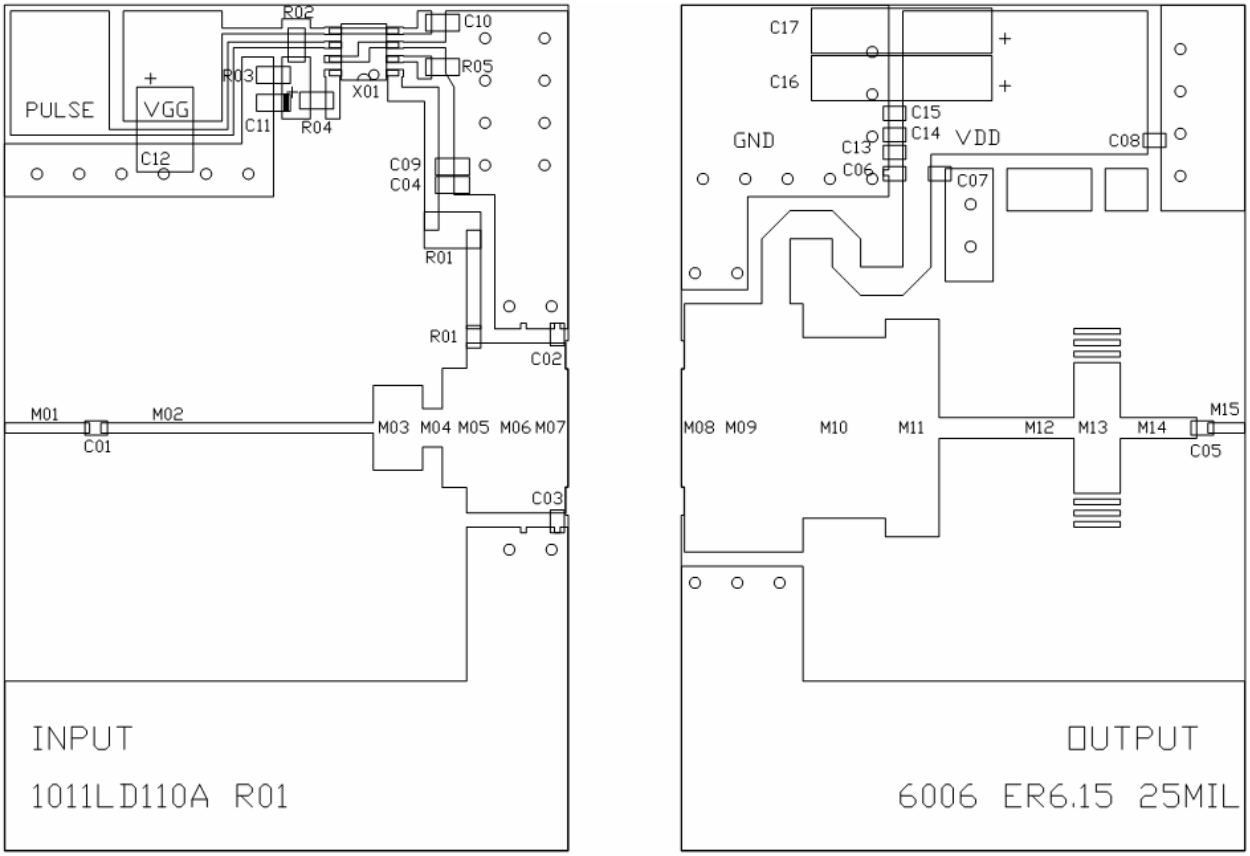








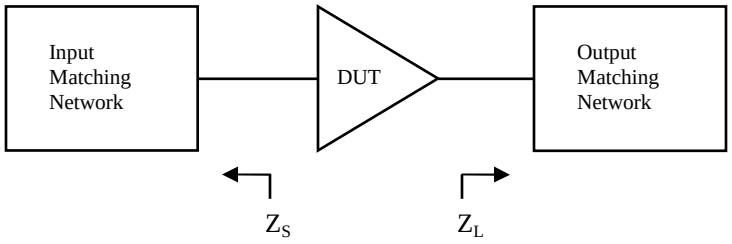
1011LD110A Test Circuit Layout



1011LD110A Test Circuit Component Designations and Values

Part	Description	Part	Description
C01, C04, C05, C06	43pF Chip Capacitor (ATC 100A)	C10, C14, C15	0.033uF Chip Capacitor
C07, C08	100pF Chip Capacitor (ATC 100A)	C11	1uF 16V Tantalum Capacitor
C02, C03	5.6pF Chip Capacitor (ATC 100A)	C12	47uF 63V Electrolytic Capacitor
C17	1000uF, 63V Electrolytic Capacitor	C16	470uF, 63V Electrolytic Capacitor
C09, C13	1000pF Chip Capacitor	L01	6 Turns, 24 AWG, IDIA 0.092″
R01, R04	15Ω, 1/4W Chip Resistor	R02, R03	200Ω, 1/4W Chip Resistor
R05	82.5Ω, 1/4W Chip Resistor	X01	ADG419, Analog Device
M01	36 x 300 mils (W x L)	M02	36 x 966 mils (W x L)
M03	300 x 175 mils (W x L)	M04	136 x 70 mils (W x L)
M05	422 x 86 mils (W x L)	M06	602 x 351 mils (W x L)
M07	420 x 8 mils (W x L)	M08	420 x 10 mils (W x L)
M09	881 x 420 mils (W x L)	M10	641 x 292 mils (W x L)
M11	771 x 190 mils (W x L)	M12	75 x 479 mils (W x L)
M13	464 x 164 mils (W x L)	M14	75 x 271 mils (W x L)
M15	36 x 130 mils (W x L)	PCB	Rogers RT6006, ε_r=6.15, 25mils, 1oz

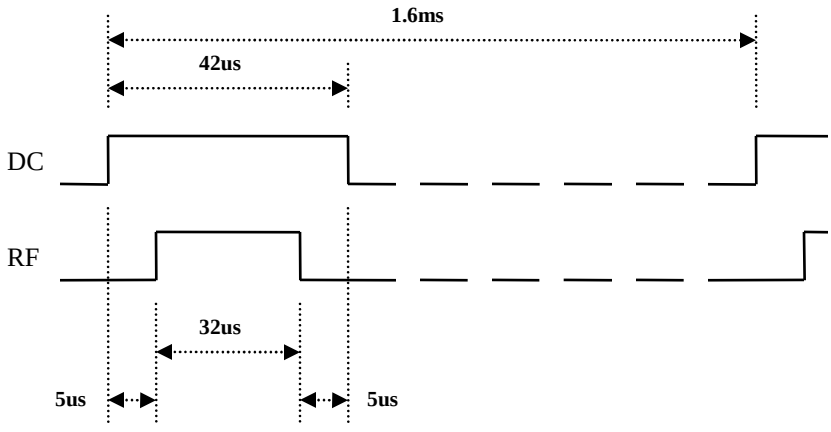
Typical Impedance Values



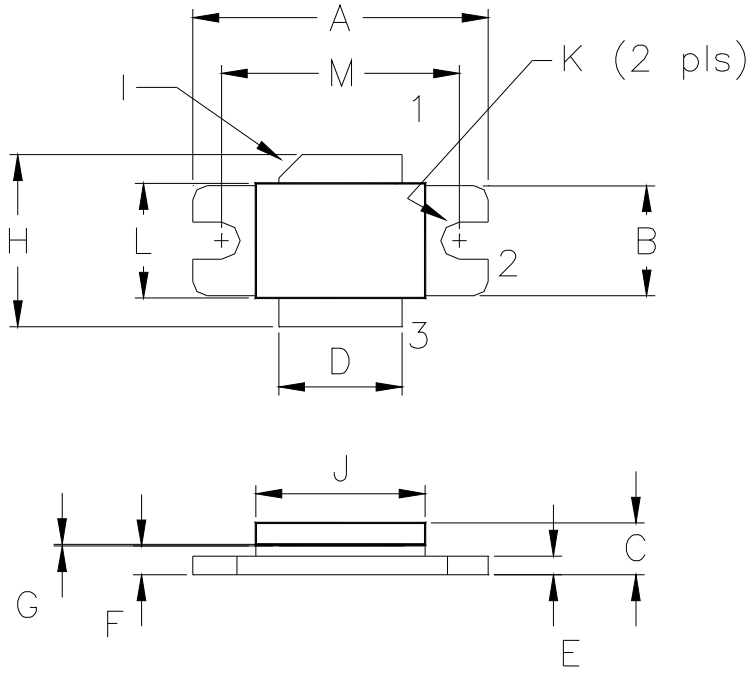
Frequency (MHz)	Z_S (Ω)	Z_L (Ω)
1030	**0.73 - j2.71**	**3.11 - j1.66**
1060	**0.70 - j2.49**	**2.87 - j1.79**
1090	**0.67 - j2.28**	**2.56 - j1.82**

* V_{DS} = 32V, I_{DQ} = 250mA, P_{out} = 110W
* Pulse Format: 32µs, 2% Long Term Duty Factor

Timing Diagram for Pulsed Bias

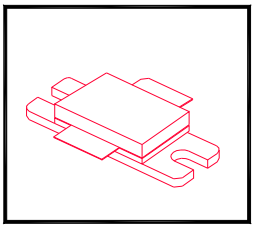


REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



DIM	MILLIMETER	±TOL	INCHES	±TOL
A	26.20	.25	1.03	.010
B	9.58	.25	.385	.010
C	4.57	.19	.180	.007
D	10.16	.13	.430	.005
E	1.65	.13	.065	.005
F	2.54	.13	.100	.005
G	0.13	.03	.005	.001
H	15.24	.76	.600	.030
I	45°	5°	45°	5°
J	15.00	.25	.590	.030
K	3.30 DIA	.13	.130 DIA	.005
L	10.16	.13	.400	.005
M	21.08	MAX	.830	MAX

PIN 1 = DRAIN
2 = SOURCE
3 = GATE



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CAGE	DWG NO.	REV
0PJR2	55QZ	A
	SCALE 2:1	SHEET