Advanced IGBT Driver  
APPLICATION MANUAL

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Introduction

To simplify the design of high power, high performance applications, MICROSEMI introduced a new advanced Dual IGBT Driver. Dedicated to drive high Power IGBT modules (up to 300A, 1200V, 50 kHz) in phase leg operation (as shown on Fig. 1), this circuit provides multiple functions to optimize IGBT performance. This application note describes some techniques to:

- Verify the driver capacity by the total gate charge calculation.
- Optimize turn-on and turn-off operation for switching losses reduction by selecting the appropriate gate resistances ($R_{G(on)}$, $R_{G(off)}$).
- Prevent cross conduction by the input signal dead time calculation.
- Eliminate gate rigging in case of paralleled IGBT modules operation.
- Understand the short circuit protection operation including fault output and reset in case of short circuit detection.
- Explain mounting procedure.

**Figure 1 Typical Phase Leg Operation**

**Description:**

Among other functions, this high speed circuit integrates galvanic isolation of logic level inputs signals, positive and negative isolated auxiliary power supplies and short circuit protection by $V_{CE(sat)}$ monitoring. Due to the compact design, this circuit is easy to mount on a PC board close to the power module in order to minimize parasitic elements. Isolated screw-on spacers guarantee good vibration withstand capability.
# Pin Description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>+15V</td>
<td>Supply Voltage</td>
<td>Positive power-supply voltage Input. All internal Aux. Power supplies are made from this Voltage including isolated secondary supplies. The range of this voltage is 14.5V to 15.5V (decoupling capacitor required)</td>
</tr>
<tr>
<td>0/15V</td>
<td>Power Ground</td>
<td>Internally connected to the GND pin and the primary ground plane. This pin must be connected to the Supply voltage Reference</td>
</tr>
<tr>
<td>H1</td>
<td>Channel 1 Input</td>
<td>Channel 1 Input signal has a Schmitt Trigger Characteristics to provide improved signal noise immunity. Logic High (5V) turn-on the IGBT. In addition Low impedance (typical 1K and 1nF) guarantees good noise immunity. A parallel 5V zener diode increase the Electrostatic Discharge Protection</td>
</tr>
<tr>
<td>H2</td>
<td>Channel 2 Input</td>
<td>Channel 2 Input signal has a Schmitt Trigger Characteristics to provide improved signal noise immunity. Logic High (5V) turn-on the IGBT. In addition Low impedance (typical 1K and 1nF) guarantees good noise immunity. A parallel 5V zener diode increase the Electrostatic Discharge Protection</td>
</tr>
<tr>
<td>Reset</td>
<td>Fault Reset Input</td>
<td>A logic High input for at least 20µs, resets fault output high and enable Outputs 1 and 2 to follow the respective Input level</td>
</tr>
<tr>
<td>FAULT OUT</td>
<td>Fault Output</td>
<td>Fault change from High Logic level (2.7K connected to +5V internal) to a logic Low following the voltage on VC1 or VC2 exceed 6.3V. Channel 1 and Channel 2 Fault outputs are open collectors connected together in a &quot;wire OR&quot; forming a single FAULT OUT pin.</td>
</tr>
<tr>
<td>GND</td>
<td>Input Signal Ground</td>
<td>Digital input ground pin should be connected to the low noise ground plane for optimum performances.</td>
</tr>
<tr>
<td>VC1</td>
<td>Collector Desat Channel 1</td>
<td>Desaturation Voltage Input. When the voltage on VC1 exceeds 6.3V while the IGBT is ON, FAULT OUT is changed from 5V to a Logic Low State and Turn-off the IGBT until Reset is brought high</td>
</tr>
<tr>
<td>Gon1</td>
<td>Turn-on Gate Output 1</td>
<td>Separate Turn-on and Turn-off gate Drive Outputs in order to Set Turn-on and Turn-off switching speed independently from each other.</td>
</tr>
<tr>
<td>Goff1</td>
<td>Turn-off Gate Output 1</td>
<td>Those pins are connected through a resistor to the gate of IGBT with short wire length (see &quot;Gate Resistors Calculation&quot;)</td>
</tr>
<tr>
<td>0V1</td>
<td>Common Output Supply Voltage</td>
<td>This pin is directly connected to the Emitter of the IGBT or through a resistor to minimize Gate ringing in case of paralleling operations</td>
</tr>
<tr>
<td>0V2</td>
<td>Common Output Supply Voltage</td>
<td>This pin is directly connected to the Emitter of the IGBT or through a resistor to minimize Gate ringing in case of paralleling operations</td>
</tr>
<tr>
<td>Goff2</td>
<td>Turn-off Gate Output 2</td>
<td>Separate Turn-on and Turn-off gate Drive Output in order to Set Turn-on and Turn-off switching speed independently from each other.</td>
</tr>
<tr>
<td>Gon2</td>
<td>Turn-on Gate Output 2</td>
<td>Those pins are connected through a resistor to the gate of IGBT with short wire length (see &quot;Gate Resistors Calculation&quot;)</td>
</tr>
<tr>
<td>VC2</td>
<td>Collector Desat Channel 2</td>
<td>Desaturation Voltage Input. When the voltage on VC2 exceeds 6.3V while the IGBT is ON, FAULT OUT is changed from 5V to a Logic Low State and Turn off the IGBT until Reset is brought high</td>
</tr>
</tbody>
</table>

## Table 1 Pin Function and Description

### Features:
- Common mode rejection higher than 10 kV/µs for very high noise immunity.
- 2500V galvanic isolation between primary and secondary and between the two secondary.
- 5V logic level with Schmidt trigger input.
- Low speed over current cut off (coupled with short circuit protection) to limit over voltage.
- Separate sink & Source outputs for turn-on and turn-off switching optimisation.
- Single V_DD=15V supply required.
- Secondary auxiliary power supplies under voltage lockout with hysteresis. The +15V bias voltage ensures low IGBT saturation voltage while the –5V guarantees fast turn-off and good noise immunity, even in an electrically noisy environment.
1- Drive Power Calculation

To determine if the IGBT driver is well suited for the application the main parameter is the total gate charge of the IGBT ($Q_g$). Most of power semiconductor data sheet specify the IGBT total gate charge with the corresponding gate voltage applied.

In this application note we will also examine some simple methods to determine the Total Gate charge.

1-1 Effective Gate Capacitor Determination

During each turn-on and turn off operation the driver must charge and discharge the effective gate capacitor, so the higher the switching frequency, the higher the driver consumption is. This effective gate capacitor may be calculated by the relation:

$$C_{EFF} = \frac{Q_g}{V_{GE}} \text{ with } V_{GE}=15V$$

Application:
The Total Gate charge Curve (see APTGF300A120 data sheet for example) gives a $Q_g$ of 2200µC @ $V_{GE}=15V$.

By the formula the effective capacitor can be calculated:

$$C_{EFF} = 146 \text{ nF}.$$ 

So the “Frequency vs. Effective Gate Capacitance” curve (see Fig. 2) allows verifying if the driver is well suited to the application. In our example, the frequency at 25°C is close to 40 kHz.

![Frequency Vs Gate effective Capacitor](image)

Figure 2  Switching Frequency vs. Effective Gate Capacitance

The driving power per channel and the consumption in the primary auxiliary power supply are:

$$P_{perchannel}(W) = C_{EFF} \times (\Delta V_{Gate})^2 \times F_{8Q}$$

(Normally the power necessary to charge a capacitor is $\frac{1}{2} CV^2f$, but in this case, during a switching period the driver must charge and discharge the effective capacitance, resulting in twice the power).
1-2 Example of phase leg operation

The total amplitude generated by the IGBT driver is 20V (15V positive, -5V negative). So the power per channel at 40 kHz and 146nF is:

\[ P = 2.3\, \text{W} \]

Additional losses like gate driver’s DC/DC converter efficiency must also be added (it represents around 30% of total losses).

The maximum steady state power dissipation of the driver is close to 1.2W (due to biasing the device). So the total primary power consumption (gate driver supply voltage=15V) is:

\[ P_{\text{TOTAL(primary)}} = 7.2\, \text{W} \]

@ Frq=40 kHz and C_{EFF}=146nF

The maximum switching frequency is also dependent on the ambient temperature. The following Figure 3 “Switching Frequency vs. Ambient Temperature” gives the derating to observe.

![Figure 3 Switching Frequency vs. Ambient Temperature](image)

1-3 Total gate Charge Measurement

- In general the effective capacitance (C_{EFF}) is close to the input capacitance value (C_{ies}) increased by a factor 5.

\[ C_{EFF} = 5 \times C_{ies} \]

And

\[ Q_g(nC) = C_{EFF} (nF) \times Voltage\, Rise(V) \]

The difference is more particularly due the the Miller plateau effect (as shown in Fig. 4) corresponding to the flat portion of the curve.
1-4 Measurement methodology

If a more accurate value is needed, the following method based on the Gate current measurement is very simple (see Fig. 5).

Important: The gate charge is increasing with the IGBT Collector voltage amplitude. So it is important to apply the same collector voltage as in the final application.

A digital oscilloscope combined with “Integral” math function analysis on the Gate current waveform gives the gate charge value by the formula:

$$Q = \int idt$$

The measurement gives: $Q = 2400\text{nAs}$

$$C_{\text{EFF}} = \frac{Q}{20} = 120\text{nF}$$

By comparison, the total gate charge for $V_{GE} = 0$ to $15\text{V}$ is:

$$Q_G@15\text{V} = 1800\text{nC}$$

Figure 4  Typical Gate Charge Curves

Figure 5  Gate Charge Measurement
2- Gate Resistors Calculation

The choice of the turn-on and turn-off gate resistors is critical in order to optimise the IGBT switching losses without exceeding the current capability of the driver.

The typical values of Ron and Roff are given in Table 2, “Typical External Components Values”.

Table 2  Typical External Component Values

<table>
<thead>
<tr>
<th>APT - Modal SP6 package</th>
<th>Technology</th>
<th>IGBT</th>
<th>Ron (ohms)</th>
<th>Roff (ohms)</th>
<th>Total gate charge (nC) @15V</th>
<th>Frequency up to (Khz) **</th>
<th>R return (ohms)</th>
<th>Additional Diode *</th>
</tr>
</thead>
<tbody>
<tr>
<td>600V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>APTGF350A60</td>
<td>NPT</td>
<td>6.8</td>
<td>6.8</td>
<td></td>
<td>1320</td>
<td>50</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>APTGT300A60</td>
<td>Trench/Fieldstop</td>
<td>4.7</td>
<td>4.7</td>
<td></td>
<td>2150</td>
<td>20</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>APTGT600A60</td>
<td>Trench/Fieldstop</td>
<td>2.2</td>
<td>2.2</td>
<td></td>
<td>4300</td>
<td>10</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1200V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>APTGF150A120</td>
<td>NPT</td>
<td>10</td>
<td>10</td>
<td></td>
<td>850</td>
<td>50</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>APTGT150A120</td>
<td>Trench/Fieldstop</td>
<td>10</td>
<td>10</td>
<td></td>
<td>700</td>
<td>20</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>APTGT200A120</td>
<td>Trench/Fieldstop</td>
<td>6.8</td>
<td>6.8</td>
<td></td>
<td>950</td>
<td>20</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>APTGF300A120</td>
<td>NPT</td>
<td>3.9</td>
<td>3.9</td>
<td></td>
<td>2250</td>
<td>25</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>APTGT400A120</td>
<td>Trench/Fieldstop</td>
<td>3.3</td>
<td>3.3</td>
<td></td>
<td>1850</td>
<td>20</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1700V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>APTGT150A170</td>
<td>Trench/Fieldstop</td>
<td>6.8</td>
<td>6.8</td>
<td></td>
<td>850</td>
<td>20</td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>APTGT300A170</td>
<td>Trench/Fieldstop</td>
<td>3.3</td>
<td>3.3</td>
<td></td>
<td>1700</td>
<td>20</td>
<td>0</td>
<td>X</td>
</tr>
</tbody>
</table>

Caution : A dead time must be observed between H1 and H2 input signals ( see “dead time” Chapter)
* : This external diode ( STTH112U from STM for example) must be connected between VC pins and IGBT collector to increase voltage capability
** : due to the driver and/or the power module switching frequency limitation ( Tamb = 85°C, Tcase module = 80°C)

Table 2  Typical External Component Values

2-1 Gate resistors Minimum Value Calculation

A minimum gate resistor value must be observed to avoid IGBT Driver damage.

The peak current is limited at 8A during turn-on and 15A during turn-off.

To calculate the minimum “ON” and “OFF” gate resistors (see Fig. 6 and Fig. 7), it should be considered that the APTRG8A120 is turned-on at +15V and turned-off at –5V therefore the gate voltage amplitude is 20V during every switching procedure.

\[
RG_{ON\min} = \frac{\Delta VG}{I_{PEAKon}} = \frac{20}{8} = 2.5\Omega
\]

\[
RG_{OFF\min} = \frac{\Delta VG}{I_{PEAKoff}} = \frac{20}{15} = 1.33\Omega
\]

In fact the IGBT gate model integrates a series resistance, so in practice:

\[RG_{ON\min}=2\Omega\]

\[RG_{OFF\min}=1\Omega\]
Also the wire length between the driver and the power module must be as short as possible. Parasitic elements in the drive loop (like emitter inductance) clearly alter the performance. In general IGBT power modules integrate a Kelvin emitter sense terminal to minimize this drive loop effect.

3- Dead Time and Drive Interlock

In case of phase leg operation, a dead time must be applied between the two input signals (H1 and H2) to ensure the complete turn-off of the active IGBT switch before turn-on of the opposite switch. If not, then short cross conductions appear which increase the losses and may destroy the IGBTs. Generally those cross conductions are short enough to disappear before the end of the necessary \( V_{CE(sat)} \) detection blanking time, so the short circuit protection will not be activated.

3-1 Minimum dead Time Calculation

The dead time is the difference between the maximum total turn-off delay time and minimum total turn-on delay time (see Fig. 8 and Fig. 9 “Tdon and Tdoff measurements”). This includes driver, gate resistors and IGBT delay times. Note that the driver data sheet gives the “Propagation Delay Difference Between any Two Drivers” (PDD) which simplifies this calculation.

Note that most of the drive losses are dissipated in the external gate resistors independently of the resistors values. In the previous example (primary power consumption calculation in phase leg operation) the Ron and Roff power will be:

\[
P = \frac{2.3}{2} = 1.15 \text{ W}
\]

In order to have good safety margin we propose:

Rgon, Rgoff = PR02 series (2W metal layer)

Low inductance metal layer resistors are recommended.
So the equation of the Minimum dead time becomes (ns):

\[
DT_{\text{min}} = (R_{\text{goff}} \cdot C_{\text{ies}}(\text{max}) \log_2 + T_{\text{off IGBT}} + T_{\text{on}}) - (R_{\text{gon}} \cdot C_{\text{ies}}(\text{min}) \log_2 + T_{\text{on IGBT}} + T_{\text{off}}) + PDD
\]

With

- \( C_{\text{ies}} \) = Input Capacitance
- \( R_{\text{goff}} \) = Turn-off gate resistor
- \( R_{\text{gon}} \) = Turn-on gate resistor
- \( H \) (Input Driver Signal)
- \( I_{\text{C}} \) (Output Collector Current (A))

3-2 APTGF300A120 Calculation Example

With \( R_{\text{gon}} = R_{\text{goff}} = 2R \) and \( R_{E} \) (emitter resistor) = 0R

\[
DT_{\text{min}} \text{ (nS)} = (41 + 500 + 30) - (30 + 70 + 50) + 350 = 771 \text{ ns}
\]

Recommended Dead Time: 1µs

3-3 Drive Interlock

This function prevents two IGBT's in the same leg from being turned on at the same time as shown in Table 3, “Operation Table”.

4- Suppression of gate ringing by \( R \) return

When IGBT module paralleling is necessary it is best to use a common gate drive. Using different driver circuits introduces additional variation in turn-on and turn-off time and possible imbalance between each power module.

To avoid gate ringing during the switching transient (collector voltage transition), an additional resistor may be connected between emitter sense connection and the common supply (0V) of the driver.
### Operation Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Secondary UVLO Desat Condition Detected</th>
<th>Reset</th>
<th>Fault Output</th>
<th>OUT G1</th>
<th>OUT G2</th>
</tr>
</thead>
<tbody>
<tr>
<td>H1 Low</td>
<td>X</td>
<td>X</td>
<td>Low</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Low</td>
<td>X</td>
<td>X</td>
<td>Not Active</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Low</td>
<td>X</td>
<td>X</td>
<td>Not Active</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Low</td>
<td>X</td>
<td>X</td>
<td>Not Active</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>High</td>
<td>X</td>
<td>X</td>
<td>Not Active</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>High</td>
<td>X</td>
<td>X</td>
<td>Not Active</td>
<td>High</td>
<td>Low</td>
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<tr>
<td>X</td>
<td>X</td>
<td>Active</td>
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<td>Low</td>
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<td>High</td>
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<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Not active</td>
<td>High</td>
<td>X</td>
</tr>
</tbody>
</table>

* : in all of the cases only one of the two outputs may be High at the same time, generally the first channel high will keep high Output level but un case of synchonise input signal the response time of each internal component will determine the high level channel and could not be garany.

** : The fault condition is memorized until Reset input is brought low, then a logic high for at least 20µs reset fault output and enable Inputs. A period of time (100 mS minimum) must be observe between each reset pulse in order to avoid the destruction of Power IGBT by over heating.

### Table 3 Operation Table

This additional “return” resistor combined with the traditional gate resistor permits driving each power device gate input in a differential mode that helps to eliminate the effects of possible oscillations (see Fig. 10, “Paralleling of Power Modules Block Diagram”).

Generally the power modules integrate emitter sense connections that reduce the driving loop effects.

In case of discrete semiconductors never forget that parasitic elements like inductance in the drive loop clearly alter the circuit performance and will increase switching losses.

Note that separate distributed resistors (Ron, Roff and Rreturn) must be matched for best synchronization. A bi-directional tranzorb should also be added to protect the IGBT gate from over voltage spikes (Z1, Z2 in Fig. 10).

![Figure 10 Paralleling of Power Module Block Diagram](image-url)
5- Protections

5-1 Short circuit protection by VCEsat monitoring

Each driver provides a short circuit protection by VCEsat monitoring. If the drive senses that the voltage across the IGBT (at ON state only and from the VC pins) is greater than 6.3V, the short circuit conditions has been detected, the corresponding driver output is slowly turned off as shown in Fig. 11 and the fault output immediately activated. The fault conditions are stored until a logic high signal for at least 20µs is applied to the reset input. The total driver reaction time in case of short circuit is 5µs, with a short circuit duration that will not exceed 6µs.

The fault outputs of each channel are connected together in a “Wired OR” forming a single fault output pin. This is an open collector with an integrated pull up resistor of 2.7K. The other side of this pull up resistor is connected to the internal 5V supply. In order to increase the immunity it is recommended to add an external pull-up resistor close to the digital components. Due to the switching over-voltage spikes (in spite of decoupling capacitors) or following a short circuit (in spite of slow turn-off) a safety margin must be observed between the VBUS voltage and the IGBT breakdown voltage (BVces) like the Vc pins maximum voltage (1200V).

See Fig. 1 “Phase Leg Operation Block Diagram”.

Note that in normal operation (no fault) the reset input may be high or low without any action inside the driver. A period of 100ms must be considered as a minimum between each reset signal to prevent the destruction of the IGBT by over heating.
For 1700V applications an additional fast diode (STTH112U from STM for example) must be connected between the Vc pins and the IGBT collector.

5-2 Secondary Auxiliary power supplies under voltage

The APTRG8A120 under-voltage lockout (UVLO) feature is designed to prevent against insufficient IGBT gate voltage.

The IGBT saturation voltage is increased significantly when the gate voltage amplitude is under 13V and dramatically when below 11V.

In this case the conduction losses are so important that they may damage the IGBT by over heating.

The UVLO will turn off the output if the secondary power supply voltage falls below 12.3V (typical) with a hysteresis of 0.4V minimum to prevent erratic operation.

6- Mounting Instructions

The IGBT driver is dedicated to be mounted on a PC Board and fixed with 4x M3 screws in order to increase the vibration withstand capability.

The recommended diameters for drill holes are 1 mm for the 18x 0.6mm square @2.54 mm raster gold plated connectors.

To minimize parasitic elements, the driver and other external components must be as close as possible to the IGBT Power module.

For this reason the PC Board will be fixed on the same support as the module (the heat sink generally).

See Fig. 12 “Recommended Layout and Mounting”.

In the case of SP6 power module, keep a distance of at least 5cm between the 2.8mm fast-on connectors and the spacer, which supports the PCB, to avoid mechanical stress.

See “SP6 Mounting Instructions” application note APT0601.

Note that the screw-on spacers are totally isolated from the rest of the circuit and are also isolated from each other.

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**Figure 12 Recommended Layout and Mounting**

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Conclusion

The APTRG8A120 Drivers Circuit simplifies the power systems design by offering most of the functions necessary to set up and protect power IGBTs. This application note describes how to use this circuit to obtain the best performance. We also demonstrate that IGBT operating parameters must be considered to design a reliable power system.

The parameters can be summarized by the following checklist:
- Total Gate charge (Qg)
- Input capacitance (CIES)
- Turn-on and Turn-off delay times (Tdon, Tdoff)
- Turn-on and Turn-off times (Ton, Toff)
- Breakdown Voltage (BVCES)
- Maximum switching Frequency (Frq)

References

1 Ralph McArthur “Making Use of Gate Charge Information in MOSFET and IGBT Data Sheets” Application Note APT0103 Advanced Power Technology.
2 “Use Gate Charge to Design the Gate Drive Circuit” AN944 International Rectifier
4 Serge Bontemps Product Manager “Parallel Connection of IGBT and MOSFET Power Modules” Application Note APT0405 Advanced Power Technology.