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APPLICATION NOTE

A 50 MHZ, 250W AMPLIFIER USING PUSH-PULL ARF448A/B

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ABSTRACT

This paper describes a simple and inexpensive power amplifier based on the new series of RF-power MOSFETs from Advanced Power Technology (APT). The geometry of these devices has been optimized for RF performance and the common source package provides for simple and thermally efficient mounting. It features a high operating voltage which permits simpler output matching and a less expensive power supply. The PA delivers 250W with 15dB gain at 50MHz. The amplifier is built around a "symmetric pair" of common source RF power MOSFETs housed in the economic TO-247 package. This paper addresses both the theoretical design and the practical construction of the circuit. Operating at higher voltages is not without challenges. Strategies are discussed for dealing with the effects of output and feedback capacitance in the higher impedance environment.

INTRODUCTION

As part of the family of new RF power MOSFETs, the ARF448A and ARF448B symmetric pair of devices has been introduced to accommodate designs in the 75 to 150 Volt regime. These devices follow the ARF446/7 pair which are characterized for 150 to 300 Volt operation. These devices are targeted at high voltage single frequency class C operation primarily in the 13.56, 27.12, and 40.68MHz ISM bands. High voltage operation is quite different from the conventional low voltage solid state RF design paradigm. The following section is intended to aid the designer in making this transition.

APPLICATION

The design goals for the amplifier in this note were as follows.

Operating voltage:	>100V
Frequency:	50MHz
Gain	> 15dB
Output power	250W
Efficiency:	>70%
Ruggedness SWR:	>20:1

The ARF448A/B have respectable high frequency gain as shown in Figure 1. At the 50MHz design frequency about 17dB gain should be available from the device. This gain margin, especially in a Class C amplifier is adequate, depending on the efficiency goal.

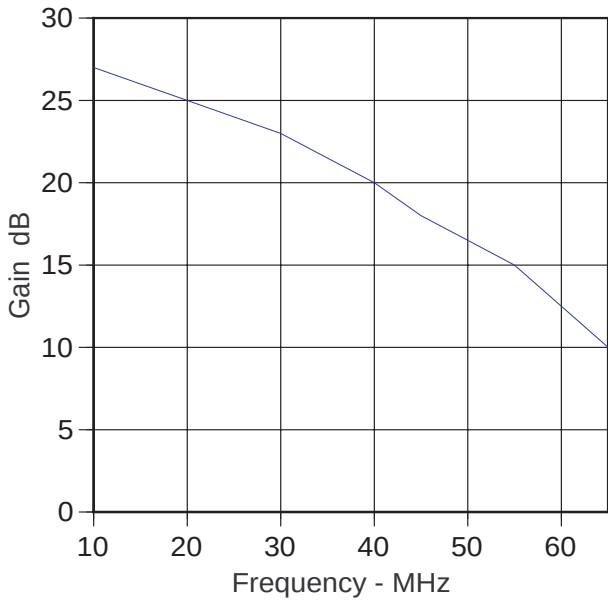


Figure 1 Gain vs. Frequency for ARF448

The input impedance of the device can be represented as a very high Q capacitor. The input capacitance can be read from the graph on the specification sheet at the intended drain voltage. For the ARF448, this is 1400pF for a Vdd of 125V. The series equivalent real part of the input capacitance is less than 1 Ohm. The output impedance is determined by the output power, drain voltage, and class of operation. The basic equation for calculating a single amplifier transistor load impedance is shown in equation (1).

This is derived from $R = E^2/P$ and takes into account the "on" voltage of the MOSFET. It accurately calculates the parallel load resistance for class A, AB, and B applications but does not deal well with Class C operation.

$$R_p = (V_{dd} - V_{ds(on)})^2 / 2\,P_o \qquad (1)$$

For class C operation, a revised equation (2) is used to take into account that the drain voltage is not really a pure half sine wave, the lower duty cycle of class C, the effects of saturation voltage, and the lead inductance found in a typical circuit.[1]

$$R_p = (0.85V_{dd})^2 / 1.7\,P_o \qquad (2)$$

Since Vdd is now 150V, Rp is nine times higher than an equivalent 50V design. This can lead to a dramatic simplification of the matching back to a 50 Ohm output load. There is a caution here, however. The output capacitance of a power MOSFET is roughly equal to that found in an equivalent low voltage device. Since the parallel output resistance is now much larger due to the higher operating voltage, the effect of the output parallel capacitive reactance is increased because the effective Q of the output is now higher. In other words, the output capacitive reactance is no longer swamped by a low output resistance. This is of some consequence to the designer of broadband circuits.

Fortunately, that is not the case here. This is a relatively narrow band design. We must still deal with the effects of the output capacitance but it is very easily done.

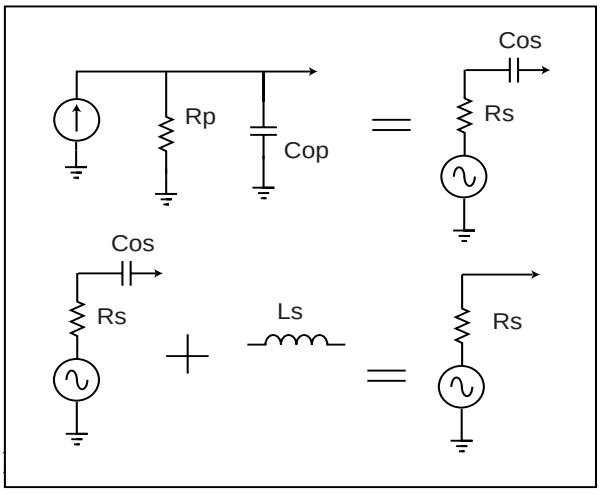
AMPLIFIER DESIGN

The design of a high power push-pull amplifier operating from 150 Volts requires several decisions. The class of operation has been specified as class C. The output power and operating voltage cannot conveniently be decided independently of each other as shown in Equation (2). The deciding factor here is the type of output network.

Push-pull operation requires a balanced circuit. The voltage to the drain of each transistor is to be fed through a bifilar choke wound on a ferrite core. This configuration is very common and provides several advantages among which are balanced flux in the magnetics of the choke and eliminating the dc from the output balun.

125V for Vdd was chosen as a compromise between maximum power and ruggedness. With each transistor providing 125W, the individual drain impedances are 90 Ohms in parallel with the output capacitance, Coss, of 1400pF. Without any compensation for the Coss, operation would be severely compromised.

The output capacitance can be compensated by either a shunt or series inductance. Since it was already decided to use the bifilar shunt feed choke, a series compensation inductance is used here for several reasons. The 90 Ohm output impedance represents a significant voltage swing at the drain which, if placed across the feed choke would cause it to saturate and get very hot. By using the shunt Coss as the first element in a L network impedance transformer, the bifilar feed choke can operate quite comfortably at a significantly lower impedance.



In order to deal with a purely resistive drain impedance, a coil is placed in series with each of the drains. The value of Rp is determined by Equation (2). The value of Coss is an inverse function of Vdd, like a varactor. Xcoss combined with Rp determine the load necessary for optimum operation. After the series equivalent of Rp and Xcoss is calculated, a conjugate match is obtained by using a series inductor. This process is shown graphically in Figure 2. C_{op} refers to the parallel output

capacitance, C_{oss}.

The Rp is calculated from equation (2) as 90 Ohms and the output capacitance is 125pF. At 50MHz the reactance Xcoss is -j25.4 Ohms. Calculating the value of Rs to be 6.6 Ohms, the voltage can be reduced or power raised just a little to obtain the desired Rs value for each drain which is 6.25 Ohms. This is transformed to 25 Ohms by the transformer action of the bifilar choke and two of these individual halves in series through the push-pull circuit gives a 50 Ohm output impedance.

There are two options available when the desired series equivalent output impedance cannot be secured with a reasonable value of drain voltage or if the output power is fixed. Both require adding more components. A capacitor can be placed in parallel with the transistor to increase the Coss thereby reducing the effective Rs. The value of Ls is adjusted accordingly. Raising the effective Rs requires overcompensating the Xcoss by using a value of Ls larger than needed for resonance. If a shunt capacitor is then added across the load, this produces a higher effective Rs. See C8 in the schematic, Figure 3. The extra inductance and shunt capacitor together with the output capacitance form a Pi network. All this can be easily worked out on a Smith chart program.

AMPLIFIER DESCRIPTION

The input circuit is a challenge. Even though the DC impedance is very high, at 50MHz the input capacitance of the MOSFET makes the input impedance virtually an RF short circuit. It is possible to design a two or three element matching network to secure a match but the Q of such a network is high. A network with a minimum Q of 7 is required to make the transformation to the measured gate input impedance of 1 -j2 Ohms. A 9:1 transformer offers a means to obtain the larger part of the transformation without any adjustment or increase in Q. It has the added advantage that any leakage inductance absorbs some of the equivalent input capacitance. The final transformation is handled with a simple L network.

The input impedance does not remain constant over the range of output power. From zero drive through the level where output power first appears and up to full output, the input impedance moves through a fairly large range due to the effects of the Miller capacitance, Crss.

Depending on the characteristics of the driver, the output power can appear to 'snap on' suddenly as the drive is increased when the input network has been previously adjusted for a match. This is because as the output rises, the input match improves which increases the net delivered power to the gate, and the output power increases more and the net input power is then suddenly too high. In class C amplifiers this is not generally a problem. Application of forward bias also improves the situation by decreasing the variation in impedance.

Linear operation with these devices requires careful attention to the thermal compensation of the bias supply. The Gm is quite high and this, coupled with the negative temperature coefficient of threshold voltage Vth, causes the quiescent current to rise suddenly as the die heats. This can destroy the transistor by over dissipation in thermal runaway. Forward bias is not recommended at operating voltages over 125V.

CIRCUIT DESCRIPTION

Figure 3 shows the schematic of the 50MHz amplifier. The gate matching is done using a transformer and tuned network. The transformer provides the balanced feed required by the push-pull configuration as well as a 9:1 transformation.

The push-pull configuration increases the effective input impedance of a single MOSFET by a factor of four. The transformer secondary cannot be left floating – a ground reference must be provided for the gates. This provides a convenient place to insert bias, if used. Using the resistors as load snubbers for the input, it becomes a bit easier to match (larger real part) and lowers the Q at the expense of a dB of gain.

The output circuit demonstrates the results of the procedure described above for matching and

compensating for the output capacity of the devices.

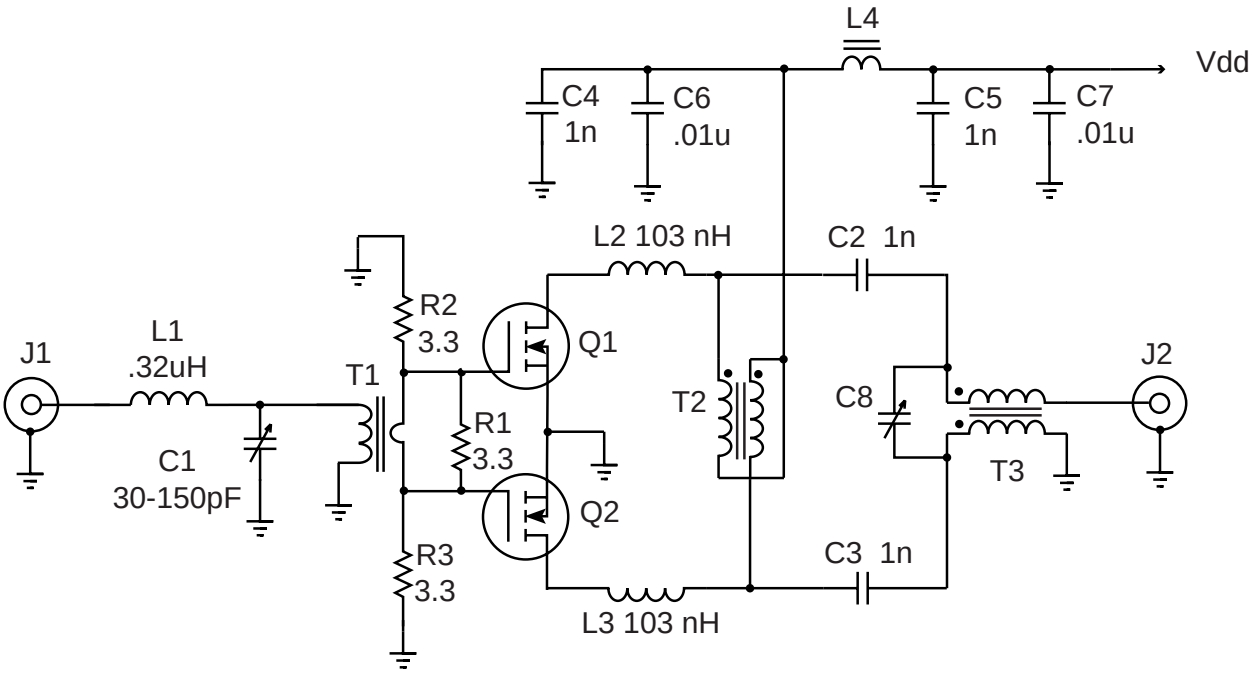


Figure 3 Schematic Diagram

L1 -12t #18ga .312" ID. L2, L3 - 3t#16.375"ID.
L4 - 2t#18 PTFE on a Fair-Rite #264354002 shield bead, μ_i = 850
C1, C8 - Mica compression trimmer 75-380 pF: Sprague GMA 30500.
C2, C3 - 1000V Ceramic chip: ATC 100E102KW
C4-C6 - 500V disc ceramic.
R1 - R3 - 1W metal film resistors
Q1 - ARF448A Q2 - ARF448B
T1 - 4:1 transformer Pri: 2t #18 PTFE coated wire, Sec: 1t 12ga braid on two Fair-Rite beads #2643540002, μ_i = 850
T2 - 6t #18 enamel wire bifilar on Fair-Rite #59610071801 toroid. μ_i = 125.
T3 - 1:1 balun, 5t RG-316 on two Fair-Rite #5961007601.

Here, the series compensation method is used and a larger value of series inductance is used to obtain a perfect match to 50 Ohms. The capacitor C8 is the shunt end of the output L-network.

T2 is the shunt feed bifilar choke. It is on the low impedance end of the L2/L3 compensating chokes so the RF voltage across it is small. With much less RF voltage across it, the toroid core does not saturate. The output coupling capacitors are large surface area types needed to carry the RF current. The inherent matching of the device assures good balance in a P-P circuit.

T3 is a 1:1 coax balun made with RG-316 Teflon coax.[3] Five turns are wound through two stacked toroids of μ_i=125 material (Fair-Rite #5961007601), the same core as used in the bifilar choke.

PERFORMANCE MEASUREMENTS

As can be seen from Figs. 5 and 6, the gain and efficiency at 50MHz are typical of classic class C operation. The maximum gain occurs at 150W, about 4dB more than the design value because of the compression needed to achieve class C operation. Maximum efficiency occurs where the output and input achieve a conjugate match to the load and source.

In the process of checking the design, operation

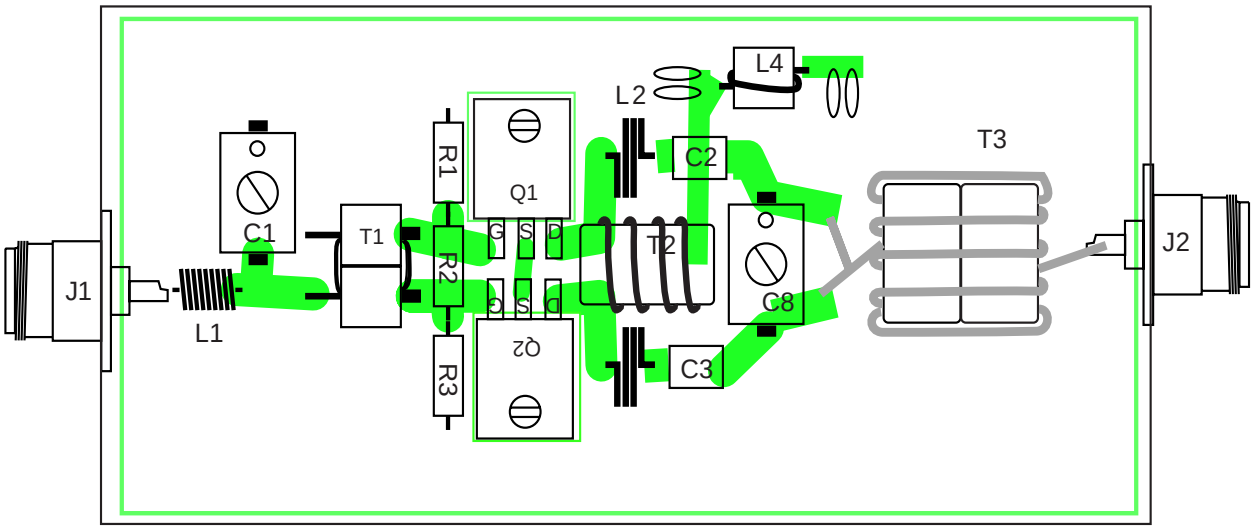


Figure 4 Circuit Layout

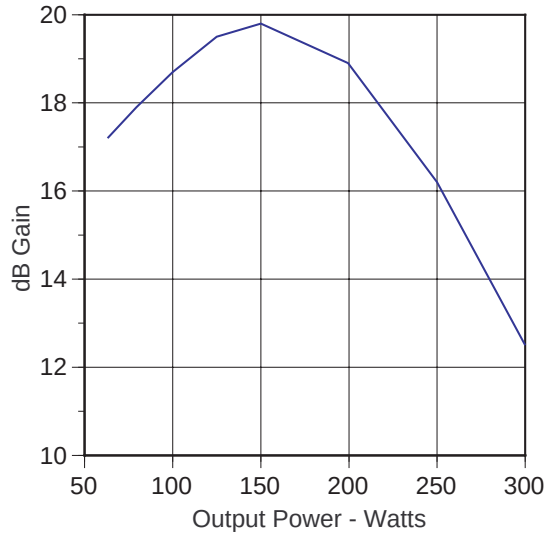


Figure 5 Gain vs. Output Power

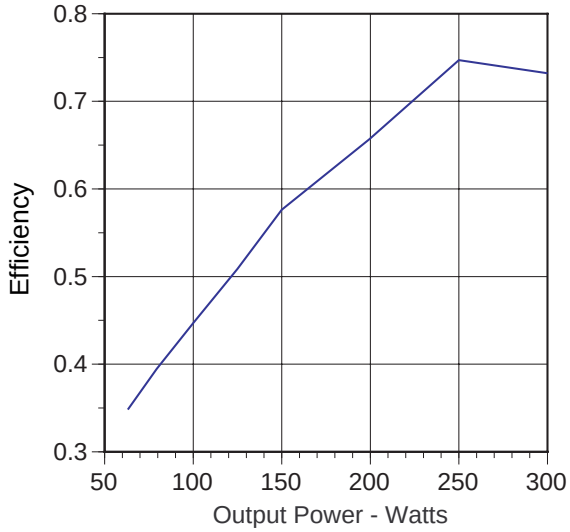


Figure 6 Efficiency vs. Output Power

without retuning was checked in five volt Vdd increments from 110 to 135V. Results clearly showed best gain and efficiency at the 125 Volt design center. It was possible to achieve reasonable operation from 100 to 150 Volts with retuning, but the peak efficiency suffered. If a large departure from the design center is intended, a change in L2 and L3 is required.

A load tolerance test was performed at 25:1 VSWR using a length of PTFE coax as an attenuator and a tuned circuit to vary the phase of the reflection coefficient.[3] No instability or failures resulted.

DEVICES

The devices used for this amplifier are ARF448A and ARF448B from Advanced Power Technology. These are an identical pair of MOSFETs in a symmetrical common source TO-247 package. The voltage rating of these is 450V BVdss. Equivalent 900V devices are ARF446 and ARF447. These higher voltage units were substituted in the circuit of Fig. 3 for comparison. The gain was lower by 2dB and the efficiency was less by 10%. The difference in efficiency is due to the higher Vds(on) of the high voltage devices. Almost equivalent gain could be had with slightly different tuning. This clearly demonstrates the wisdom, when efficiency is a

concern, of using devices that are optimized for the voltage you are using.

CONSTRUCTION

The layout of the amplifier is shown in Figure 4. The amplifier was built on double sided 1oz. copper clad FR-4 material mounted directly on an extruded heat sink. The back side was left intact with all the parts surface mounted except for the transistors. Two rectangular holes were cut to permit mounting the transistor packages directly on the heat sink beneath. All the edges of the board and three sides of the rectangular holes were wrapped with copper foil to obtain good connection between the top and bottom ground planes.

A piece of copper foil was also placed at the source connections to make a DC connection with the backside ground plane. If a low inductance connection can be made between the two sources in a push-pull amplifier, the length of the connection from that point to ground does not effect the gain since it only carries DC – it is not part of the RF circuit. In circuit layout it is imperative that absolute symmetry be maintained between the two halves of the amplifier, especially on the gate side where the impedance is very low. The mirror image packaging of the ARF448 devices greatly facilitate this layout.

CONCLUSION

This paper demonstrated an application of the recent breakthrough in RF power device technology by APT. The problems associated with high voltage, large area devices are identified, and solutions are discussed. The devices are demonstrated in a practical 250W push-pull amplifier at 50MHz.

These devices are the first from this new MOS V process and the first with RF-specific geometry. More devices in this family will be forthcoming – both high power and high voltage – devices for the generation of RF power at HF up to 100MHz.

[1] Kraus, Bostian, and Raab, *Solid State Radio Engineering*, John Wiley & Sons, Inc., New York, 1980.p.405

[2] William E. Sabin, Edgar O. Schoenike, et al, *Single Sideband Systems and Circuits,* McGraw-Hill 1993.

[3] Franke and Noorani, "Lumped-Constant Line Stretcher for Testing Power Amplifier Stability", RF Design, Mar/Apr 1983.

Editor's Note

Since this artile was published, APT has developed an improved device, the ARF460A and ARF460B. They will substitute directly in this application.
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