APT0002
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APPLICATION NOTE

New 500V Linear MOSFETs
for a 120 kW Active Load

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Summary

Power MOSFETs are generally designed as switches. Total power dissipated is the sum of "on"-state losses (Id^2 x Rds(on)) plus losses generated during the very short switching intervals. Desirable characteristics include the lowest possible ON resistance, high breakdown voltage, very high gain (g_{fs} or G_m), minimum switching losses, and a low gate threshold voltage $V_{GS(th)}$.

   In those applications requiring operation in the linear region, these characteristics are not ideal. Firstly, G_m is too high and, secondly, $V_{GS(th)}$ has a negative temperature coefficient ($\Delta V_{th}/\Delta T_J$), which makes it impossible to maintain constant drain current without negative feedback. Finally, and most dangerous of all, large switchmode MOSFETs exhibit a phenomenon known as "hot spotting" or current tunnelling.

   In an ideal device, current density across the die is uniform and the resulting junction temperature profile is also uniform. In practice, however, minor imperfections such as small voids in the die attachment solder or non-homogeneous junction doping etc, cause non-uniform current distribution and variations in the junction temperature profile. Hot spotting is then triggered by the negative temperature coefficient of gate threshold voltage acting in a localized manner. As one part of the die heats up more than another, the local junction $V_{GS(th)}$ falls and G_m then causes that area to turn on harder, drawing even more current. Since G_m increases with current, the runaway process accelerates rapidly until failure occurs.

   The development of the 500V APL501JN linear power MOSFET and its 1kV APL1001JN sibling was stimulated by the expressed desire of linear MOSFET customers to have greater usable power dissipation. Understanding the nature of hotspotting led to innovative re-engineering to lower the V_{GS} versus I_C temperature coefficient crossover point. In these new devices, the source structure has been modified to produce an asymmetric channel, that is one where some parts of the interdigitated single channel are longer than others. The effect of this is to reduce current density in the channel region which in turn lowers the tempco crossover point. The onset of forward biased thermal runaway is retarded, enabling up to 50% more usable power dissipation in the linear mode.

   One such application that has benefited from this new technology is the TDI Dynaload range of water-cooled dynamic loads. Here, individual 12kW modules are paralleled together to produce integrated and very compact power systems capable of dissipating up to 120,000 Watts, for such end uses as power supply testing.

Introduction

It is not appreciated in the all-pervasive switchmode world that power MOSFETs cannot and do not meet their published Forward Biased Safe Operating Area (FBSOA) ratings, because the average designer working in this discipline does not care. Such is not the case, however, among those engineers constrained to use these devices in the "linear mode", where significant and concurrent values of drain voltage and current produce very high internal power dissipation.

FBSOA Testing

There is no easy way to test for FBSOA, because it is by nature a destructive test. Furthermore, there are significant variations in capability from unit to unit within a production lot and even more between die lots. Statistical analysis of the results will yield both typical and limit values for the part. For commercial production, a screening test is used which tests to a minimum level.

The SOA test fixture uses a water-cooled heat sink to keep the case close to 25C. A test value of drain voltage is selected, typically 50 to 80 percent of the rated drain voltage. The drain current is sensed by a sense-resistor in series with the source. An op amp, with its non inverting input tied to a reference voltage, establishes the device drain current as a function of the sense-resistor voltage.. The test procedure is to gradually increase the drain current in steps until the DUT fails. Each of the steps is held for a minute to ensure that the junction temperature reaches equilibrium. The power dissipation at which failure occurs is recorded for each device, and this defines the DC Safe Operating Area.

If the current is pulsed and the pulse width kept less than the thermal time constant of the device, the failure point can be several times the rated power dissipation of the device. This demonstrates that the failure mechanism is hot spotting. Under pulsed conditions, the junction temperature is more uniform so that the "hot spot" does not have time to develop.

Forward biased safe operating area for a semiconductor device (FBSOA or just SOA for linear devices) is a triangular area bounded on the left side by a positive sloped line defined by the Rds(on) of the device, and on the right side by a negative slope line determined by the power dissipation of the device. A typical SOA curve is shown in Figure 1.
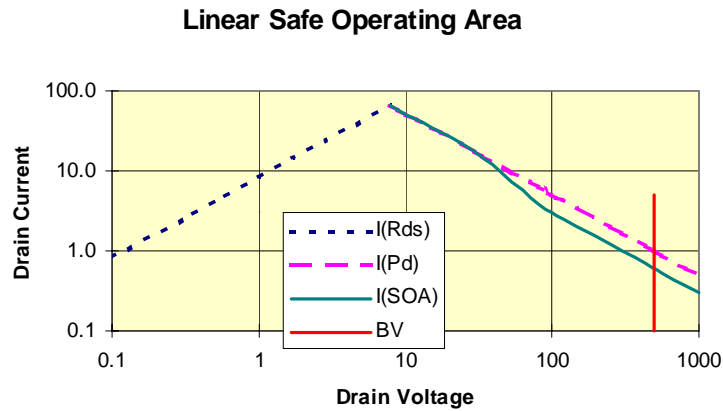
Linear Safe Operating Area

Figure 1   Typical FBSOA Curve

This figure appears on virtually every power device data sheet and, athough the $R_{\Theta JC}$ and $R_{DS(on)}$ parameters on which it is based are carefully measured and controlled by the manufacturer, the figure itself is derived by calculation and is seldom if ever rigorously validated.

In the case of switchmode devices, FBSOA is of little importance. The device is operated between two points on the figure, one on the Rds line at some current and one off the chart at some voltage and zero current. Power dissipation in a switched application is the sum of the on loss, $I_D^2 \times R_{DS(on)}$,and the dynamic switching losses which occur while making the transition between the two operating points. The characteristics which concern a switchmode designer are the $R_{DS(on)}$ characteristic and the parameters which determine the dynamic losses. Linear operation is different. The device is operated in a non-saturated mode, away from the $R_{DS(on)}$ line and somewhere within the SOA. In this mode, it behaves as a variable resistance, which is is exactly its role as a programmable active load.

Circuit for an active load

Linear operation of a MOSFET cannot be reliably accomplished without negative feedback. Whether as a "programmable resistor" in an active load or as the control element in a linear series regulator, the device must always be used inside a control loop. Within such a loop, thermal variations of V_{th} and G_m can be accommodated.

As a design example, consider the active device requirements for a programmable load to be used for testing a regulated power supply. The power supply has a maximum output of 3.5A at 300V. The active load will therefore need a device with a BV_{DSS} of at least 300V and must be capable of dissipating the entire output of the supply plus a safety factor to permit testing of the over current protection feature.

Devices suitable for the voltage requirement are fairly common, but a single device with more than 500W of usable power dissipation is not. The question is then to decide how many devices must be paralleled.

The APL501J device has a rated FBSOA of 300W and a rated power dissipation P_D of 520W, but as already explained this latter is not really usable in linear operation. The critical parameter defining allowable power capacity is R_{JC}. For an APL501J, R_{JC} is 0.24K/W and R_{CS} 0.6K/W, so if the desired operating T_J is 130°C and the sink is water cooled at 30°C, the allowable (switchmode) power dissipation is (130-30)/0.3 = 330W. However, since this exceeds the 300W FBSOA rating of the device, the 300W max FBSOA limit must prevail. Applying a 20% safety factor reduces this to 240W.

If the power supply being tested is capable of delivering 3.5A at 300V, the MOSFET load-bank must absorb 1050W. 1050W/240W = 4.4, so five devices in parallel are required, assuming that five devices can be configured to share the load equally.

Paralleling devices

No matter how carefully devices are matched for one given characteristic, G_m for example, differences in other parameters and variations in mechanical assembly will generally conspire to unbalance paralleled devices. Some form of feedback control is mandatory to assure current sharing, and the easiest way to do this is to install source resistors to monitor the drain current of each MOSFET. Resistor tolerances then determine the relative matching between the MOSFETs. The resulting resistor voltages are applied to the inverting inputs of operational amplifiers driving the gates, the non-inverting inputs being tied to a current-dependent reference voltage.

The value of the source resistor depends on the dynamic range of adjustment required, the noise content in the output, the minimum load resistance and the stability requirements of the system. A resistor outputting 1 to 2 volts maximum is ideal. The temperature coefficient of the resistors will determine the temperature stability of the system. Since the feedback is unique to each device, any number of MOSFETs may be paralleled without risk. The same current-dependent reference voltage can be applied to all the opamps. A typical arrangement is shown in Figure 2.
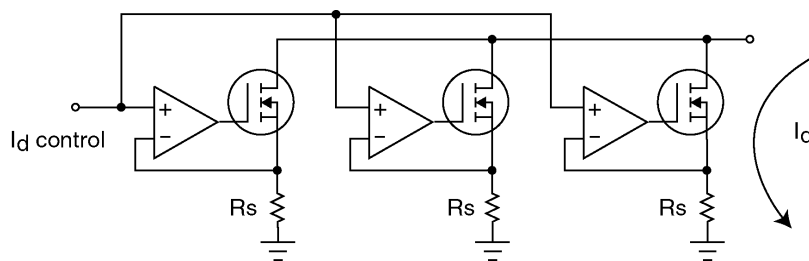

Figure 2- Paralleling several MOSFETS

Device changes to improve SOA

The development of the 500V APL501JN along with its 1kV APL1001JN stable-mate was stimulated by the expressed desire of potential users to have substantially increased allowable power dissipation in the linear mode. As already postulated, the fundamental mechanism behind MOSFET FBSOA failures is localized thermal runaway caused by "hot spotting". It results from the interaction between non-uniform heating over the surface of the die and the negative temperature coefficient of gate threshold voltage as illustrated in Figure 3.
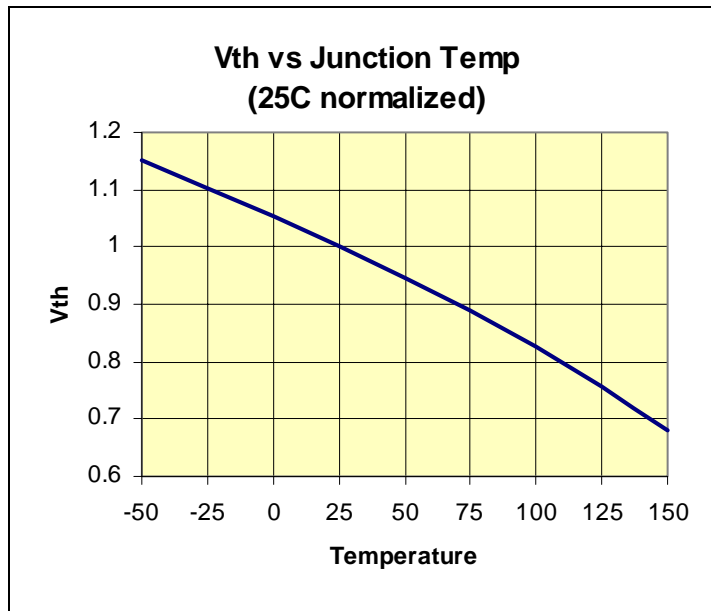
Vth vs Junction Temp (25C normalized)

[Figure 3: Plot of Vth (vertical axis, 0.6 to 1.2) vs Temperature (horizontal axis, -50 to 150). A downward sloping curve from about 1.15 at -50 to about 0.68 at 150.]

Figure 3

The phenomenon can be viewed as a classic example of an unstable feedback loop. From a device standpoint, only three variables can be manipulated to improve the stability of the system: $R_{\Theta JC}$, G_m, and the tempco of V_{th}.

- In the case of the APL501 and APL1001, $R_{\Theta JC}$ is a function of die size and the package, so is more or less fixed. In any event, since a bigger die would yield a lower $R_{\Theta JC}$ and a higher G_m, the net loop gain would remain unchanged.
- Within limits, the very high G_m of a switchmode device can be reduced considerably before difficulties start to appear in linear applications. Common MOSFET design rules indicate that G_m is generally inversely proportional to $R_{DS(on)}$ and proportional to channel width and die area.
- The primary means for improving SOA of the new design was to reduce its crossover or turnover current. Crossover current of the original switchmode part was 30A, this being where the transfer characteristic curves cross in Figure 4, or the current at which the slope is zero in Figure 5. By modifying the gate-source geometry using a fabrication process dubbed "asymmetric channel", the crossover current was reduced by half, with commensurate improvements in linear-mode FBSOA and usable power dissipation.
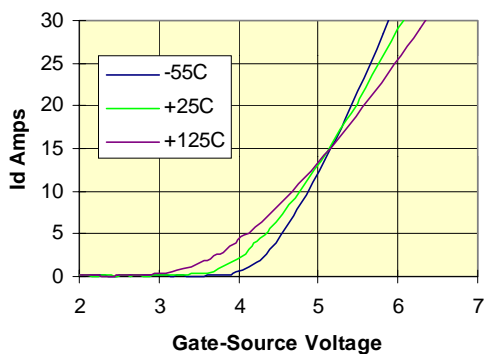
Transfer Characteristics vs Tj

[Figure 4: Plot of Id Amps (vertical axis, 0 to 30) vs Gate-Source Voltage (horizontal axis, 2 to 7). Three curves labeled -55C, +25C, +125C.]

Gate-Source Voltage vs Tj

[Figure 5: Plot of Normalized Vgs (vertical axis, 0.88 to 1.06) vs Junction Temp (C) (horizontal axis, -25 to 100). Five curves labeled .1 A, 1A, 2A, 4A, 5A.]
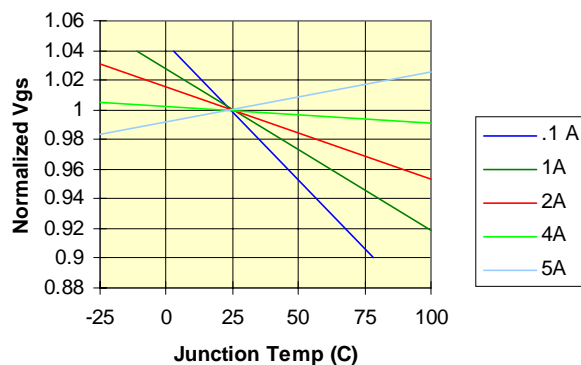
Figure 4

Figure 5

As can be seen from Table 1, crossover performance differs markedly among nominally similar devices - all having chip areas of about 128,000 sq mils. Note that the later high performance switchmode designs- characterized by higher speed, lower gate charge, tighter gate/source pitch, lower on-state resistance etc, all display progressively worse FBSOA performance as measured by crossover current. As a result, the new optimized linear design was based on the older MOS IV process, rather than on the more recent MOS V or MOS VI developments.

Device	Crossover Current	Device Process
APL501J	15A	New Linear Process
APT5010JN	30A	MOS IV®
APT5010JVR	62A	MOS V®
APT5010LLC	100A	MOS VI®

Table 1 Performance versus Process

A schematic cross section of the APL501J chip is depicted in Fig 6. Unlike the vast majority of competitive power MOSFETs that feature multi-cellular chip structures, APT devices are manufactured with a single-cell interdigitated gate and source structure. A proprietary process change results in the formation of a shorter channel length along one side of the structure. The net effect is the creation of two distributed parallel MOSFETs with different transfer characteristics. The portion of the die with the shorter channel length has a slightly lower gate threshold voltage (V_{th}) and a lower zero temperature coefficient point than the portion with the longer channel. At low drain currents, the low V_{th} portion of the die dominates the current flow. Since this portion of the die is operating closer to the zero temperature coefficient point, hot spotting and subsequent thermal runaway is less likely to occur. At higher currents, the current sharing between the two portions of channel becomes more uniform and operation approaches that of a device with a normal symmetrical channel structure. In this situation, the usable FBSOA is 50% higher than that of the original APT PowerMOS IV® switchmode device.
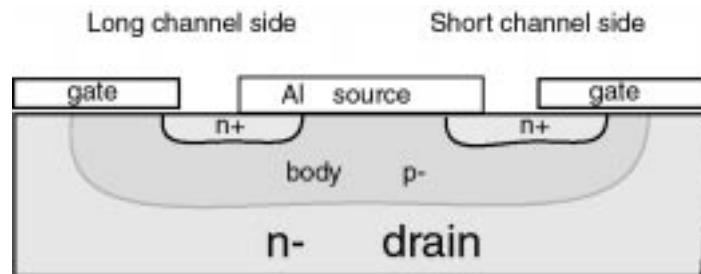

Figure 6 – Asymmetric Source

Conclusions

Incorporated into TDI-Dynaload's WCL series of 12kW water-cooled electronic load modules, which may be stacked together to dissipate up to 120kW at 400V or 10,000A per system, APT's new APL501J linear MOSFETs operate safely and consistently at power levels in excess of 300W at 400V. In comparison, SOT227 packaged

switchmode devices from other manufacturers are limited to about 100W at 400V. This vast improvement in FBSOA has allowed TDI to develop the highest power density electronic loads available today. Although the APL501J does exhibit the power roll off with applied drain voltage characteristic of all switchmode devices, this can be put to good advantage in the new device, in that the SOA curve shows a dramatic increase in power capability at lower voltages. At voltages below 100V, Dynaload has demonstrated that the APL501J is capable of dissipating up to 500W without failure.

Affiliations

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