

## Optimizing MOSFET and IGBT Gate Current to Minimize $dv/dt$ Induced Failures in SMPS Circuits

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The subcircuit in Figure 1 is found in many of today's switchmode power supply designs, including buck converters, boost converters, half-bridge converters, and full-bridge converters.

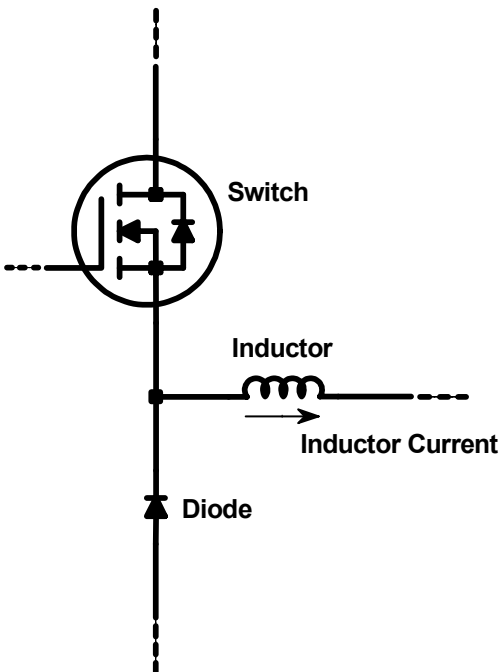


Figure 1. Generalized Switchmode Subcircuit

These are circuits in which the drive conditions do not change even though the current in the inductor changes as the load changes. The switch in general may be any semiconductor power switch that works, but MOSFETs and IGBTs will be in view

in this note. It is shown as a MOSFET in the figure. The diode in the subcircuit may be a discrete diode or in some cases it may be the intrinsic body diode of a MOSFET. It is shown as a discrete diode. Figure 2 shows an equivalent subcircuit for which the analysis is the same. That is, it does not matter which configuration is

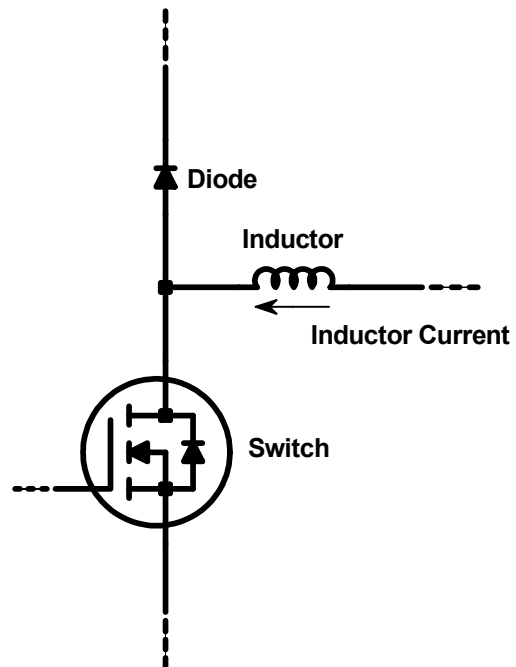
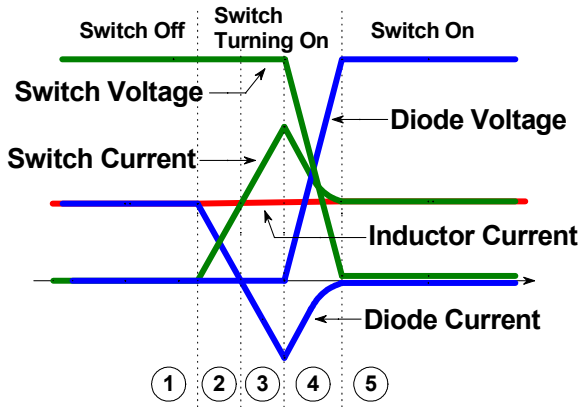


Figure 2. Generalized Switchmode Subcircuit

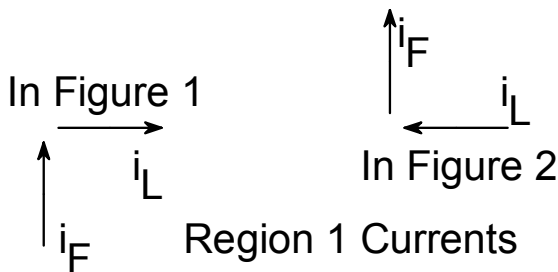
in view, the discussion in this note applies to both equally.

Figures 1 and 2 have three branches: the switch, the diode, and the inductor. The current in these three branches must sum to zero. Figure 3 illustrates the discussion that follows. Note the five regions numbered at the bottom of the figure.

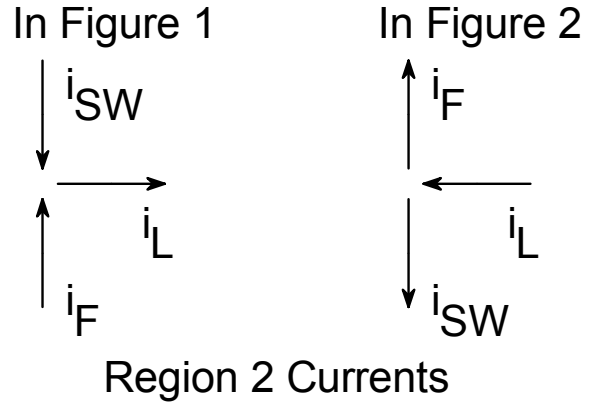


**Figure 3. Switch and diode voltage and current showing regions of activity**

**In region 1**, the switch is off. When the switch is off, the diode current equals the inductor current, because the switch current equals zero. This relationship is shown immediately below in the graphic depicting the region 1 currents with arrows. The switch current is not shown, since it is zero. The diode current is positive (see Figure 3) and is therefore labelled “ $i_F$ .”



**In region 2**, the switch is turning on. Region 1 ends and region 2 begins when the switch current begins to flow. As the switch current grows the diode current diminishes.



The following relationships exist:

$$\frac{di_F}{dt} = -\frac{di_{SW}}{dt} \text{ and}$$

$$i_{SW} + i_F = i_L.$$

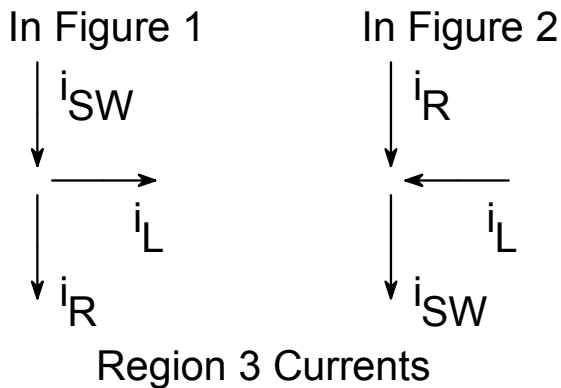
The first relationship, which says the slope of the diode forward current is equal and opposite to the slope of the switch current, is another way of saying that the switch current dictates the slope of the diode forward current in region 2. As will be stated later, the same is true in region 3. The second relationship is depicted in the graphic showing the region 2 currents with arrows. The inductor current equals the sum of the switch current and the diode current.

**In region 3**, the switch is still turning on and the diode current has become negative. Region 2 ends and region 3 begins when the diode current passes through zero. Now that the diode current has changed sign, it will be referred to as “ $i_R$ .” As the switch current increases, the negative diode current,  $i_R$ , increases. The following relationships exist:

$$\frac{di_R}{dt} = \frac{di_{SW}}{dt} \text{ and}$$

$$i_R + i_L = i_{SW}.$$

Again, the switch current dictates the slope of the diode current. This is the meaning of the first relationship.



The second relationship is depicted in the graphic showing the region 3 currents as arrows. The switch current equals the sum of the diode current and the inductor current in region 3.

The system stays in region 3 as long as there is enough stored charge in the diode to sustain the slope of the diode current ( $di_R/dt$ ) as dictated by the switch current.  $I_{RRM}$  is reached when the stored charge can no longer support the  $di_R/dt$  of region 3.

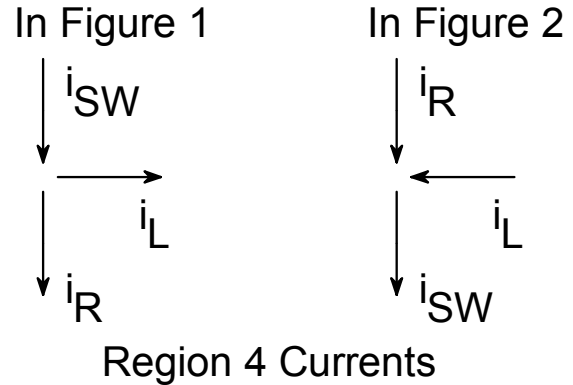
**In region 4**, the switch is still turning on. Indeed the switch is in the process of turning on in three regions—regions 2, 3, and 4. Region 3 ends and region 4 begins when the diode current reaches  $I_{RRM}$ . The diode current is still negative and is still referred to as “ $i_R$ .” In this region, as the diode current decreases, the switch current also decreases. Now the diode current is dictating the slope of the switch current. The following relationships exist:

$$\frac{di_{SW}}{dt} = \frac{di_R}{dt},$$

$$i_R + i_L = i_{SW}, \text{ and}$$

$$i_R = \frac{d(Cv_R)}{dt}.$$

Again, the diode current,  $i_R$ , is dictating the slope of the switch current, as indicated in the first relationship. The second relationship is depicted in the graphic showing the region 4 currents as arrows.



The region 4 currents have the same relationship with each other that the region 3 currents have: the diode current plus the inductor current equals the switch current. The third relationship shows the dependence of the diode current,  $i_R$ , on the diode’s reverse voltage and the diode’s capacitance. The capacitance, of course, is varying with the reverse voltage.  $i_R$  is the time rate of change of the product of diode capacitance and diode voltage.

It is important at this juncture to address a common idea about reverse recovery, namely, that  $i_R$  in region 4 does not depend on the circuit. This is only true when the switch tries to bring the diode reverse voltage up faster than the diode’s capacitance can be changed and charged. The capacitance changes as well as being charged. However, in the circuits we are discussing, very often the switch brings up the diode voltage less rapidly than the diode’s capacitance can be changed and charged. In this latter case,  $i_R$  does indeed depend on the circuit.

It is not until the system arrives in region 4 (or perhaps slightly before) that the switch voltage and the diode voltage begin to change. The change in the voltages and the occurrence of  $I_{RRM}$  take place at nearly the same time but for different reasons.

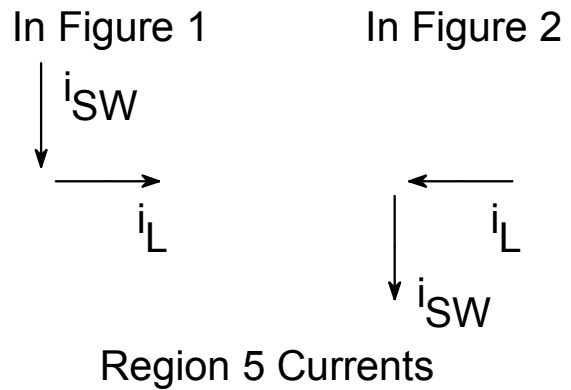
The switch voltage cannot begin to change until the diode voltage begins to come up. The switch brings about changes in the diode voltage as the switch is able to change its own voltage. However, this cannot come about until the diode voltage is able to be changed. In figure 3, the curve labelled “Diode Voltage” is really the inverted reverse voltage on the diode. That is, it is the voltage from the cathode to the anode. When the depletion region in the diode reaches its zero-bias width and the depletion region is able to expand beyond that width, the voltage on the diode begins to increase under the influence of the voltage imposed by the switch. That is, as the switch voltage begins to decrease, the cathode-to-anode voltage on the diode begins to increase. This moment may coincide with the moment  $I_{RRM}$  is reached, or it may precede it, depending on the amount of stored charge in the vicinity of the diode’s junction. As already stated,  $I_{RRM}$  is reached when the stored charge can no longer support the  $di_R/dt$  of region 3. Moving on through region 4, the switch voltage continues to decrease and the diode’s cathode-to-anode voltage continues to increase in response.

At the end of region 4, the diode’s reverse voltage has reached its target value and  $i_R$  has reached its leakage level. In other words, except for leakage, when  $v_R$  reaches the level of the applied voltage,  $i_R$  stops flowing. It cannot be otherwise, since  $i_R$  is the time rate of change of the product of  $v_R$  and the diode’s capacitance. To repeat the equation that expresses this concept:

$$i_R = \frac{d(Cv_R)}{dt}$$

**In region 5**, the switch is on and the diode has completed its reverse recovery. Region 4 ends and region 5 begins when  $i_R$  goes to zero (actually it goes to the leakage level) and when  $v_R$  has reached the level of the applied voltage. This is the same time at which the switch is fully on. When the switch is on, the diode is reverse biased and is not conducting. Therefore, when the switch is on, the switch current equals the inductor cur-

rent. This relationship is depicted in the graphic showing the currents in region 5 as arrows.  $i_R$  is not shown because it is zero (neglecting leakage).



In the preceding discussion of the five regions, the subcircuits of Figures 1 and 2 have been in view. A discussion of diode  $dv/dt$  as it relates to these subcircuits follows. Sentences in bold typeface bring out the highpoints.

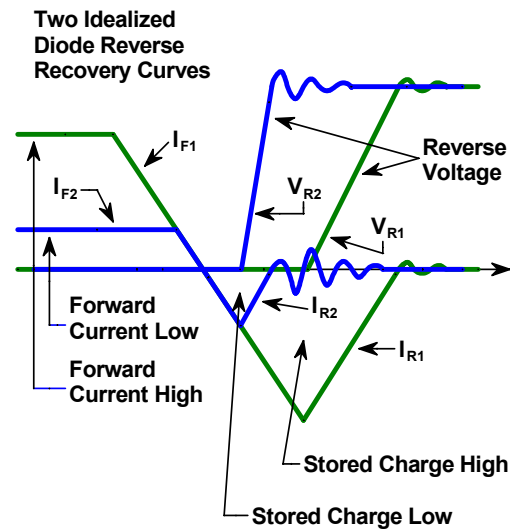


Figure 4. Two Idealized Diode Reverse Recovery Curves

**For a given set of drive conditions,  $dv_R/dt$  for the diode will be higher on turn-off when there is less stored charge in the diode, and detrimental ringing may occur.** Figure 4 illustrates this principle. Once the diode’s reverse voltage begins to rise, the rate at which it builds depends on the amount of stored charge left in the diode. In order for the diode to withstand

reverse voltage, stored charge must be swept out and the depletion region at the  $p-n$  junction must widen. The rate at which this takes place is represented by the time derivative of the reverse current,  $di_R/dt$ . Some diodes snap off (high  $di_R/dt$ ) and some diodes follow a softer trajectory (lower  $di_R/dt$ ).

These differences are not shown in Figure 4 and do not change what is shown, since the figure depicts two conditions for the same diode, not two different diodes. Accordingly, the reverse voltage will rise faster or slower depending on the amount of stored charge in the diode, regardless of whether the diode is characterized by a snappy or a soft recovery. The reverse voltage on the diode increases as the stored charge is removed and as the depletion layer expands in response to the applied voltage. The limit in this process is the diode's own breakdown voltage. If the breakdown voltage is exceeded, the diode will go into avalanche, a condition to be avoided. The reverse voltage settles at the level of the applied voltage. There is more or less ringing as it settles, depending on the amount of stray inductance in the circuit and on the availability of current from the switch. If the ringing has too much amplitude and energy, the diode can be destroyed. If there is a switch in parallel with the diode, it too can be damaged. If the circuit had absolutely no stray inductance, there would be no ringing. Regardless of whether a diode snaps off or has a softer recovery, the voltage is able to build faster in a diode that has less stored charge, because it doesn't take as long to remove fewer charges. Therefore, the voltage will be able to rise fastest on a diode that has no stored charge, although not instantly, since the depletion region still has to be widened. Figure 4 also indicates that the ringing in the circuit is worse for the higher  $dv/dt$  case, i.e., the case of lower stored charge in the same diode. All cases of ringing are not shown in Figure 4. The ringing can be a lot or a little depending on the layout and the configuration of the gate drive. For the purposes of this discussion it is enough to know what is depicted in Figure 4.

**There is less stored charge in the diode when the forward current (equal to the inductor**

**current) is low.** Again this is illustrated by Figure 4. Remember that this is based on the case in which the drive conditions are the same, as would be true in a circuit where the current in the inductor varies in response to the load. As the load becomes low and the current in the inductor becomes low, the forward current in the diode becomes low, as well. In turn, the stored charge in the diode becomes low and the  $dv_R/dt$  becomes high. Again, this is all in the same diode. Snappy diodes will have higher  $dv_R/dt$  than soft recovery diodes by virtue of their shorter minority carrier lifetimes and the way they are distributed through the material. Even so, the snappy diode will still follow the pattern of Figure 4: when the snappy diode has less stored charge (a low forward current case), its  $dv_R/dt$  will be higher, and when its stored charge is more (a higher forward current case), its  $dv_R/dt$  will be lower than in its own lower stored charge case. This discussion is not about which diode is in the circuit, but rather, given whatever diode is in the circuit, how does  $dv_R/dt$  work? It works as shown in Figure 4.

**Therefore, the lowest-current (no-load or low-load) case is the worst case for  $dv/dt$  failures.** When the inductor current is the lowest, the stored charge is the least, and the  $dv_R/dt$  is the greatest. This fact leads to the need to optimize the gate drive for the lowest-current case. It is the designer's responsibility to identify the lowest current case for the design. Adjusting for zero-current when the lowest current is non-zero would not be optimal. It would result in drive current smaller than it needs to be and losses greater than they need to be.

**Optimize the drive by reducing the gate current until the ringing is tolerable.** For typical gate drive systems utilizing square voltage pulses to drive the gate, reducing the gate current is done by increasing the gate resistance. Backing off on the gate current reduces the  $dv_R/dt$  with the result that the ringing is also reduced. Figure 5 illustrates the effect of reducing the drive current:  $dv_R/dt$  is reduced, and ringing is reduced. The arrows going through the curves

are pointing in the direction of decreasing drive current. The other result is that turn-on and turn-off times for the switch are increased. This in turn increases switching losses. Optimization effects a proper tradeoff between the ringing and the losses. In other words an amount of ringing that is not harmful may have to be tolerated in order to keep losses as low as possible.

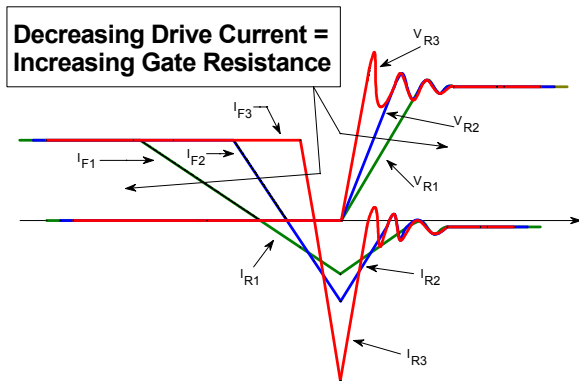


Figure 5. Reverse Recovery Curves for Different Drive Currents

Keeping ringing within safe limits, the gate drive must be adjusted to minimize the losses. Of course, in some circuits, minimizing EMI must be part of the optimization, as well.

**If you optimize the gate drive for the full-load case (not the worst case), you may break devices in the lowest-load case.** Suppose the gate drive is optimized in the manner described above for the full-load case. The diode current and reverse voltage would be like the curves labelled “1” in Figure 4. The lowest-load case would have curves like the ones labelled “2” in Figure 4. Consequently,  $dv_{R2}/dt$ , which is greater than  $dv_{R1}/dt$ , may be high enough to incite sufficient ringing to bring the diode to failure through avalanche that has too much energy. On the other hand, if the gate drive is optimized for the lowest-load case ( $dv_{R2}/dt$ ), then the other cases will not bring about failure, since  $dv_R/dt$  in those cases is lower than  $dv_{R2}/dt$ .

**Optimize the gate drive for the lowest-current case.** The amount of ringing, including the energy in the ringing, depends on the circuit layout, the choice of diode, and on the gate drive configura-

tion. One important goal in layout is to minimize inductive loops to the end that ringing is reduced as much as possible. In some cases the layout is so good that, for the given application, the ringing is very benign. In other cases, it may be necessary to replace a snappy diode with a softer recovery diode, thus also reducing the ringing. Once the layout is finalized, the gate drive must be optimized to bring the ringing within acceptable limits and to minimize the losses, if layout and diode selection have not already done so. Optimizing the gate drive for the worst case, the lowest-current case, should eliminate failures due to  $dv/dt$  in the subcircuits of Figures 1 and 2.