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Power MOSFET Tutorial

Jonathan Dodge, P.E.
Applications Engineering Manager
Advanced Power Technology
405 S.W. Columbia Street
Bend, OR 97702

Introduction

Power MOSFETs are well known for superior switching speed, and they require very little gate drive power because of the insulated gate. In these respects, power MOSFETs approach the characteristics of an "ideal switch". The main drawback is on-resistance $R_{DS(on)}$ and its strong positive temperature coefficient. This application note explains these and other main features of high voltage N-channel power MOSFETs, and provides useful information for device selection and application. Advanced Power Technology MOSFET datasheet information is also explained.

Power MOSFET Structure

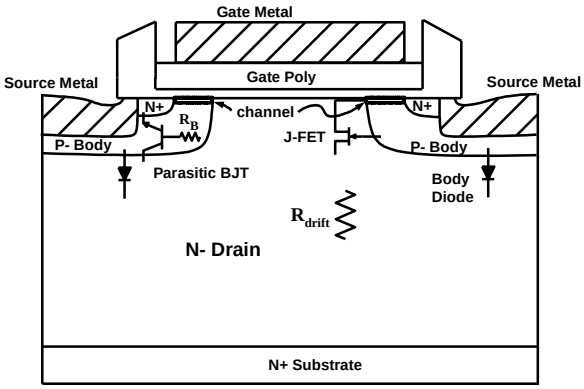

Figure 1 N-Channel MOSFET Cross Section

Figure 1 shows a cross section of an APT N-channel power MOSFET structure. (Only N-channel MOSFETs are discussed here.) A positive voltage applied from the source to gate terminals causes electrons to be drawn toward the gate terminal in the body region. If the gate-source voltage is at or above what is called the threshold voltage, enough electrons accumulate under the gate to cause an inversion n-type layer; forming a conductive channel across the body region (the MOSFET is enhanced). Electrons can flow in either direction through the channel. Positive (or forward) drain current flows into the drain as electrons move from the source toward the drain. Forward drain current is blocked once the channel is turned off, and drain-source voltage is supported by the reverse biased body-drain p-n junction.

In N-channel MOSFETs, only electrons flow during forward conduction – there are no minority carriers. Switching speed is only limited by the rate that charge is supplied to or removed from capacitances in the MOSFET. Therefore switching can be very fast, resulting in low switching losses. This is what makes power MOSFETs so efficient at high switching frequency.

$R_{DS(on)}$

The main components of on resistance $R_{DS(on)}$ include the channel, JFET (accumulation layer), drift region, and parasitics (metallization, bond wires, and package). At voltage ratings above about 150V, drift region resistance dominates $R_{DS(on)}$.

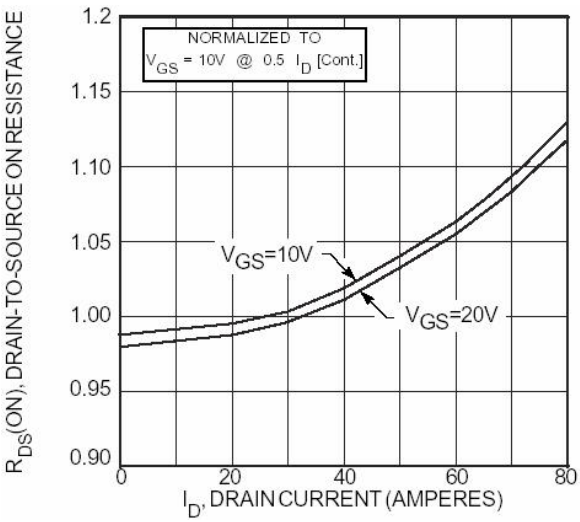

Figure 2 $R_{DS(on)}$ vs. Current, APT50M75B2LL

The effect of current on $R_{DS(on)}$ is relatively weak in high voltage MOSFETs . Looking at Figure 2, doubling the current results in only about a 6% increase in $R_{DS(on)}$.

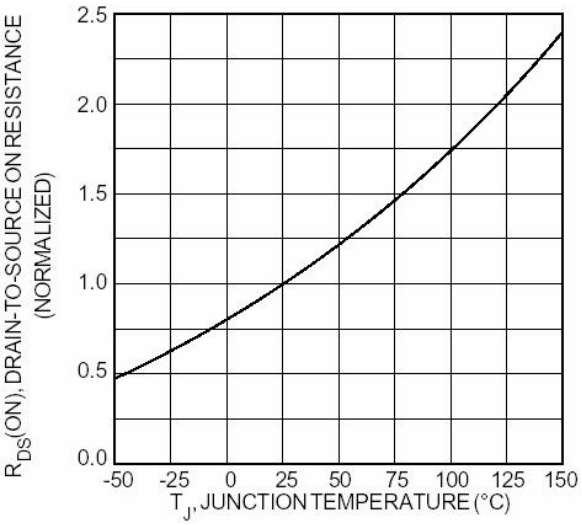

Figure 3 $R_{DS(on)}$ vs. Temperature, APT50M75B2LL

Temperature on the other hand has a strong effect on $R_{DS(on)}$. As seen in Figure 3, on resistance approximately doubles from 25ºC to 125ºC. The temperature coefficient of $R_{DS(on)}$ is the slope of the curve in Figure 3 and is always positive because of majority-only carriers. The strong positive $R_{DS(on)}$ temperature coefficient compounds the $I^2 \cdot R$ conduction loss as temperature increases.

The positive $R_{DS(on)}$ temperature coefficient is a nice feature when paralleling power MOSFETs because it ensures thermal stability. It *does not* however ensure even current sharing. This is a common misconception [1]. What really makes MOSFETs so easy to parallel is their relatively narrow part-to-part parameter distribution, particularly $R_{DS(on)}$, combined with the security from current hogging provided by the positive $R_{DS(on)}$ temperature coefficient.

For any given die size, $R_{DS(on)}$ also increases with increasing voltage rating $V_{(BR)DSS}$, as shown Figure 4.

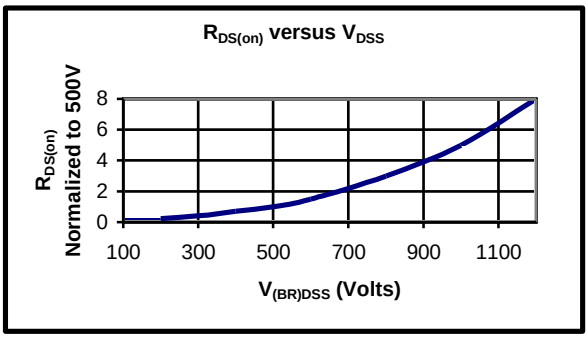

Figure 4 Normalized $R_{DS(on)}$ vs. $V_{(BR)DSS}$

A curve fit of rated $R_{DS(on)}$ versus $V_{(BR)DSS}$ for Power MOS V® and Power MOS 7® MOSFETs reveals that $R_{DS(on)}$ increases as the square of $V_{(BR)DSS}$. This non-linear relationship between $R_{DS(on)}$ and $V_{(BR)DSS}$ is a compelling reason to research ways to reduce the conduction loss of power transistors [2].

Intrinsic and Parasitic Elements

JFET

Within the structure of a MOSFET, you can imagine an integral JFET shown in Figure 1. This JFET has a significant influence on $R_{DS(on)}$ and is part of the normal operation of the MOSFET.

Intrinsic Body Diode

The body-drain p-n junction forms an intrinsic diode called the body diode (see Figure 1). Reverse drain current cannot be blocked because the body is shorted to the source, providing a high current path through the body diode. Enhancing the device reduces conduction loss when reverse drain current flows because electrons flow through the channel in addition to electrons and minority carriers flowing through the body diode.

The intrinsic body diode is convenient in circuits that require a path for reverse drain current (often called freewheeling current), such as bridge circuits. For these circuits, FREDFETs are offered with improved reverse recovery characteristics. FREDFET is simply a trade name Advanced Power Technology uses to distinguish a MOSFET that has additional processing steps to speed up the reverse recovery of the intrinsic body diode. There is no separate diode in a FREDFET; it is the MOSFET intrinsic body diode. Either electron irradiation (which is usually used) or platinum doping is used for minority carrier lifetime control in the body diode, greatly reducing the reverse recovery charge and time.

A side effect of FREDFET processing is higher leakage current, particularly at high temperature. However, considering that MOSFETs have low leakage current to begin with, the added leakage current of a FREDFET is normally of no concern below 150°C junction temperature. Depending on the irradiation dose, a FREDFET may have a higher $R_{DS(on)}$ rating than a corresponding MOSFET. The body diode forward voltage is also slightly higher for a FREDFET. Gate charge and switching speed are identical between MOSFETs and FREDFETs. From here on, the term MOSFET will be used for both MOSFETs and FREDFETs unless specifically stated otherwise.

The reverse recovery performance of a MOSFET or even of a FREDFET is "crummy" compared to a discrete fast recovery diode. In a hard switched application operating at 125°C, the turn-on loss in the switch due to the reverse recovery current of the body diode is about five times higher than if a discrete fast recovery diode is used. There are two reasons for this:

1. The area of the body diode is the same as the area of the MOSFET or FREDFET, whereas the area of a discrete diode for the same function can be much smaller and hence have much lower recovery charge.
2. The body diode of a MOSFET or even a FREDFET is not optimized for reverse recovery like a discrete diode is.

Like any conventional silicon diode, body diode reverse recovery charge and time depend on temperature, di/dt, and current. The forward voltage of the body diode, V_{SD}, decreases with temperature by about 2.5 mV/°C.

Parasitic Bipolar Transistor

The layered MOSFET structure also forms a parasitic NPN bipolar junction transistor (BJT), and turning it on is definitely not part of normal operation. If the BJT were to turn on and saturate, it would result in a condition called latchup, where the MOSFET cannot be turned off except by externally interrupting the drain current. High power dissipation during latchup can destroy the device.

The base of the parasitic BJT is shorted to the source to prevent latchup and because breakdown voltage would be greatly reduced (for the same $R_{DS(on)}$) if the base were allowed to float. It is theoretically possible for extremely high dv/dt during turn-off to cause latchup. For modern, conventional power MOSFETs however, it is very difficult to build a circuit capable of achieving such high dv/dt.

There is a risk of turning on the parasitic BJT if the body diode conducts and then commutates off with excessively high dv/dt. High commutation dv/dt causes high current density of minority carriers (positive carriers, or holes) in the body region, which can build up enough voltage across the body resistance to turn on the parasitic BJT. This is the reason for the peak commutating (body diode recovery) dv/dt limit in the datasheet. Peak commutating dv/dt is higher for a FREDFET compared to a MOSFET because of reduced minority carrier lifetime.

Temperature Effects

Switching Speed

Switching speed and loss are practically unaffected by temperature because the capacitances are unaffected by temperature. Reverse recovery current in a diode however increases with temperature, so temperature effects of an external diode (be it a discrete diode or a MOSFET or FREDFET body diode) in the power circuit affect turn-on switching loss.

Threshold Voltage

The threshold voltage, denoted as $V_{GS(th)}$, is really a turn-off specification. It tells how many milliamps of drain current will flow at the threshold voltage, so the device is basically off but on the verge of turning on. The threshold voltage has a negative temperature coefficient, meaning the threshold voltage decreases with increasing temperature. This temperature coefficient affects turn-on and turn-off delay times and hence the dead-time requirement in a bridge circuit.

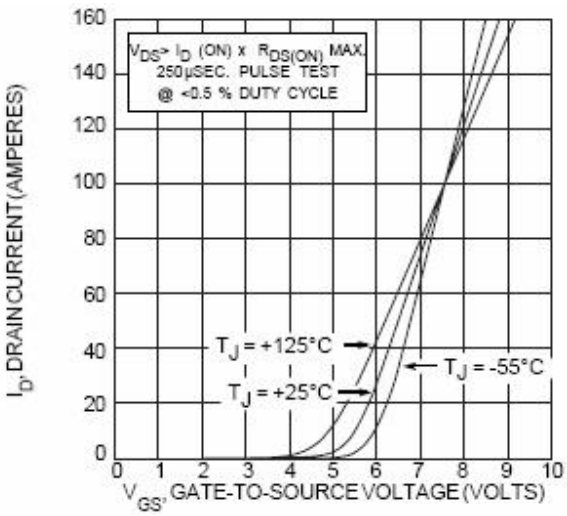

Figure 5 Transfer Characteristic, APT50M75B2LL

Transfer Characteristic

Figure 5 shows the transfer characteristic for an APT50M75B2LL MOSFET. The transfer characteristic depends on both temperature and drain current. In Figure 5, below 100 Amps the gate-source voltage has a negative temperature coefficient (less gate-source voltage at higher temperature for a given drain current). Above 100 Amps, the temperature coefficient is positive. The gate-source voltage temperature coefficient and the drain current at which it crosses over from negative to positive are important for linear mode operation [3].

Breakdown Voltage

Breakdown voltage has a positive temperature coefficient, as will be discussed in the Datasheet Walkthrough section.

Short Circuit Capability

Short circuit withstand capability is not typically listed in the datasheet. This is simply because conventional power MOSFETs are unmatched for short circuit withstand capability compared to IGBTs or other devices with higher current density. It goes without saying that MOSFETs and FREDFETs are short circuit capable.

Datasheet Walkthrough

The intent of datasheets provided by APT is to include relevant information that is useful and convenient for selecting the appropriate device as well as predicting its performance in an application. Graphs are provided that can be used to extrapolate from one set of operating conditions to another. It should be noted that the graphs represent typical performance, not minimums nor maximums. Performance also depends somewhat on the circuit; different test circuits yield slightly different results.

Maximum Ratings

V_{DSS} – Drain-Source Voltage

This is a rating of the maximum drain-source voltage without causing avalanche breakdown, with the gate shorted to the source and the device at 25°C. Depending on temperature, the avalanche breakdown voltage could actually be less than the V_{DSS} rating. See the description of $V_{(BR)DSS}$ in Static Electrical Characteristics.

V_{GS} – Gate-Source Voltage

V_{GS} is a rating of the maximum voltage between the gate and source terminals. The purpose of this rating is to prevent damage of the gate oxide. The actual gate oxide withstand voltage is typically much higher than this but varies due to manufacturing processes, so staying within this rating ensures application reliability.

I_D – Continuous Drain Current

I_D is a rating of the maximum continuous DC current with the die at its maximum rated junction temperature $T_{J(max)}$ and the case at 25°C and sometimes also at a higher temperature. It is based on the junction-to-case thermal resistance rating $R_{\theta JC}$ and the case temperature T_C as follows:

$$P_D = \frac{T_{J(max)} - T_C}{R_{\theta JC}} = I_D^2 \cdot R_{DS(on)@T_{J(max)}} \qquad (1)$$

This equation simply says that the maximum heat that can be dissipated, $\frac{T_{J(max)} - T_C}{R_{\theta JC}}$, equals the maximum allowable heat generated by conduction loss, $I_D^2 \cdot R_{DS(on)@T_{J(max)}}$, where $R_{DS(on)@T_{J(max)}}$ is the on resistance at the maximum junction temperature. Solving for I_D:

$$I_D = \sqrt{\frac{T_{J(max)} - T_C}{R_{\theta JC}} \cdot \frac{1}{R_{DS(on)@T_{J(max)}}}} \qquad (2)$$

Note that there are no switching losses involved in I_D, and holding the case at 25°C is seldom feasible in practice. Because of this, actual switched current is typically less than half of the I_D @ T_C = 25°C rating in a hard switched application; one fourth to one third is common.

Graph of I_D versus T_C

This graph is simply the solution to (2) over a range of case temperatures. Switching losses are not included. Figure 6 shows an example. Note that in some cases, the package leads limit the continuous current (switched current can be higher): 100 Amps for TO-247 and TO-264 packages, 75 Amps for TO-220 package, and 220 Amps for the SOT-227 package.

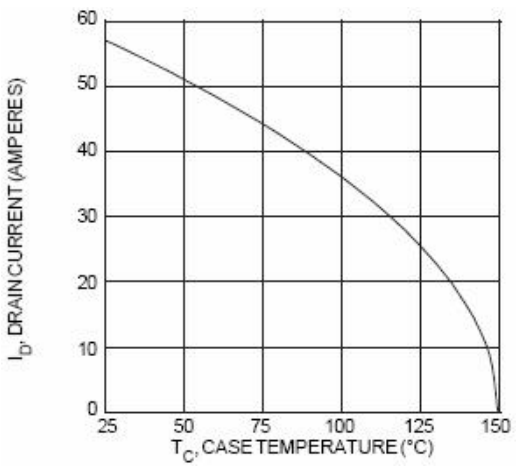

Figure 6 Maximum Drain Current vs. Case Temperature, APT50M75B2LL

I_{DM} – Pulsed Drain Current

This rating indicates how much pulsed current the device can handle, which is significantly higher than the rated continuous DC current. The purposes of the I_{DM} rating are:

- To keep the MOSFET operating in the Ohmic region of its output characteristic. See Figure 7. There is a maximum drain current for a corresponding gate-source voltage that a MOSFET will conduct. If the operating point at a given gate-source voltage goes above the Ohmic region "knee" in Figure 7, any further increase in drain current results in a significant rise in drain-source voltage (linear mode operation) and a consequent rise in conduction loss. If power dissipation is too high for too long the device may fail. The I_{DM} rating is set below the "knee" for typical gate drive voltages.
- A current density limit to prevent die heating that otherwise could result in a burnout site.
- To avoid problems with excessive current through the bond wires in case the bond wires are the "weak link" instead of the die.

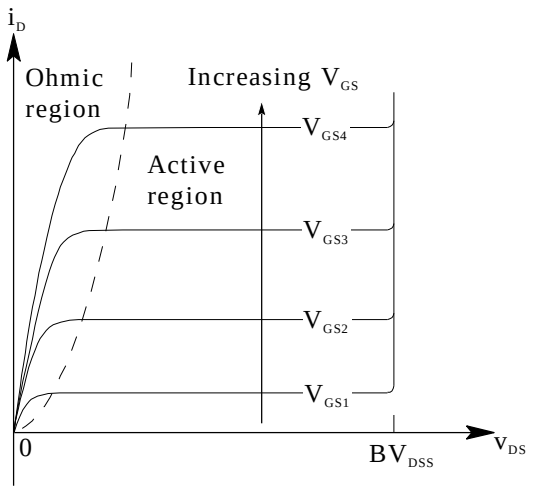

Figure 7 MOSFET Output Characteristic

Regarding the thermal limitation on I_{DM}, temperature rise depends upon the pulse width, time between pulses, heat dissipation, and $R_{DS(on)}$ as well as the shape and magnitude of the current pulse. Simply staying within the I_{DM} limit does not ensure that the maximum junction temperature will not be exceeded. See the discussion on transient thermal impedance under Thermal and Mechanical Characteristics for a way to estimate junction temperature during a current pulse.

P_D – Total Power Dissipation

This is a rating of the maximum power that the device can dissipate and is based on the maximum junction temperature and the thermal resistance $R_{\theta JC}$ at a case temperature of 25ºC.

$$P_D = \frac{T_{J(max)} - T_C}{R_{\theta JC}} \qquad (3)$$

The linear derating factor is simply the inverse of $R_{\theta JC}$.

T_J, T_{STG} – Operating and Storage Junction Temperature Range

This is the range of permissible storage and operating junction temperatures. The limits of this range are set to ensure a minimum acceptable device service life. Operating well within the limits of this range can significantly enhance the service life.

E_{AS} – Single Pulse Avalanche Energy

If a voltage overshoot (typically due to leakage and stray inductances) does not exceed the breakdown voltage, then the device will not avalanche and hence does not need to dissipate avalanche energy. Avalanche energy rated devices offer a safety net for over-voltage transients, depending on the amount of energy dissipated in avalanche mode.

All devices that are avalanche energy rated have an E_{AS} rating. Avalanche energy rated is synonymous with unclamped inductive switching (UIS) rated. E_{AS} indicates how much reverse avalanche energy the device can safely absorb.

Conditions for a test circuit are stated in a footnote, and the E_{AS} rating is equal to $\frac{L \cdot i_D^2}{2}$, where L is the value of an inductor carrying a peak current i_D, which is suddenly diverted into the drain of the device under test. It is the inductor voltage exceeding the breakdown voltage of the MOSFET that causes the avalanche condition. An avalanche condition allows the inductor current to flow through the MOSFET, even though the MOSFET is in the off state. Energy stored in the inductor is analogous to energy stored in leakage and/or stray inductances and is dissipated in the MOSFET.

When MOSFETs are paralleled, it is highly unlikely that they have exactly the same breakdown voltage. Typically, one device will avalanche first and subsequently take all the avalanche current (energy).

E_{AR} – Repetitive Avalanche Energy

A repetitive avalanche rating has become "industry standard" but is meaningless without information about the frequency, other losses, and the amount of cooling. Heat dissipation (cooling) often limits the repetitive avalanche energy. It is also difficult to predict how much energy is in an avalanche event. What the E_{AR} rating really says is that the device can withstand repetitive avalanche without any frequency limitation, provided the device is not overheated, which is true of any avalanche capable device. During design qualification, it is good practice to measure the device or heat sink temperature during operation to see that the MOSFET does not overheat, especially if avalanching is possible.

I_{AR} – Avalanche Current

For some devices, the propensity for current crowding in the die during avalanche mandates a limit in avalanche current I_{AR}. Thus avalanche current is the "fine print" of avalanche energy specifications; it reveals the true capability of a device.

Static Electrical Characteristics

$V_{(BR)DSS}$ – Drain-Source Breakdown Voltage

$V_{(BR)DSS}$ (sometimes called BV_{DSS}) is the drain-source voltage at which no more than the specified drain current will flow at the specified temperature and with zero gate-source voltage. This tracks the actual avalanche breakdown voltage.

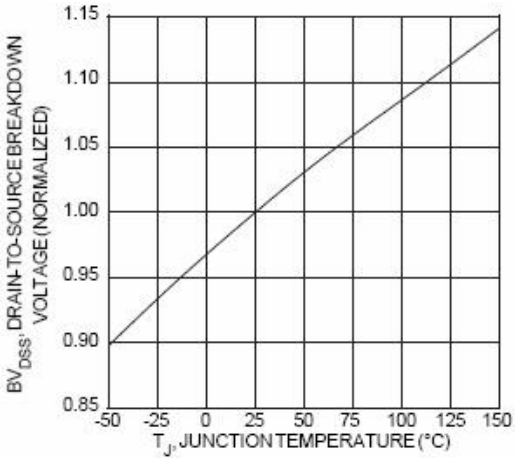

Figure 8 Normalized Breakdown Voltage versus Temperature, APT50M75B2LL

As shown in Figure 8, $V_{(BR)DSS}$ has a positive temperature coefficient. A MOSFET can block more voltage when hot than when cold. In fact, when cold, $V_{(BR)DSS}$ is less than the maximum V_{DSS} rating, which is specified at 25°C. For the example shown in Figure 8, at -50ºC, $V_{(BR)DSS}$ is about 90% of the 25ºC maximum V_{DSS} rating.

$V_{GS(th)}$ – Gate Threshold Voltage

This is the gate-source voltage at which drain current begins to flow, or stops flowing when switching off the MOSFET. Test conditions (drain current, drain-source voltage, and junction temperature) are also specified. All MOS gated devices exhibit variation in threshold voltage between devices, which is normal. Therefore, a range in $V_{GS(th)}$ is specified, with the minimum and maximum representing the edges of the $V_{GS(th)}$ distribution. As discussed previously under Temperature Effects, $V_{GS(th)}$ has a negative temperature coefficient, meaning that as the die heats up, the MOSFET will turn on at a lower gate-source voltage.

$R_{DS(on)}$ – On Resistance

This is the drain-source resistance at a specified drain current (usually half the I_D current) and gate-source voltage (usually 10 Volts), and at 25°C unless otherwise specified.

I_{DSS} – Zero Gate Voltage Drain Current

This is the drain-source leakage current at a specified drain-source voltage when the gate-source voltage is zero. Since leakage current increases with temperature, I_{DSS} is specified both at room temperature and hot. Leakage power loss is I_{DSS} times drain-source voltage and is usually negligible.

I_{GSS} – Gate-Source Leakage Current

This is the leakage current that flows through the gate terminal at a specified gate-source voltage.

Dynamic Characteristics

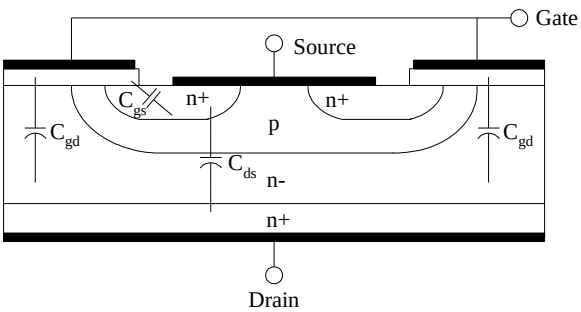

Figure 9 Power MOSFET Structure Capacitances

Figure 9 shows the locations of power MOSFET intrinsic capacitances. The values of the capacitances are determined by the structure of the MOSFET, the materials involved, and by the voltages across them. These capacitances are independent of temperature, so MOSFET switching speed is also insensitive to temperature (except for a minor effect related to the threshold voltage changing with temperature).

Capacitances C_{gs} and C_{gd}, vary with the voltage across them because they are affected by depletion layers within the device [4]. However, C_{gs} has only a small voltage change across it compared to C_{gd} and consequently a small capacitance change. The change in C_{gd} with drain-to-gate voltage can be as much as a factor of 100 or more.

Figure 10 shows the intrinsic capacitances from a circuit perspective. The gate-to-drain and gate-to-source capacitances impact the susceptibility of unwanted dv/dt induced turn-on in bridge circuits.

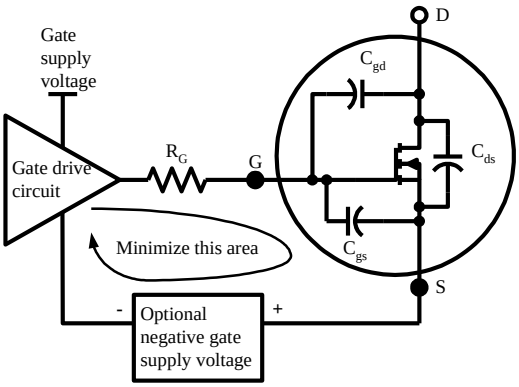

Figure 10 Power MOSFET Intrinsic Capacitances

In a nutshell, the smaller C_{gd} is the less susceptibility there is for dv/dt induced turn-on. Also, C_{gs} and C_{gd} form a capacitive voltage divider, and a large ratio of C_{gs} to C_{gd} is desirable for dv/dt immunity. This ratio multiplied by the threshold voltage is a figure of merit for dv/dt turn-on immunity, and APT power MOSFETs lead the industry with this and other figures of merit.

C_{iss} – Input Capacitance

This is the input capacitance measured between the gate and source terminals with the drain shorted to the source for AC signals. C_{iss} is made up of the gate to drain capacitance C_{gd} in parallel with the gate to source capacitance C_{gs}, or

$$C_{iss} = C_{gs} + C_{gd}$$

The input capacitance must be charged to the threshold voltage before the device begins to turn on, and discharged to the plateau voltage before the device turns off. Therefore, the impedance of the drive circuitry and C_{iss} have a direct effect on the turn on and turn off delays.

C_{oss} – Output Capacitance

This is the output capacitance measured between the drain and source terminals with the gate shorted to the source for AC voltages. C_{oss} is made up of the drain to source capacitance C_{ds} in parallel with the gate to drain capacitance C_{gd}, or

$$C_{oss} = C_{ds} + C_{gd}$$

For soft switching applications, C_{oss} is important because it can affect the resonance of the circuit.

C_{rss} – Reverse Transfer Capacitance

This is the reverse transfer capacitance measured between the drain and gate terminals with the source connected to ground. The reverse transfer capacitance is equal to the gate to drain capacitance.

$$C_{res} = C_{gd}$$

The reverse transfer capacitance, often referred to as the Miller capacitance, is one of the major parameters affecting voltage rise and fall times during switching. It also effects the turn-off delay time.

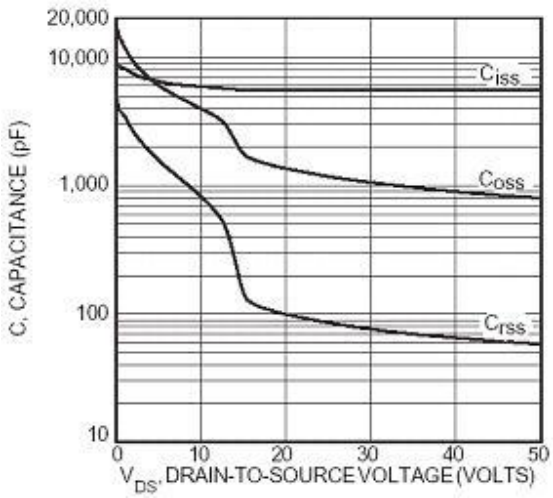

Figure 11 Capacitance vs Voltage, APT50M75B2LL

Figure 11 shows an example graph of typical capacitance values versus drain-source voltage. The

capacitances decrease over a range of increasing drain-source voltage, especially the output and reverse transfer capacitances.

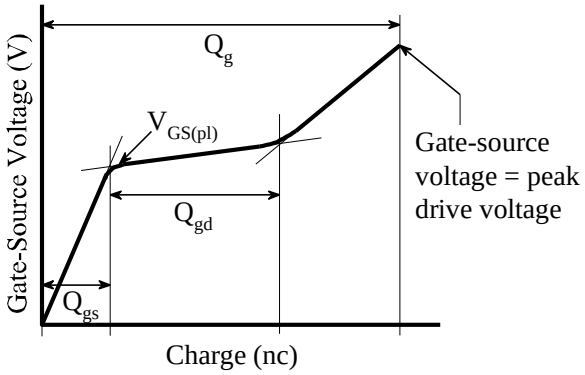

Figure 12 v_{GS} as a Function of Gate Charge

Q_{gs}, Q_{gd}, and Q_g – Gate Charge

Gate charge values reflect charge stored on the inter-terminal capacitances described earlier. Gate charge is often used for designing gate drive circuitry since it takes into account the changes in capacitance with changes in voltage during a switching transient [5, 6].

Referring to Figure 12, Q_{gs} is the charge from the origin to the first inflection in the curve, Q_{gd} is the charge from the first to second inflection in the curve (also known as the "Miller" charge), and Q_g is the charge from the origin to the point on the curve at which v_{GS} equals a specified gate drive voltage.

Gate charge values vary slightly with drain current and drain-source voltage but not with temperature. Test conditions are specified. A graph of gate charge is typically included in the datasheet showing gate charge curves for a fixed drain current and different drain-source voltages. The plateau voltage $V_{GS(pl)}$ shown in Figure 12 increases slightly with increasing current (and decreases with decreasing current). The plateau voltage is also directly proportional to the threshold voltage, so variation in threshold voltage correlates to variation in the plateau voltage.

Resistive Switching Times

For purely historical reasons, resistive switching data is included in MOSFET datasheets.

$t_{d(on)}$, – Turn-on Delay Time

Turn-on delay time is the time from when the gate-source voltage rises past 10% of the gate drive voltage to when the drain current rises past 10% of the specified current.

$t_{d(off)}$, – Turn-off Delay Time

Turn-off delay time is the time from when the gate-source voltage drops below 90% of the gate drive voltage to when the drain current drops below 90% of the specified current. This gives an indication of the delay before current begins to transition in the load.

t_r – Rise Time

Rise time is the time between the drain current rising from 10% to 90%, start to stop of the specified current.

t_f – Fall Time

Fall time is the time between the drain current falling from 90% to 10%, start to stop of the specified current.

Inductive Switching Energies

Because resistive switching data is so difficult to use for predicting switching losses in a real power converter, Advanced Power Technology includes inductive switching energy data in many MOSFET and FREDFET datasheets. This makes it convenient for a power supply designer to directly compare the performance of a MOSFET or FREDFET with another transistor, even one of a different technology such as an IGBT, and to successfully utilize the most appropriate power transistor.

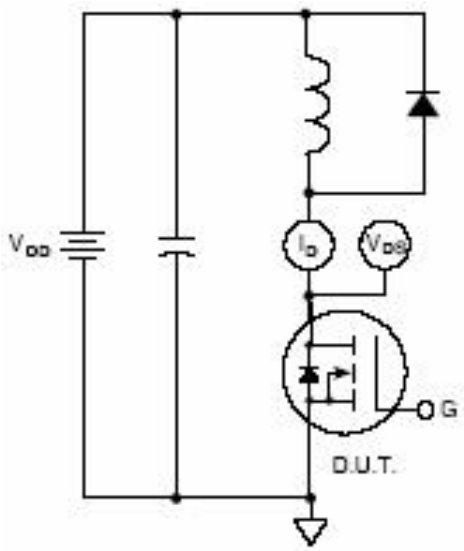

Figure 13 Inductive Switching Loss Test Circuit

Figure 13 shows the inductive switching test circuit schematic. It is a pulsed test with very low duty cycle such that the energy in the inductor collapses long before the next set of pulses, and self heating can be ignored. The temperature of the device under test

(DUT) and the clamp diode are regulated by a temperature forcing system.

The following test conditions are specified in the Dynamic Characteristics table: V_{DD} in Figure 13, test current, gate drive voltage, gate resistance, and junction temperature. Note that the gate resistance may include the resistance of the gate driver IC. Since switching times and energies vary with temperature, mostly because of the diode in the test circuit, data is provided both at room temperature and hot, with the diode heated along with the DUT. Graphs are also provided showing the relationships between switching times and energies to drain current and gate resistance. Delay time and current rise and fall time definitions are the same as for resistive switching.

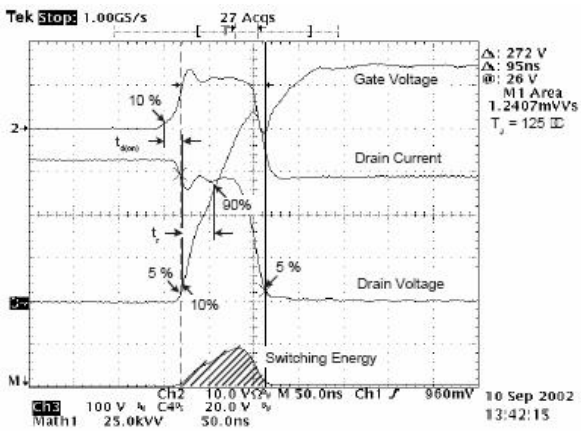

Figure 14 Turn-on Waveforms and Definitions

Actual switching waveforms are used in the datasheet to define the various measured parameters. Figure 14 shows turn-on waveforms and definitions.

Switching energy can be scaled directly for variation between application voltage and the datasheet switching energy test voltage. So if the datasheet tests were done at 330 Volts for example, and the application is at 400 Volts, simply multiply the datasheet switching energy values by the ratio 400/330 to scale.

Switching times and energies vary strongly with other components and stray inductances in the circuit. The diode has a particularly strong effect on turn-on energy. Stray inductance in series with the source that is part of the gate drive return significantly affects switching times and energies. Therefore, switching time and energy values and graphs in the datasheet are representative only and may vary from observed results in an actual power supply or motor drive circuit.

E_{on} – Turn-on Switching Energy with Diode

This is the clamped inductive turn-on energy that includes a commutating diode reverse recovery current in the DUT turn-on switching loss. Note that FREDFETs in a hard switched bridge circuit where the body diode is hard commutated off have about 5 times higher turn-on energy than if a discrete fast recovery diode is used, like in the test circuit of Figure 13.

Turn-on switching energy is the integral of the product of drain current and drain-source voltage over the interval from when the drain current rises past 5% or 10% of the test current to when the voltage falls below 5% of the test voltage. The 5% to 10% of current rise to 5% of voltage fall definitions for the integration interval in the waveforms in Figure 14 accommodate the resolution of the instrumentation while providing a reliable means of duplicating the measurement that does not compromise accuracy.

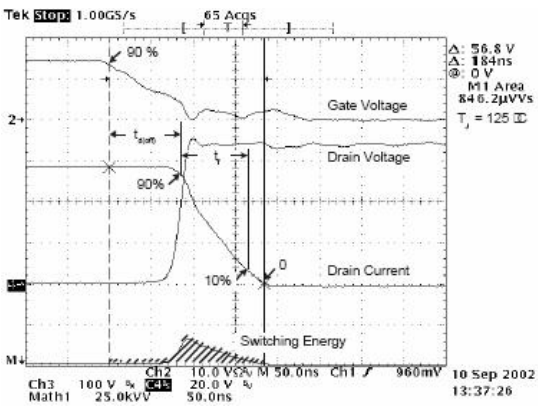

Figure 15 Turn-off Waveforms and Definitions

E_{off} – Turn-off Switching Energy

This is the clamped inductive turn-off energy. Figure 13 shows the test circuit and Figure 15 shows the waveforms and definitions. E_{off} is the integral of the product of drain current and drain-source voltage over the interval starting from when the gate-source voltage drops below 90% to when the drain current reaches zero. This is in accordance with JEDEC standard 24-1 for measuring turn-off energy.

Thermal, Mechanical Characteristics

$R_{\theta JC}$ – Junction to Case Thermal Resistance

This is the thermal resistance from the junction of the die to the outside of the device case. Heat is the result of power lost in the device itself, and thermal resistance relates how hot the die gets relative to the

case based on this power loss. Note that tests at APT revealed the plastic temperature to be the same as the metal portion of the case for discrete parts.

The maximum $R_{\theta JC}$ value incorporates margin to account for normal manufacturing variation. Due to manufacturing process improvements, the industry trend is toward decreasing the margin between the maximum $R_{\theta JC}$ value and the typical value. The amount of margin is usually not published.

$Z_{\theta JC}$ – Junction to Case Transient Thermal Impedance

Transient thermal impedance takes into account the heat capacity of the device, so it can be used to estimate instantaneous temperatures resulting from power loss on a transient basis.

Thermal impedance test equipment applies power pulses of varying duration to the DUT, waiting for the junction temperature to settle back down between each pulse. This measures the 'single pulse' transient thermal impedance response. From this, a curve fit is used to create a resistor-capacitor (RC) model. Figure 16 shows such a transient thermal impedance RC model. Some datasheets may show the capacitors and resistors in parallel, but this is an error. The capacitors are "grounded" as shown in Figure 16, and the component values remain the same. There is no physical significance to the intermediate nodes in the model. Various numbers of resistor-capacitor pairs are used simply to create a good fit to actual measured thermal impedance data.

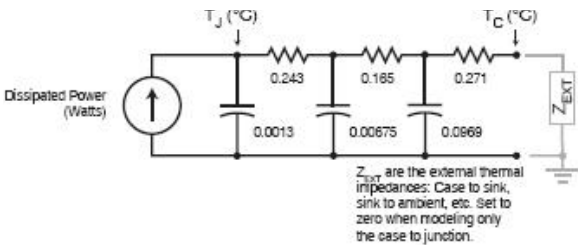

Figure 16 Transient Thermal Impedance RC Model

To simulate temperature rise with the RC model, you apply a current source whose magnitude is the power being dissipated in the MOSFET. Thus you can use PSPICE or other electronic simulator to apply an arbitrary power loss input. From this, you can estimate the junction-to-case temperature rise as the voltage across the ladder by setting Z_{EXT} to zero (a short), as shown in Figure 16. You can extend the model to include a heat sink by adding additional capacitors and/or resistors.

The transient thermal impedance "family of curves" that is published in the datasheet is simply a rectangular pulse simulation based on the RC thermal impedance model. Figure 17 shows an example. You can use the 'family of curves' to estimate peak temperature rise for rectangular power pulses, which is common in a power supply. However, because the minimum pulse width is 10 µs, the graph is only relevant for switching frequencies less than 100 kHz. At higher frequency you simply use the thermal resistance $R_{\theta JC}$.

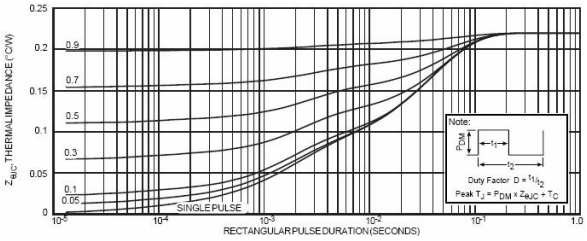

Figure 17 Thermal Impedance 'Family of Curves'

Datasheet Extrapolation Example

Suppose in a switch mode power supply application we want to hard switch 15 Amps at 200 kHz, 400 Volts, and 35% duty cycle on average. The gate drive voltage is 15 Volts, and the gate drive resistance is 15? during turn-on and 5?c during turn-off. Also, suppose we want to let the junction reach 112ºC maximum and can maintain the case at 75ºC. With a 500 Volt device, there is only a 100 Volt margin between the application voltage and V_{DSS}. Barring surges in the 400V bus, the narrow voltage margin is sufficient because the large avalanche capability of a MOSFET provides at "safety net". It is a boost configuration with continuous conduction, so the faster body diode recovery of a FREDFET is not needed; a MOSFET will work fine. Which device should we choose?

Since this is a relatively high frequency application the Power MOS 7® series would be the best choice. Let's look at the APT50M75B2LL. Its current rating is 57 Amps, more than three times the switched current, which is a good starting point considering the high switching frequency and hard switching. We will estimate the conduction loss, switching losses, and then see if the heat can be dissipated fast enough. The total power that can be dissipated is

$$\frac{T_J - T_C}{R_{\theta JC}} = \frac{112°C - 75°C}{0.22\frac{°C}{W}} = 168W .$$

At 112°C, $R_{DS(on)}$ is roughly 1.8 times higher than at room temperature (see Figure 3). So conduction loss is

$$P_{conduction} = 1.8 \cdot 0.075\Omega \cdot 15A^2 \cdot 0.35 = 10.6W$$

For turn-on switching loss, we can look at the figure of switching loss versus current at 125°C shown in Figure 18. Even though our application requires a maximum of 112°C junction temperature, this graph is accurate enough because MOSFET switching energy is not sensitive to temperature except for the temperature-related behavior of the diode in the circuit, and this should not have a big change between 112°C and 125°C. In any case, our estimates will be conservative.

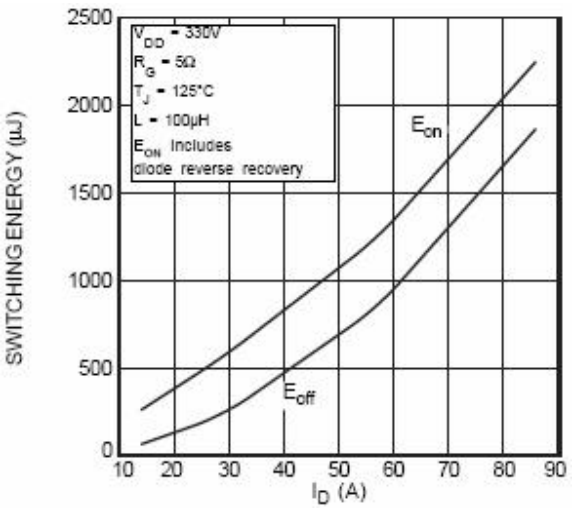

Figure 18 Inductive Switching Loss, APT50M75B2LL

From Figure 18, at 15 Amps, E_{on} is about 300 µJ, and E_{off} is about 100 µJ. These were measured at 330 Volts, and our application has a 400 Volt bus. So we can simply scale the switching energies by voltage:

$$E_{on} = \frac{400V}{330V} \cdot 300\mu J = 364\mu J$$

$$E_{off} = \frac{400V}{330V} \cdot 100\mu J = 121\mu J$$

Data in Figure 18 were also measured with a gate resistance of 5?æ and we will use 15?æat turn-on. So we can use the switching energy versus gate resistance data shown in Figure 19 to scale again.

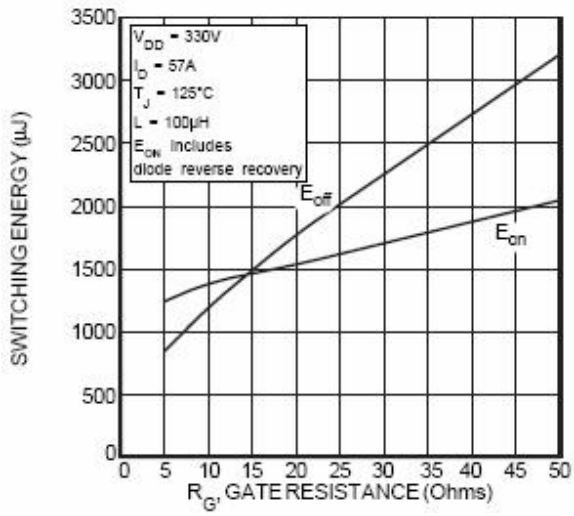

Figure 19 Switching Energy vs. Gate Resistance, APT50M75B2LL

Even though the test current in Figure 19 is higher than our application current, it is reasonable to apply the ratio of change in switching energy from Figure 19 to our case. From 5?Uto 15?Ư E_{on} changes by a factor of about 1.2 (about 1500µJ / 1250µJ, just looking at Figure 19). Applying this to the voltage-corrected data we looked up in Figure 18, we get

$$E_{on} = 1.2 \cdot 364\mu J = 437\mu J$$

Switching losses are

$$P_{switch} = f_{switch} \cdot (E_{on} + E_{off})$$
$$= 200kHz \cdot (437\mu J + 121\mu J) = 112W$$

$P_{conduction} + P_{switch} = 123W$, which is within what is allowed to keep the junction below 112°C with the case cooled to 75°C. So the APT50M70B2LL will meet the requirements of this example application. The same techniques can be used to see if a smaller MOSFET will work.

As a practical matter, the losses are high for a single device, dominated by far by the turn-on switching loss. To keep the case at 75°C will probably require a ceramic insulator (for electrical isolation) between the case and high capacity heat sink. An advantage of a MOSFET is that snubbers and/or resonant techniques can be applied to reduce switching losses without worrying about voltage or temperature-dependent switching effects in the MOSFET.

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