

## MicroNote 114

---

# Derating Silicon Transient Voltage Suppressors at Elevated Temperatures

---

By Kent Walters

The electrical characteristics on transient voltage suppressor (TVS) datasheets are listed at 25 °C for breakdown voltage ( $V_{(BR)}$ ), standby current ( $I_D$ ), peak impulse current ( $I_{PP}$ ), clamping voltage ( $V_C$ ), and peak pulse power ( $P_{PP}$ ). For surge performance, the  $P_{PP}$  is important to also characterize and derate at elevated temperatures. For TVS devices, this differs in what temperature limits may be for very short transients, particularly for the internal junction temperatures ( $T_J$ ) compared to other diodes, such as zeners rated for continuous power.

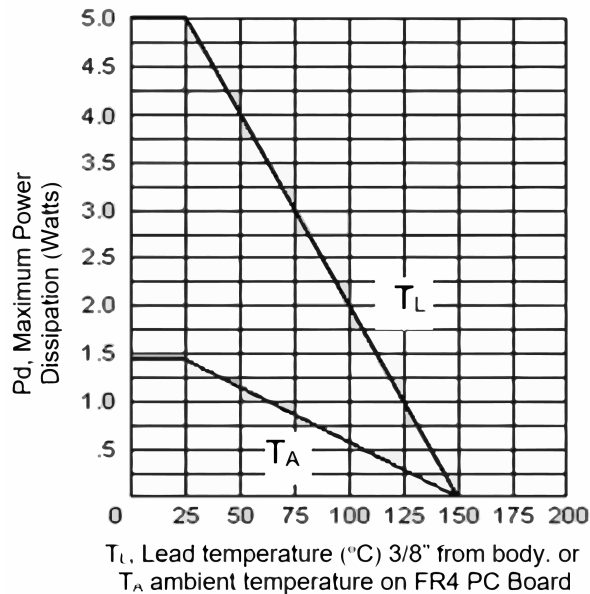
For many diodes where the average or continuous power is provided as a maximum rating at 25 °C, the peak temperatures for linearly derating to zero are often shown as 175 °C for hermetic devices in glass, metal, or ceramic packages, and 150 °C for plastic packages in the industry. These may also vary depending on manufacture.

The maximum temperature ratings are also influenced by the internal junction temperature of the device, which will exceed the applicable external reference points on the device (such as case ( $T_C$ ), leads ( $T_L$ ), end cap ( $T_{EC}$ ), solder point ( $T_{SP}$ ), and so on). When the full-rated power is applied to the device, the  $T_J$  is significantly greater in value than the external reference points. The increase in junction temperature with applied power can also be expressed as thermal resistance junction to case ( $R_{\theta JC}$ ), junction to lead ( $R_{\theta JL}$ ), junction to end cap ( $R_{\theta JEC}$ ), junction to solder point ( $R_{\theta JSP}$ ), etc. These thermal resistance values are in units of °C/W.

The average or continuous power ratings of diodes are typically derated with temperature from the full-rated power level to zero power at the maximum rated  $T_J$ . The horizontal axis on this derating is typically in terms of the external reference point for the device under test (DUT), such as the  $T_L$ ,  $T_C$ ,  $T_{EC}$ ,  $T_{SP}$ , etc. However, it may also be derated relative to ambient temperature ( $T_A$ ) with a specified mounting method, such as an FR4 PC board with 1 oz Cu. In these examples, the thermal resistance from junction to ambient ( $R_{\theta JA}$ ) is much higher, since there is often a significant amount of added thermal resistance from the solder mounting point of the DUT to ambient through the PCB (often FR-4 material with 1 oz copper). These added parasitic thermal resistance values from PC board mounting methods are often higher than the DUT itself.

These further considerations in mounting on PC boards typically reduce the dc power capability of the DUT for overall thermal management. An example is shown in [Figure 1 \(see page 2\)](#) for a zener diode with a thermal resistance of 25 °C/W junction to lead or end cap that can be rated at 5 W with an infinite heat sink, but is only capable of 1.4 W on a typical FR4 PC board. It should also be noted that the derating slope of the DUT equates to the inverse value of its thermal resistance in W per degree centigrade, or in this example,  $1/25 = 0.04$  W/°C. When used in this manner, the derating slope should start from the maximum temperature rating, such as 150 °C in this example for a plastic package, and work backwards in temperature to 25 °C or the maximum power rating of the DUT, whichever comes first.

**Figure 1: DC Power Derating Curve**



In contrast to this, TVS devices are not normally operated at continuous power like a zener. Instead they are used in a “standby mode” at the working standoff voltage ( $V_{WM}$ ) near ambient temperatures for optimum surge performance. Also see [MicroNote 134](#) for zener and TVS comparisons.

The specified  $V_{WM}$  is typically at 90% or less of minimum breakdown voltage ( $V_{BR}$ ), as shown in the Electrical Characteristics section of TVS datasheets. In this mode of operation for the TVS, the  $T_J$  is approximately the same temperature as the ambient or external terminations of the device, since the only continuous power is from the very low standby current ( $I_D$ ) or leakage current at  $V_{WM}$ . However, the  $T_J$  significantly increases during any random transients that may occur that approach its maximum surge rating.

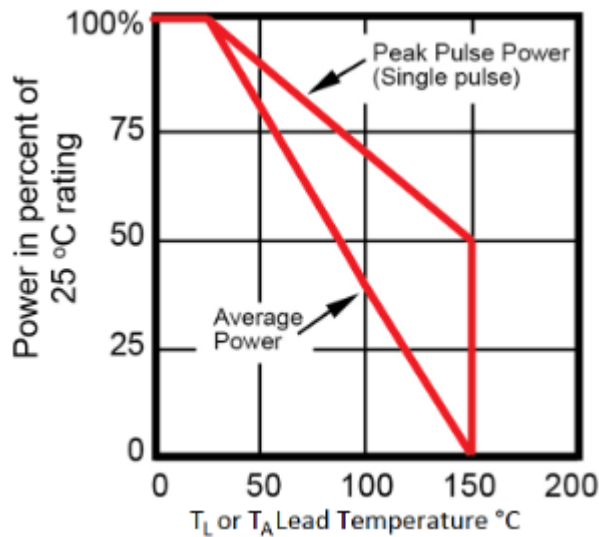
When a silicon TVS device is operated in this manner in the standby mode, any random high-voltage transient will drive the device into avalanche breakdown resulting in a corresponding high current transient through the device where it immediately clamps voltage. This also diverts the large surge current from line to ground when located as a parallel shunt path in front of a protected load. The maximum clamping voltage ( $V_C$ ) during the surge is typically 50 % higher than the specified minimum  $V_{BR}$  at low currents in most TVS datasheets.

It is also during the short transient event that junction temperature ( $T_J$ ) significantly increases. Most of the  $V_C$  increase above  $V_{BR}$  is from the positive temperature coefficient of the avalanche breakdown mechanism and very high  $T_J$  values generated at the p-n junction. A portion of the  $V_C$  increase is also contributed from parasitic resistance or zener “dynamic impedance” of the TVS device for typical rated surge currents at 10/1000  $\mu$ s or as shown for higher surge currents and shorter pulse waveforms in many TVS datasheets. The high  $T_J$  values experienced during this very rapid clamping action can also easily exceed the maximum rated temperatures typically shown for continuous power (150 °C or 175 °C). This higher  $T_J$  phenomenon for short transients is also recognized in MIL-STD-750 for non-destructive tests as found in paragraph 4.8 page 14. It is also now being recognized in TVS performance specs in MIL-PRF-19500.

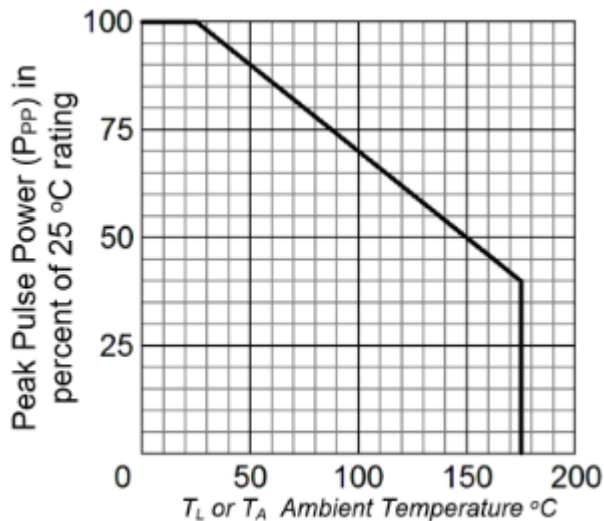
With these observations, the higher  $T_J$  values can be displayed differently for  $P_{PP}$  ratings on TVS devices. Also the  $P_{PP}$  ratings are much higher than continuous power since the thermal impedance for short transients is much lower in degrees centigrade per watt than thermal resistance for continuous power. These high  $T_J$  value projections are also often illustrated in a derating slope to 275 °C. It can also be higher in some TVS datasheets for lower voltage selections when considering the semiconductor physics and silicon “intrinsic” behaviour properties. For example, in low-voltage device types, the active silicon p-n junction includes higher “n” or “p” type doping concentrations and will tolerate higher transient junction temperatures (and higher levels of thermally generated electron-hole pairs) before electrical performance degrades.

The described 275 °C derating slope for  $P_{PP}$  is illustrated in [Figure 2 \(see page 3\)](#) for a plastic device that is typically derated to zero on average or dc power at 150 °C. Another example is shown in [Figure 3 \(see page 3\)](#) for the same  $P_{PP}$  derating slope except for hermetic devices typically rated up to 175 °C.

**Figure 2: Derating Curve for Plastic Packages**



**Figure 3: Derating Curve for Hermetic Packages**



The percentage in derating for  $P_{PP}$  also applies to peak pulse current ( $I_{PP}$ ) for the same clamping voltage ( $V_c$ ). Despite these higher projected internal  $T_J$  values during a transient, the peak pulse power ( $P_{PP}$ ) or peak pulse current ( $I_{PP}$ ) must still be abruptly derated to zero for external temperatures at 150 °C for plastic devices or 175 °C for hermetic packages such as glass, metal, or ceramic as may be applicable to avoid other package issues with surrounding materials. In that respect, the thermal time constant for heat escaping from the active silicon die element inside a package to adjacent materials is in the vicinity of 1 ms for TVS devices such as with 10/1000  $\mu$ s waveforms where most TVS products are rated. As a result, the short transient event (heat source) will conclude before the heat travels well beyond the die region to the extremities of the package or terminals. The internal solder connections or other bonding methods to the die can briefly withstand 275 °C in TVS packages.

As seen in [Figure 2 \(see page 3\)](#) and [Figure 3 \(see page 3\)](#), this derating method for  $P_{PP}$  or  $I_{PP}$  offers greater surge performance for TVS devices versus temperature. For example, this method recognizes silicon p-n junction TVS devices will still have 50% of their capability at 150 °C instead of a severe derating to near zero at 150 °C or 175 °C. This is also included in [MicroNote 132](#) for the “DIRECTselect Methods” in showing maximum rated peak pulse current  $I_{PP}$  at 10/1000  $\mu$ s, or for what is also identified as  $I_P$  on shorter transient threats described in the RTCA/DO160 specification for aircraft.

## Support

For additional technical information, please contact Design Support at:

<http://www.microsemi.com/designsupport>

or

Kent Walters ([kwalters@microsemi.com](mailto:kwalters@microsemi.com)) at 480-302-1144


**Microsemi Corporate Headquarters**

One Enterprise, Aliso Viejo,  
 CA 92656 USA  
 Within the USA: +1 (800) 713-4113  
 Outside the USA: +1 (949) 380-6100  
 Fax: +1 (949) 215-4996  
 Email: [sales.support@microsemi.com](mailto:sales.support@microsemi.com)  
[www.microsemi.com](http://www.microsemi.com)

© 2018 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and service for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct an complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any product and services at any time without notice.

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at [www.microsemi.com](http://www.microsemi.com).