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Power Matters.™

Energy Efficient Digital Frontend Designs With PolarFire FPGAs For Small Cells

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Overview

In mobile access networks, small cell based indoor coverage scenarios are increasing. Power over Ethernet (PoE) based small cell deployments not only provide the lowest total cost of operation (TCO) for operators but also demand low power in implementation.

This paper highlights the lowest power and performance optimized PolarFire™ FPGAs suitability for digital frontend (DFE) designs in small cells.

Introduction

Conventional macrocells alone are no longer sufficient to handle the needs of today's wireless subscribers because of the growing demand for in-building wireless coverage and the massive influx of mobile data traffic. Moreover, the imminent adoption of centimeter and millimeter wave spectrum, to support higher data rates in 5G networks, necessitates the use of much smaller cell sizes.

To cope with the growing capacity and coverage requirements, mobile operators are significantly increasing their investments in a variety of Heterogeneous Network (HetNet) infrastructure technologies such as strategically deployed small cells, carrier Wi-Fi, and Distributed Antenna System (DAS) networks. Wireless infrastructure includes many elements—macro base stations, metro cells, outdoor and indoor DAS, small cells and more—all working together in a HetNet environment as summarized in the following figure.

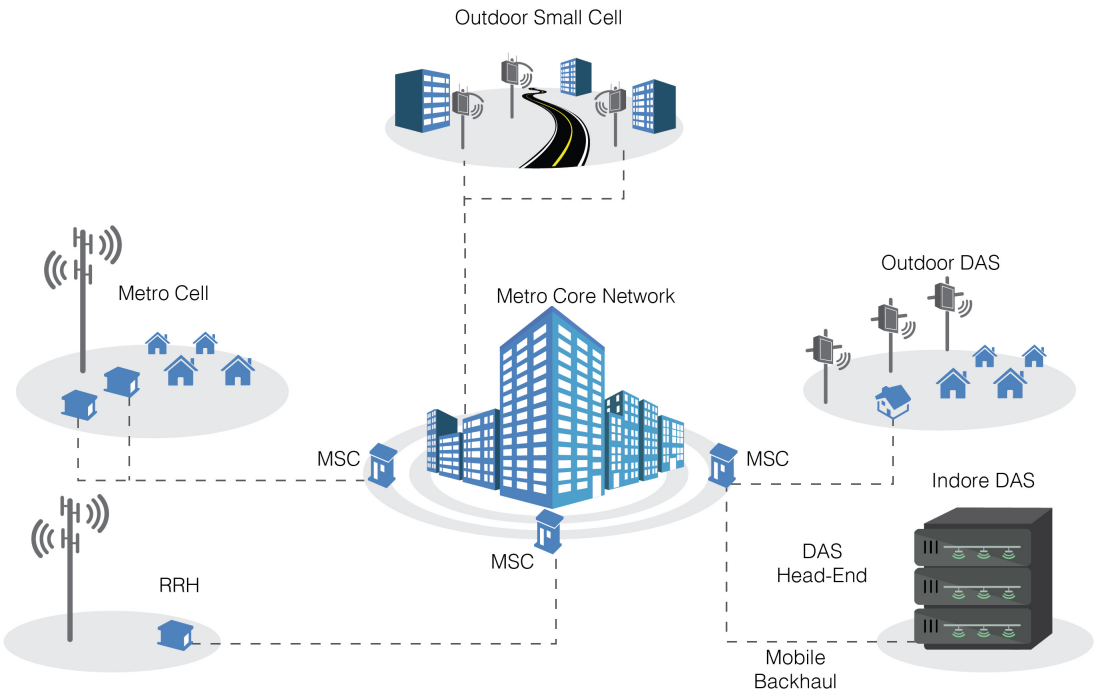


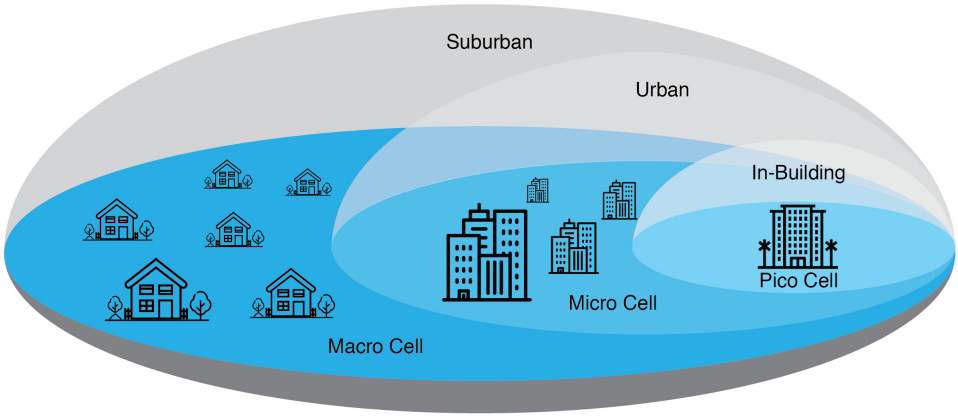
Figure 1: HetNet Infrastructure

Wireless service providers will continue to add capacity to their networks with small cells to connect more users than what an entire base station once supported. Around 80% of all mobile broadband traffic is consumed by users located indoors; the challenge is to deliver fast and seamless connectivity to indoor users. There are multiple deployment options for providing indoor mobile broadband, out of which, the indoor small cells provide the lowest TCO for providing coverage and capacity to indoor hot spots in enterprises and public buildings. These small cells enable service providers to eliminate expensive rooftop systems, and their installation and rental costs, which reduce the overall cost. These small cells also improve the performance of mobile handsets. Mobile phones transmit at lower power levels if they are in the range of a small cell base station, this setup effectively increases the battery life of mobile phones.

Small Cells

Small cells are small base stations with lower transmit power levels, and were were added in Release 9 of the 3GPP LTE specification in 2008. Small cells are a single element in the network densification drive. Network densification aims at adding more base station connections to the existing wireless infrastructure. These cells typically have a range from 10 meters to several hundred meters. Types of small cells include femtocells, Picocells, and microcells—broadly increasing in size from femtocells to microcells. The main goal of small cells is to increase the edge data capacity, speed, and overall network efficiency of the macrocell.

In a small cell network, each small cell adds a new cell with new capacity and coverage depending on achievable signal-to-interference-plus-noise ratio (SINR). Also, air interface resources are reused in a small cell network. In buildings, small cell networks predominantly use LAN cabling, which is very easy to install and does not require skilled personnel. The output power, cell radius sizes and other features of different types of base stations, from small cells to macrocells are summarized in the following figure.



Type	Output Power(W)	Coverage(Km)	Users	Location
Macrocell	>50	10 to 30	>2000	Outdoor
Microcell	1 to 10	0.2 to 2	100 to 1000	Outdoor/Indoor
Picocell	0.25 to 1	0.1 to 0.2	20 to 100	Outdoor/Indoor
Femtocell	<0.25	<0.1	<20	Indoor

Figure 2: Base Station Types

Seeing that digital indoor distributed solutions are inevitable, traditional macro network vendors are joining to launch digital indoor solutions. Many of these small cells will be hosted by enterprise customers. Outdoor small cell deployments can be complicated by backhaul challenges and negotiations with municipalities. In Contrast, many carriers have found that enterprise customers are eager to deploy small cells indoors and use their existing power supplies. In this deployment, maximizing performance and supporting multiple users with a relatively limited power budget is a unique challenge. PoE is commonly used to power indoor small cells. A typical block diagram of the data path of a small cell is shown in the following figure.

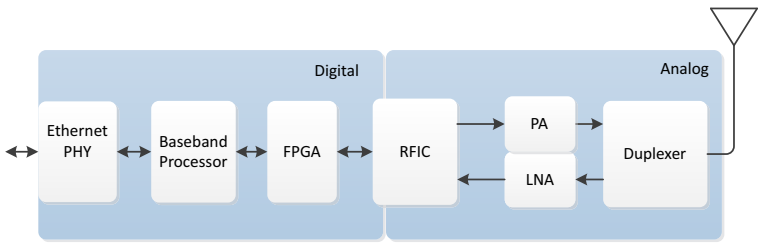


Figure 3: Data Path Of a Small Cell

Power Budget With PoE

Carriers want to deploy the next-generation small cells in metrocell indoors to give users the best experience they demand. They want to deploy them using PoE, which offers an easier, faster, and cheaper way to power small cells than routing another power line. It is well known that baseband digital devices often survive on a restricted power budget, because the RF amplifiers consume 50-70% of the power. The typical power budget of a small cell is shown in the following figure.

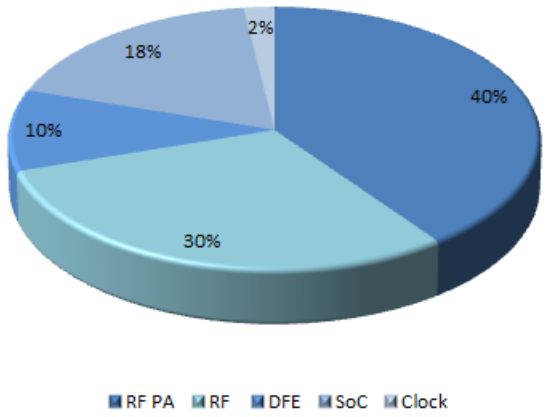


Figure 4: Power Budget Of PoE Based Small Cell

FPGAs For DFE Designs

There are different methodologies to implement DFE functionalities in practical hardware—FPGA, ASIC, and DSP. Each has its strength and weakness in terms of flexibility, cost and power consumption. These aspects have to be considered when defining the overall system architecture. FPGAs are widely used for DFE designs and low power is extremely important along with performance. The following figure shows the basic functional blocks of DFE in FPGAs.

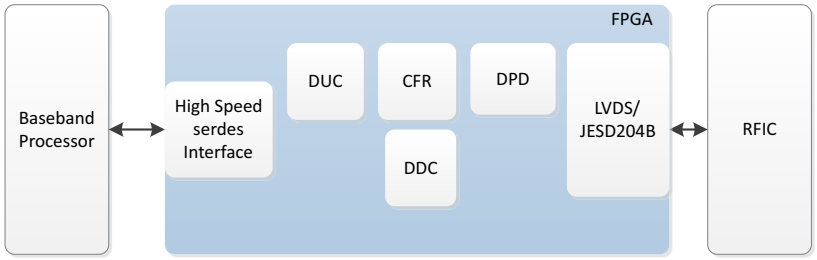


Figure 5: DFE Functional Blocks in an FPGA

As shown in the previous figure, high-speed serial protocol —JESD204B or parallel LVDS, which is part of RFIC digital interface, are handled in FPGA. Digital Up Converter (DUC) and Digital Down Converter (DDC) are high signal processing intensive blocks, which demand performance at a high clock rate. The RF power amplifier's performance improvement algorithms such as Crest Factor Reduction (CFR) and Digital Pre-distortion (DPD) helps improve the efficiency of Power Amplifiers, and thus reduce overall power consumption.

Hard blocks like MACC and transceiver are the key requirements in DFE designs to support wider bandwidths and serial interface standards. Transceiver performance is closely coupled with the need for higher signal processing capability to transfer data to and from the base station and provide efficient connectivity to high-speed data converters.

PolarFire FPGAs for DFE Designs

PolarFire FPGAs, providing power efficiency with required performance, are ideal for DFE designs. PolarFire™ FPGAs are the fifth generation family of non- volatile FPGA devices from Microsemi, built on state-of- the-art 28nm non-volatile process technology. Cost- optimized PolarFire FPGAs deliver the lowest power at mid-range densities.

The following sections briefly discuss the capabilities of PolarFire Math blocks, transceivers, and power efficiency.

Math Blocks in PolarFire FPGAs

With up to 1,480 MACC blocks, PolarFire devices deliver the 1287 GMAC processing, which is important for implementing critical digital algorithms in these systems. PolarFire MACC block features pre-adder circuit, 18x18 multiply unit, and 48-bit adder/accumulator. The block also features ROM of depth 16 x 18, which can store coefficients. In radio designs, half-band filter coefficients can be stored in this ROM for better area and timing performance. The signal processing blocks can be built up using CoreFIR and CoreDDS IPs. The PolarFire MACC block is shown in the following figure.

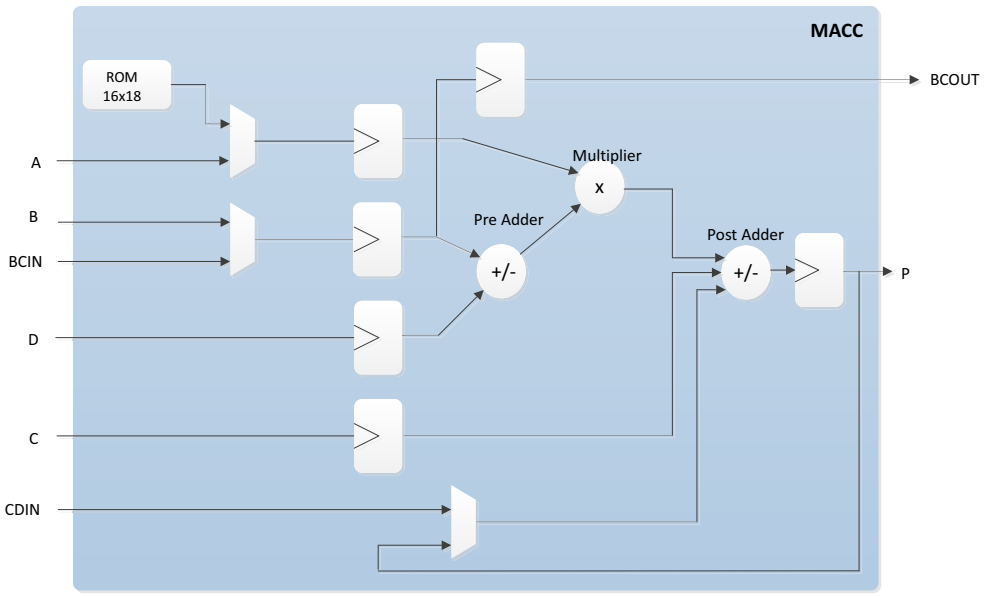


Figure 6: PolarFire MACC Block

Transceivers for High-Speed Data Transfer

PolarFire serial transceivers support high-speed SERDES interface and protocols like CPRI and JESD204B with the data rate of up to 12.7 Gbps. The high-speed SERDES interface is used to connect the FPGA and the baseband processor. JESD204B protocol is used to connect the FPGA and the RF data converter connectivity on the radio. In addition, PolarFire Transmit PLL features jitter cleaner, which can be used to produce jitter cleaned reference to

onboard PLL avoiding external Jitter cleaner. In PolarFire FPGAs, the wireless designs can be clocked at 122.88/245.76/368.64 MHz to meet the performance. The following figure shows the PolarFire Transceiver block.

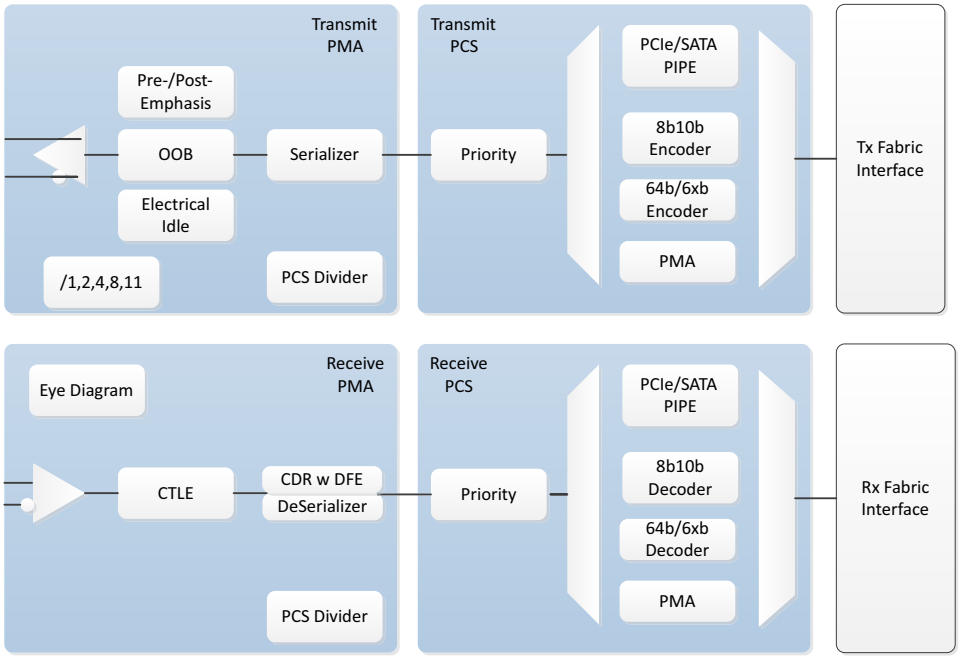


Figure 7: PolarFire Transceiver Block

Power Efficiency

Microsemi FPGAs consume drastically lower total power than competitive FPGAs. The following Flash-based characteristics of Microsemi devices attribute to this low power consumption feature:

- Inherent low leakage current
- Zero in-rush current
- Zero configuration current

The unique Flash*Freeze capability of Microsemi devices enables even lower power operation for low duty cycle applications. The competitive power profile between SRAM FPGAs and Microsemi FPGAs is summarized in the following table.

Table 1 • **Competitive Power Profile**

Power	SRAM FPGAs	Microsemi FPGAs
In-rush Power (during power-up)	High	Zero
Configuration power	High	Zero
Static power	High	Ultra low
Dynamic power	High	Low
Low power Modes	Low	Ultra low
Total Power	High	Lowest power

In Rush and Configuration Current

SRAM FPGAs power up in non-configured state and need to complete the initial power-up and reset sequence. Initially, the various configuration bits are in unknown states and need to initialize on every power cycle. Hence, a current surge is created that may generate a spike as high as several amperes for as long as a few hundred microseconds resulting in an in-rush power. To mitigate this current spike, many SRAM FPGAs have added complex power sequencing requirements to the system. In addition to the in-rush power, a configuration cycle is required each time an SRAM FPGA powers up. This configuration cycle burns additional power and delays the startup of FPGA functionality.

Microsemi FPGAs are live at power-up because they are non-volatile and hence, do not need external configuration devices for reprogrammability. As a result, Microsemi FPGAs eliminate hundreds of milliwatts at device startup and configuration, and thereby, eliminate the need for external devices for mitigation.

Radio Design and Power Comparison

A typical 4G radio system design for LTE is shown in the following figure. The design is configured for 2x2 MIMO LTE 40 MHz with CPRI interface to the baseband at 4.9 Gbps rate, this is the most popular configuration. Digital up conversion and down conversion is done with series of highly optimized cascaded filter chain moving the sample rates form 30.72 Msps to 122.88 Msps and vice versa.

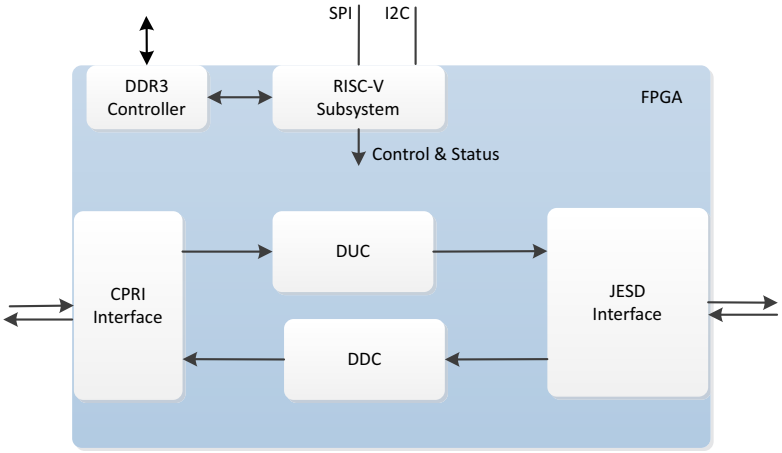


Figure 8: DFE Blocks in PolarFire FPGA

The mixed signal converters popularly used in these systems do come with JESD204B high speed serial digital interface standard. In PolarFire FPGAs, this interface is used in the design at 4.9 Gbps rate with four transceivers in place. A soft processor RISC-V subsystem is used in the FPGA for configuring and monitoring the blocks internal to FPGA and RFICs. The internal control and status of various blocks is handled by the RISC-V subsystem through a standard APB bus interface. The external controlling and monitoring of the RFIC block is also handled by the RISC-V subsystem through SPI and I2C. The CPRI and JESD204B protocols are clocked at 122.88 MHz with the 32-bit user interface. The signal processing blocks DUC and DDC are clocked at 245.76 MHz.

Resource Utilization

PolarFire FPGAs come in different densities. The following table lists the resource utilization of the 4G radio system design on the MPF300T device.

Table 2 • **Resource Utilization on the MPF300TS Device**

Logic Element/Component	Utilization
4LUT	43K
FF	34K
MACC	163
µSRAM	804
LSRAM	161
Transceiver (at 4.9152 Gbps)	5
Core Frequency	245.76 MHz

Power Comparison

Considering the 4G LTE MIMO 2x2 designs, with 40 MHz instantaneous bandwidth clocked at 245.76 MHz, power comparison between PolarFire, Xilinx, and Altera devices is summarized in the following figure.

Process: Industrial, Maximum

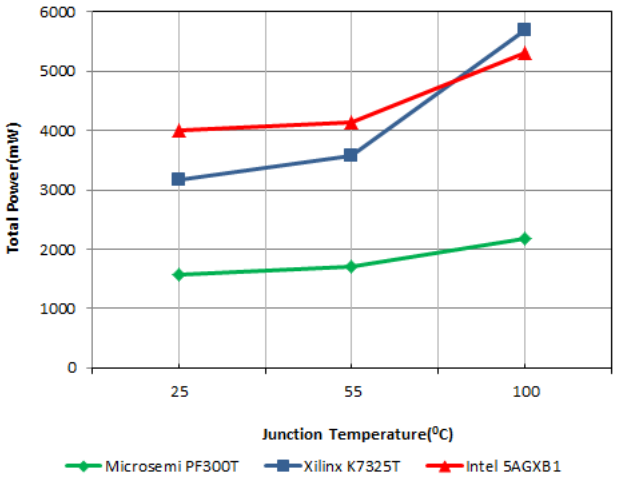


Figure 9: Total Power Comparison

The important components of power in FPGA systems—Static and Dynamic (without I/O), have been charted against other FPGA products in the following figure.

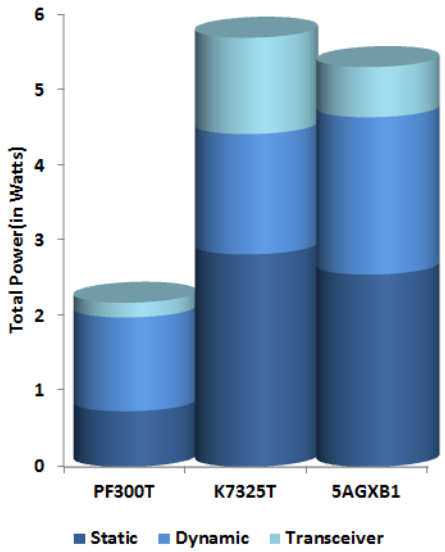


Figure 10: Static, Dynamic, and Transceiver Power Comparison

The power estimator tools are used for the analysis.

Summary

Given the power advantage combined with performance, PolarFire FPGAs are well suited for energy efficient wireless radio designs. For a given thermal design, the low power exhibited by PolarFire FPGAs shall provide a great choice for the system designer to choose ASICs around Baseband SoCs and RFICs with much more flexibility.

References

For more information about the features of PolarFire FPGAs, see the following PolarFire documents.

PO0137: PolarFire FPGA Product Overview

UG0680: PolarFire FPGA Fabric User Guide

UG0677: PolarFire FPGA Transceiver User Guide

PolarFire Power Estimator

UG0752: PolarFire FPGA Power Estimator User Guide

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