Microsemi Corporation: CN18002

November 6, 2017

Customer Notification No: CN18002

Customer Advisory Notice (CAN)

Change Classification: Minor

Subject

RTG4 FPGA Family Changes

Summary

This document describes five Customer Advisory Notices (CAN) for all RTG4 devices. A summary and the action required by the customer can be found in the table below.

Notification	Description	Action required
CAN 18002.1	Vref Output Enable Tie-off	Open your project using Libero SoC v11.8 SP2, and update Vref pin assignment if the DRC check flags your design.
CAN 18002.2	I/O Output Data and Output Enable Inversion	Open your project, and recompile it using Libero SoC v11.8 SP2 if the DRC check flags your design.
CAN 18002.3	LSRAM Timing Marginality	Open your project, and recompile it using Libero SoC v11.8 SP2 if the DRC check flags your design.
CAN 18002.4	LVPECL DC Voltage Specification	None
CAN 18002.5	B-LVDS and M-LVDS DC/AC Specification	Open your project, and disable on-die termination using Libero SoC v11.8 SP1.

CAN 18002.1 Vref Output Enable Tie-Off

Reason for Change

In the device I/O configuration, the Output Enable (OE) of the I/O pair where Vref is assigned to the P-side was incorrectly tied to '0', resulting in high-Z state on any output assigned to the corresponding N-side.

If **ALL** of the following conditions exist in your design, the output assigned to the N-side of the PN pin pair will be set to high-Z.

- Vref is used on MSIO or MSIOD bank **and**
- Vref is assigned to the P-side of a PN I/O pair **and**
- The N-side of the same PN pin pair is a user OUTPUT, BIBUF or TRIBUFF

Description of Change

Libero SoC v11.8 SP2 will enforce a new DRC rule that will prevent the above condition.

Application Impact

The affected output assigned to the N-side of the PN pin pair is in a high-Z state. This is a time zero failure.

Action Required

Open your existing project in Libero SoC v11.8 SP2. If the above condition is detected when opening your project, it will be flagged by the following message:

"Your design '…' contains an IO configuration which is not legal. An output is placed on the N side of a differential IO, where the P side is a VREF pin. You must change the affected IO's using the IO Editor or a PDC constraint."

Resolve the error by either moving the Vref assignment to another pin on the I/O bank, or by moving the output assigned to the N-side.

Products Affected by this Change

See Appendix A.

CAN 18002.2 I/O Output Data and Output Enable Inversion

Reason for Change

I/O Output Data and Output Enable inversion occurs during Automatic I/O Register Combining with Libero SOC v11.8 SP1. This reverses the polarity of the inputs to OUTBUF/BIBUF/TRIBUFF cells.
This is a time zero failure and can be detected in post-layout simulation. Only designs created in Libero SoC v11.8 SP1 are affected. The polarity is changed on the output data and output enable path of an I/O (OUTBUF, BIBUF, or TRIBUFF). This occurs when the FPGA fabric flip-flop driving the output data or output enable port is automatically combined into the I/O output flip-flop or output enable (OE) flip-flop (also called out_reg and en_reg respectively). This incorrect inversion does not occur on I/O registers that were combined manually via user-specified I/O register constraints.

Output delay constraints in the Layout SDC (i.e., set_output_delay), which are applied to the output port during layout, will enable automatic I/O register combining under certain conditions:

- Register output to I/O buffer fanout is 1.
- No user-specified (manual) constraints to preserve the fabric flip-flops (i.e., set_preserve).
- No user-specified (manual) constraints to combine the output and output enable flip-flops into their respective I/O registers (i.e., set_ioff).

Description of Change

Libero SoC v11.8 SP2 will fix the bug introduced in Libero SoC v11.8 SP1. When opening a project, a DRC check will inform you of any changes required with the following message:

"Your design '...' contains IO-Register combinations which need to be updated. Please re-run Place and Route."

Application Impact

This is a time zero failure. Outputs and the output enable path that previously had been working properly will be inverted from their desired state.

Action Required

Open your design and recompile using Libero SoC v11.8 SP2 if the DRC check flags your design.

Products Affected by this Change

See Appendix A.

CAN 18002.3 LSRAM Timing Marginality

Reason for Change

The large SRAM (LSRAM) x9 and x12 configurations in dual-port and two-port modes have a circuit timing marginality. These offending LSRAM configurations can cause functional failure during operating life as a result of aging on RTG4 devices.

Description of Change

Libero SoC v11.8 SP2 will detect offending LSRAM configurations when opening your design. If offending configurations are detected, recompiling the design will automatically extend address space, or swap read/write ports for certain LSRAM x9 and x12 configurations to maintain desired functionality while avoiding affected configurations. Some configurations will prompt the user to regenerate the LSRAM block.

Application Impact

- LSRAM x18 and x36 configurations are NOT affected. Since error detection and correction (EDAC) is available only in x18 and x36 configurations, LSRAM with EDAC enabled is not affected.
- x9 and x12 configurations, in single-port mode are NOT affected.
- Only x9 and x12 configurations, in dual-port or two-port mode are affected.

Action Required

Open your project and recompile using Libero SoC v11.8 SP2 if the DRC check flags your design.

- If the DRC check does not detect offending LSRAM configurations, no action is required.
- If the DRC check detects offending configurations when using CoreFIFO, regenerate CoreFIFO with Libero SoC v11.8 SP2.
- If the DRC check detects the usage of LSRAM instances in two-port mode with Write x9 and Read x36, please contact Microsemi Technical Support for more information.

Here are examples of Libero messages when offending LSRAM configurations are detected:

When opening existing projects:

```
Info: Your design '…' contains LSRAM configurations which need to be remapped:
  Two-Port Write x9, Read x36 blocks - deprecated:        2
  Dual-Port x12 blocks - needs regeneration:              4
  LSRAM blocks where A and B ports need to be swapped:    8
  Dual-Port x9 blocks – need to be remapped:              5

Info: The following Two-Port Write x9, Read x36 LSRAM blocks are deprecated. You must select
alternative configurations for your design, and regenerate them using the      configurator.

Info: The following Dual-Port x12 blocks must be regenerated. You must open the Dual-Port LSRAM
Configurator component that corresponds to these blocks, and regenerate. Note that one component
may contain multiple LSRAM blocks.

Info: The following LSRAM blocks need to have their ports A and B swapped. You must rerun Compile
(Classic Flow) or Synthesize (Enhanced Constraints Flow) for the changes to take effect. No other
action is required.

Info: The following Dual-port x9 blocks need to be remapped. You must rerun Compile (Classic Flow)
or Synthesize (Enhanced Constraints Flow) for the changes to take effect. No other action is
required.
```

When recompiling in Libero SoC v11.8 SP2:

```
Info: LSRAM configurations remapped:
  Two-Port Write x9, Read x36 blocks - deprecated:   2
  Dual-Port x12 blocks - needs regeneration:         4
  LSRAM blocks where A and B ports were swapped:     8
  Dual-Port x9 blocks remapped:                      5

Info: LSRAM blocks where ports A and B ports were swapped.

Info: Dual-Port x9 blocks remapped.

Error: The following 4 Two-Port Write x9, Read x36 LSRAM blocks are deprecated. You must select
alternative configurations for your design, and regenerate them using the configurator.

Error: The following 4 Dual-Port x12 blocks must be regenerated. You must open the Dual-Port LSRAM
Configurator component that corresponds to these blocks, and regenerate. Note that one component
may contain multiple LSRAM blocks
```

Products Affected by this Change

See Appendix A.

CAN 18002.4 LVPECL DC Voltage Specification

Reason for Change

The preliminary RTG4 datasheet revision 2 contains errors in the LVPECL DC voltage specification. In the production RTG4 datasheet revision 3, the input common mode voltage and input differential voltage specifications have been updated for the LVPECL I/O standard. There is no change to the availability of the 100-Ω internal on-die termination (ODT) for LVPECL I/Os.

Description of Change

The following tables show the preliminary and production values for these specifications.

Table 1 • Preliminary LVPECL Specification

Symbols	Parameters	Min	Max	Units
VICM	Input common mode voltage	0.3	2.8	V
VID	Input differential voltage	100	1000	mV

Table 2 • Production LVPECL Specification

Symbols	Parameters	Min	Max	Units
VICM	Input common mode voltage	0.6	1.8	V
VID	Input differential voltage	600	2400	mV

Application Impact

The updated VID specification should not impact RTG4 board design because:

- The preliminary VID min specification of 100 mV implies a very weak LVPECL driver sourcing only 1mA across the 100-Ω internal ODT. Typical LVPECL drivers are relatively high current drivers.
- The production VID min specification of 600 mV should be compatible with a typical LVPECL driver.

Action Required

None

Products Affected by this Change

See Appendix A .

CAN 18002.5 B-LVDS and M-LVDS DC/AC Specification

Reason for Change

The preliminary RTG4 datasheet revision 2 contains errors in the B-LVDS and M-LVDS DC voltage specification. In the production RTG4 datasheet revision 3, the input common mode voltage, input differential voltage specifications and ODT availability have been updated for the B-LVDS and M-LVDS I/O standards.

The internal 100-Ω ODT has been removed from production datasheet and Libero SoC v11.8 SP1 software. Note that typical B-LVDS and M-LVDS receivers require external termination instead of the internal 100-Ω ODT.

Description of Change

B-LVDS

Table 3 • Preliminary B-LVDS DC Specification

Symbols	Parameters	Min	Max	Units
VICM	Input common mode voltage	0.05	2.4	V
VID	Input differential voltage	0.1	VDDI	V

Table 4 • Preliminary B-LVDS AC Switching Characteristics for Receiver (Input Buffers)

		t_{py}		
	On-Die Termination (ODT) in Ω	Speed Grade -1	Speed Grade STD	Units
Bus-LVDS (for MSIO I/O Bank)	None	2.263	2.662	ns
	100	2.263	2.662	ns
Bus-LVDS (for MSIOD I/O Bank)	None	2.241	2.636	ns
	100	2.241	2.636	ns

Table 5 • Production B-LVDS Specification

Symbols	Parameters	Min	Max	Units
VICM	Input common mode voltage	0.05	2.2	V
VID	Input differential voltage	0.2	VDDI	V

Table 6 • Production B-LVDS AC Switching Characteristics for Receiver (Input Buffers)

		t_{py}		
	On-Die Termination (ODT) in Ω	Speed Grade -1	Speed Grade STD	Units
Bus-LVDS (for MSIO I/O Bank)	None	1.244	1.463	ns
Bus-LVDS (for MSIOD I/O Bank)	None	1.232	1.448	ns

M-LVDS

Table 7 • Preliminary M-LVDS DC Specification

Symbols	Parameters	Min	Max	Units
VICM	Input common mode voltage	0.3	1.2	V
VID	Input differential voltage	50	2400	mV

Table 8 • Preliminary M-LVDS AC Switching Characteristics for Receiver (Input Buffers)

		t_{py}		
	On-Die Termination (ODT) in Ω	Speed Grade -1	Speed Grade STD	Units
M-LVDS (for MSIO I/O Bank)	None	2.263	2.662	ns
	100	2.263	2.662	ns
M-LVDS (for MSIOD I/O Bank)	None	2.241	2.636	ns
	100	2.241	2.636	ns

Table 9 • Production M-LVDS Specification

Symbols	Parameters	Min	Max	Units
VICM	Input common mode voltage	0.05	2.2	V
VID	Input differential voltage	200	600	mV

Table 10 • Production M-LVDS AC Switching Characteristics for Receiver (Input Buffers)

		t_{py}		
	On-Die Termination (ODT) in Ω	Speed Grade -1	Speed Grade STD	Units
M-LVDS (for MSIO I/O Bank)	None	1.244	1.463	ns
M-LVDS (for MSIOD I/O Bank)	None	1.232	1.448	ns

Application Impact

With the internal 100-Ω ODT enabled, performance and functionality may be affected at time-zero because B-LVDS and M-LVDS require different termination resistor values compared to that provided by the ODT.

Action Required

Libero SoC v11.8 SP1 and later software disables ODT for B-LVDS and M-LVDS I/O standards.

- When a design with ODT-enabled B-LVDS/M-LVDS I/Os is first opened in Libero SoC v11.8 SP1 software, the Generate Programming step is invalidated. To continue designing in this software release, disable ODT for all impacted I/O standards.
- If a design contains ODT-enabled B-LVDS/M-LVDS I/Os for high-speed serial interfaces (For example, SERDES REFCLK is ODT-enabled B-LVDS I/O), these configurations with ODT enabled are no longer supported in this software release. To continue designing with Libero SoC v11.8 SP1 and later software, regenerate these configurations with ODT disabled.

Products Affected by this Change

See Appendix A .

Appendix A

Table 11 • List of Affected RTG4 Devices

RT4G150-CG1657EV	RT4G150-LG1657PROTO
RT4G150-LG1657EV	RT4G150-1CG1657PROTO
RT4G150-CG1657E	RT4G150-1CB1657PROTO
RT4G150-LG1657E	RT4G150-1LG1657PROTO
RT4G150-CG1657B	RT4G150-CQ352EV
RT4G150-LG1657B	RT4G150-CQ352E
RT4G150-1CG1657EV	RT4G150-CQ352B
RT4G150-1LG1657EV	RT4G150-1CQ352EV
RT4G150-1CG1657E	RT4G150-1CQ352E
RT4G150-1LG1657E	RT4G150-1CQ352B
RT4G150-1CG1657B	RT4G150-CQ352PROTO
RT4G150-1LG1657B	RT4G150-1CQ352PROTO
RT4G150-CG1657PROTO	RT4G150-CQ352ES
RT4G150-CB1657PROTO	RT4G150-CQ352MS

Contact Information

If you have any questions, please contact Microsemi's SoC Technical Support at soc_tech@microsemi.com.

Regards,

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