Microsemi Corporation

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Product/Process Change Notification No: PCN17026

Change Classification: Major

Subject: RTG4 FPGA Family Important Changes

Contents

PCN17026.1 LVDS DC Voltage Specification

Description of Change

The input common mode voltage and input differential voltage specifications have been changed for the LVDS25 and LVDS33 I/O standards.

LVDS25 Changes

Current LVDS25 Specification

Symbols	Parameters	Min	Typical	Max	Units
VICM	Input common mode voltage	0.05	1.25	2.35	V
VID	Input differential voltage	100	350	600	mV

New LVDS25 Specification

Symbols	Parameters	Conditions	Min	Typical	Max	Units
VICM	Input common mode voltage	With on-die termination	0.05	1.25	1.5	V
		With external differential termination	0.05	1.25	2.2	V
VID	Input differential voltage	With on-die termination	200	350	2400	mV
		With external differential termination	200	350	2400	mV
Rt	Termination Resistance	On-die termination	90	100	150	Ω
		External 100 Ω differential termination	95	100	105	Ω
		External 200 Ω differential termination	190	200	210	Ω

LVDS33 Changes

Current LVDS33 Specification

Symbols	Parameters	Min	Typical	Max	Units
VICM	Input common mode voltage	0.05	1.25	2.35	V
VID	Input differential voltage	100	350	600	mV

New LVDS33 Specification

Symbols	Parameters	Conditions	Min	Typical	Max	Units
VICM	Input common mode voltage	With external differential termination	0.6	1.25	1.8	V
VID	Input differential voltage	With external differential termination	500	–	2400	mV
Rt	Termination Resistance	External differential termination	190	200	210	Ω

Action Required

LVDS25

When VICM > 1.5 V, an external differential termination of 100 Ω (typical) or 200 Ω (typical) is required to meet the minimum input differential voltage specification of 200 mV. A 200 Ω differential termination effectively doubles the differential voltage for a given drive current compared to a 100 Ω on-die termination (ODT). For example, a 2.5 mA current produces 500 mV of differential voltage across the 200 Ω termination, whereas it produces only 250 mV across a 100 Ω termination. When using external termination, please ensure ODT is disabled in Libero SoC software.

This change affects devices using LVDS25, RSDS, Mini-LVDS, and HCSL I/O standards.

LVDS33

An external differential termination of 200 Ω (typical) is required to meet the minimum input differential voltage specification of 500 mV since the LVDS33 receiver no longer supports ODT.

Libero SoC v11.8 SP1 software disables ODT for LVDS33 I/O standards.

- When a design with ODT-enabled LVDS33 I/Os is first opened in Libero SoC v11.8 SP1 software, the Generate Programming step is invalidated. To continue designing in this software release, disable ODT for all impacted I/O standards.
- If a design contains ODT-enabled LVDS33 I/Os for high-speed serial interfaces (For example, SERDES REFCLK is ODT-enabled LVDS33 I/O), these configurations with ODT enabled are no longer supported in this software release. To continue designing in Libero SoC v11.8 SP1 software, regenerate these configurations with ODT disabled.

Products Affected by this Change

See the list of affected devices in the Appendix.

PCN17026.2 Power-up and Power-down Sequence Requirement Changes

Description of Change

The power-up and power-down sequence requirements have been updated for RTG4 devices.

Power-up Sequence

1. VDDPLL Requirements

No power-up sequence is required if the device is held in reset by asserting DEVRST_N until the VDDPLL supplies reach their minimum level recommended in the datasheet.

If the device cannot be held in reset, the following power-up requirements apply:

- All PLLs are held in reset until the VDDPLL supply reaches its minimum recommended level

  OR

- VDDPLL must NOT be the last supply to ramp up and must reach its minimum recommended level before the last supply (VDD or VDDIx) starts ramping up.

2. SERDES_x_Lyz_VDDAIO Requirements

There is no power-up sequence if SERDES_x_Lyz_VDDAIO supplies are tied to VDD. If SERDES_x_Lyz_VDDAIO and VDD cannot be tied together, power up SERDES_x_Lyz_VDDAIO and VDD at the same time.

Power-down Sequence

No power-down sequence is required if an external 1-kΩ pull-up or pull-down resistor is used for each critical output that cannot tolerate an output glitch during power-down or DEVRST_N assertion. If an external resistor cannot be used, the following requirements apply:

- VDDIx supplies are powered down first and remain powered-down through 0V

  OR

- VPP is powered down last. If VPP or VDD levels fall below the minimum recommended level, both VPP and VDD must be powered down through 0V before powering back up. Do not power down VPP without powering down VDD. VPP and VDD can be powered down in any sequence.

Products Affected by this Change

See the list of affected devices in the Appendix.

PCN17026.3 Cold-sparing Supply Termination

Description of Change

The following terminations are required on RTG4 power supplies in cold-sparing mode.

Refer to the *RTG4 I/O User Guide* for more information.

RTG4 Power Supply Termination Requirements for Cold-Sparing Mode

Supply Pins	Description	Cold Sparing Board Tie-Off
VDD	Core supply	10 KΩ to VSS
VDDIx	I/O supplies	Supplied
VDDPLL	PLL supply	Supplied or 10 KΩ to VSS
VPP	Supply for the programming blocks	10 KΩ to VSS
VDDI3	JTAG I/O supply	Supplied
SERDES_x_Lyz_VDDAIO	SERDES analog supplies	10 KΩ to VSS
SERDES_x_Lyz_VDDAPLL	SERDES PLL supplies	Supplied or 10 KΩ to VSS
SERDES_VDDI	SERDES reference clock receiver supply	Supplied
SERDES_VREF	Reference voltage for SERDES reference clock	10 KΩ to VSS
VREF0 VREF9	FDDR voltage reference	10 KΩ to VSS

Products Affected by this Change

See the list of affected devices in the Appendix.

PCN17026.4 Updated Register Timing When Using SET Filter

Description of Change

When the Single Event Transient (SET) filter is enabled, either globally or per instance, the static timing analyzer, SmartTime, does not account for the SET filter impact while analyzing the timing on pins En and SLn of the fabric register or the mathblock register. As a result, SmartTime has been showing more optimistic timing data on these pins when using SET filter. The impact of having SET filter to the fabric register pins' set-up time and hold time is as follows:

Additional delay with SET Filter ON, Tj=125 °C			
Register Pins	**Speed Grade -1**	**Speed Grade -STD**	**Units**
FF:En/SLn setup	917	968	ps
FF:En/SLn hold	313	395	ps
MATH:En/SLn setup	1017	967	ps
MATH:En/SLn hold	162	194	ps

Register timing with SET filter is now updated in Libero SoC v11.8 SP1 software.

Action Required

No action is needed for designs not using SET filters. By default, SET filters are disabled in Libero SoC software.

Customers using SET filters in their designs must open their designs with Libero v11.8 SP1 and re-run the timing analysis. If there are no timing violations, no action is required. If new timing violations exist, the following options can be used to resolve them:

- Re-run place-and-route
- Re-run place-and-route with high effort
- Re-run place-and-route with repair min-delay option
- Run place-and-route with multi-pass
- Adjust timing constraints or use Chip Planner to floorplan the affected interfaces

If timing violations still occur, contact our technical support for further assistance.

Products Affected by this Change

See the list of affected devices in the Appendix.

PCN17026.5 Timing Data Adjustments for a Subset of Fabric to Custom Block Interconnect

Description of Change

Interconnect timing data has been updated to more accurately reflect silicon measurements between the fabric and the surrounding blocks. These fabric to custom block interconnects have variable metal length depending on I/O location that was not accounted for in the previous software timing model. The following table contains the worst-case additional timing delay introduced in Libero SoC v11.8 SP1 software for the following affected interfaces:

- I/O to CCC and GB
- APB to CCC
- CCC to GB
- Fabric to CCC, APB, NPSS, PCIE and FDDR
- Fabric to I/O and I/O to Fabric
- IOINFF
- I/O tap delays

Application Impact

- Clock insertion delays and propagation delays between I/Os and flip-flops depending on the I/O location
- Clock-to-out, external setup and external hold timing are impacted
- The additional timing delay is important for source synchronous applications where I/O delay taps are used to align data and clock
- The impact on register-to-register clock frequencies is less than 1%

Additional delay, Tj = 125 °C			
Affected Interface	**Speed Grade -1**	**Speed Grade -STD**	**Units**
CCC to GB	1040	1224	ps
GB to RGB	207	240	ps
I/O to CCC	680	799	ps
I/O to GB	582	685	ps
APB to CCC	253	297	ps
CCC to Fabric	617	726	ps
Fabric to CCC	966	1136	ps
Fabric to APB	392	461	ps
Fabric to NPSS	379	446	ps
Fabric to PCIE	359	422	ps
Fabric to FDDR	446	525	ps
Fabric to I/O	302	355	ps
I/O to Fabric	147	173	ps

Action Required

Customers must open their designs with Libero v11.8 SP1 and re-run the timing analysis. If there are no timing violations, no action is required. If new timing violations exist, the following options can be used to resolve them:

- Re-run place-and-route
- Re-run place-and-route with high effort
- Re-run place-and-route with repair min-delay option on
- Run place-and-route with multi-pass
- Adjust timing constraints or use chip planner to floorplan the affected interfaces

If timing violations still occur, contact our technical support for further assistance.

Products Affected by this Change

See the list of affected devices in the Appendix.

PCN17026.6 SpaceWire Recovered Data Rate

Description of Change

For the embedded SpaceWire clock and data recovery circuits in RTG4, the recovered data rate has been updated to reflect the latest timing updates in Libero SoC v11.8 SP1 software. The following table contains the updated maximum data rate and frequency:

SET Filter	I/O Bank	Number of Channels	Max Data Rate (Mbps)		Max Frequency (MHz)	
			-1 Speed Grade	-STD Speed Grade	-1 Speed Grade	-STD Speed Grade
OFF	MSIO/MSIOD	14	200	180	100	90
	DDRIO	2	132	116	66	58
ON	MSIO/MSIOD	14	150	132	75	66
	DDRIO	2	132	116	66	58

Products Affected by this Change

See the list of affected devices in the Appendix.

Contact Information

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Regards,

Microsemi Corporation

Any projected dates in this PCN are based on the most current product information at the time this PCN is being issued, but they may change due to unforeseen circumstances. For the latest schedule and any other information, please contact your local Microsemi Sales Office, the factory contact shown above, or your local distributor.

Appendix

List of Affected RTG4 Devices

RT4G150-CG1657EV	RT4G150-LG1657PROTO
RT4G150-LG1657EV	RT4G150-1CG1657PROTO
RT4G150-CG1657E	RT4G150-1CB1657PROTO
RT4G150-LG1657E	RT4G150-1LG1657PROTO
RT4G150-CG1657B	RT4G150-CQ352EV
RT4G150-LG1657B	RT4G150-CQ352E
RT4G150-1CG1657EV	RT4G150-CQ352B
RT4G150-1LG1657EV	RT4G150-1CQ352EV
RT4G150-1CG1657E	RT4G150-1CQ352E
RT4G150-1LG1657E	RT4G150-1CQ352B
RT4G150-1CG1657B	RT4G150-CQ352PROTO
RT4G150-1LG1657B	RT4G150-1CQ352PROTO
RT4G150-CG1657PROTO	RT4G150-CQ352ES
RT4G150-CB1657PROTO	RT4G150-CQ352MS

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