Microsemi

Radiation-Tolerant FPGAs Update
Space Forum 2017

Minh Nguyen
Senior Marketing Manager, Space

Company Overview

- Leading-edge semiconductor solutions differentiated by:
  - Performance
  - Reliability
  - Security
  - Power

- Solid financial foundation
  - FY2016 revenue: $1.6B
  - 4800 employees today

- Major focus products
  - FPGAs and ASIC
  - Timing and OTN
  - Mixed-signal and RF
  - Switches and PHYs
  - Storage controllers
  - Discretes and integrated power solutions

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Microsemi's Space Pedigree

Extensive Space Heritage
- Developing space solutions for six decades
- Proven track record of innovation, quality, and reliability

Broad Solutions Portfolio
- Power, mixed-signal, and digital for bus and payload applications

Expanding our Product Portfolio through Continuous Innovation

A Partner for the Long Run
- 60-year space heritage

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Delivering A Comprehensive Space Portfolio

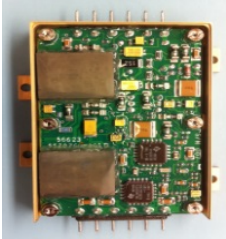|	
Radiation-Tolerant FPGAs	High performance, high density, low power TID up to 300 Krad, SEL immune RTG4 FPGAs up to 300 MHz and 150K LE RTProASIC3, RTAX, and RTSX-SU QML qualified
Rad-Hard Mixed Signal Integrated Circuits	Telemetry and motor control space system managers High-side drivers Regulators and PWMs Extensive custom IC capability
Space-Qualified Oscillators	Ovenized Quartz oscillators Hybrid voltage controlled and temperature-compensated crystal oscillators Cesium clocks
Rad-Hard Power Solutions	Rad-hard JANS diodes, bi-polar small signal transistors, and MOSFETs Rad-hard isolated DC–DC converter modules Custom power supplies: 2 W to > 5 KW Linear and POL hybrids Electromechanical relays

Portfolio Breadth: Example Signal Processing Payload

- FPGAs
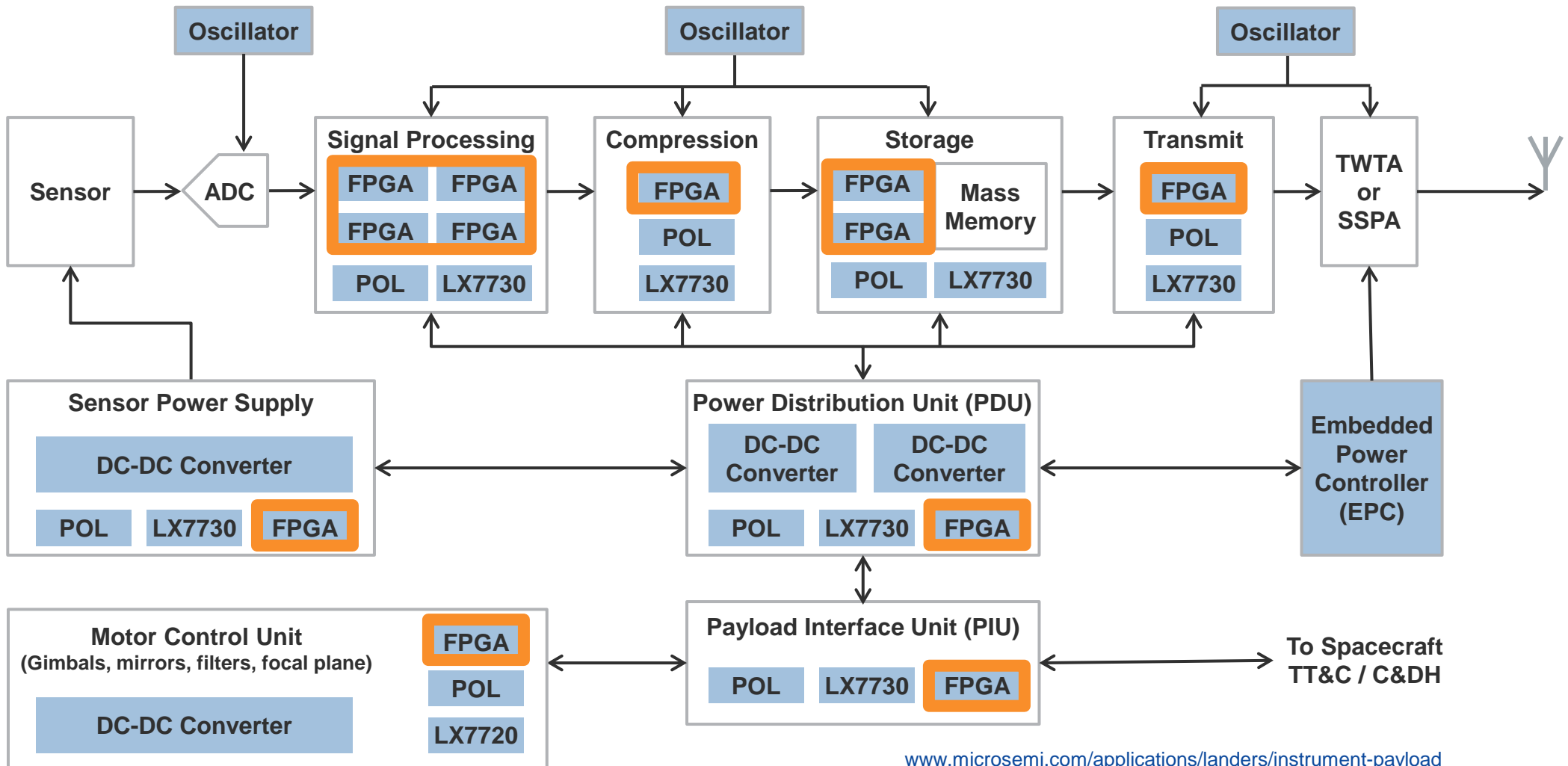
www.microsemi.com/applications/landers/instrument-payload

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Agenda

- ## RTG4 Product Update
  - Introducing CQ352 Package
  - Qualification Update
  - Software and IP

- ## RT FPGA Heritage Update

- ## Export Control Status

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RTG4 Product Update

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RTG4 High-Speed RT FPGAs

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High-Speed Signal Processing
- Reprogrammable, non-volatile
- 65nm Flash process
- 300 MHz
- 150 KLE
- 5 Mbit SRAM
- 462 Multipliers
- 24 x 3.125 Gbps SERDES
- TID > 100 Krad
- SEL immune

RTAX-S / DSP
Command and Control
Medium Speed Processing

RT ProASIC3

RTSX-SU

Logic Density
- 150 KLE
- 20 KLE
- 9 KLE
- 2 KLE

Frequency of Operation
- 50 MHz
- 100 MHz
- 300 MHz
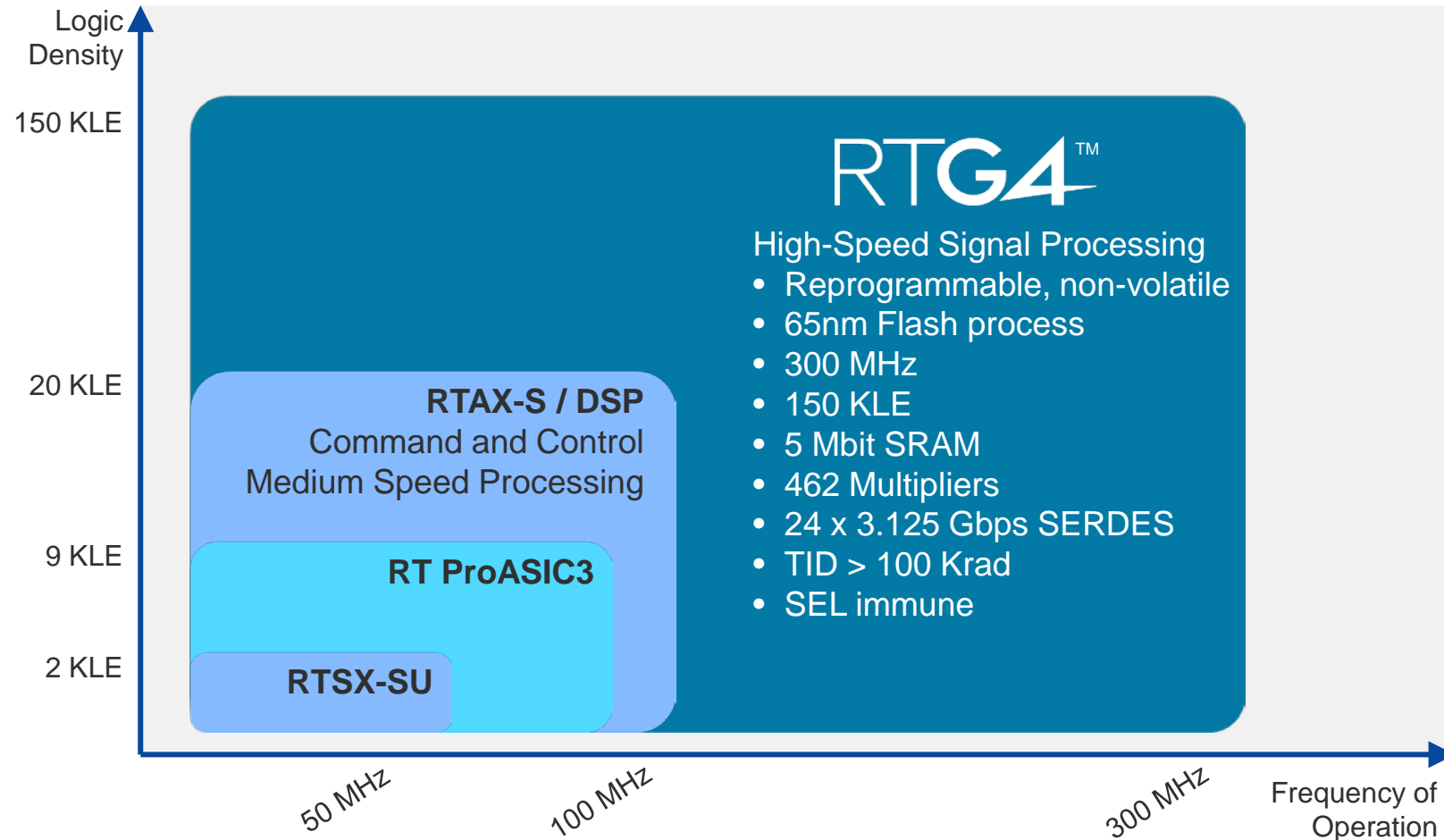
RTG4 mitigates the risks of ASICs and SRAM FPGAs, and has 20x improvement in signal processing throughput

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Introducing the CQ352 Package

Resources	RT4G150	
Logic Elements (TMR Register + 4-Input C Logic)	151,824	151,824
18x18 Multiply-Accumulate Blocks	462	462
RAM Mbits (1.5 Kbit and 24 Kbit Blocks, with ECC)	5.2	5.2
UPROM Kbits	381	381
DDR2/3 SDRAM Controller (with ECC)	2 x 32	0
PCI Express Endpoints	2	1
Globals	24	24
PLLs (Rad Tolerant)	8	8
SpaceWire Clock and Data Recovery Circuits	16	4
User IO (excluding SERDES)	720	166
SERDES lanes (3.125 Gbps)	24	4
Hermetic, Ceramic Packages		
CG1657 (Ceramic Column Grid Array, Six Sigma Columns) LG1657 (Ceramic Land Grid Array, No Solder Termination) CB1657 (Ceramic Ball Grid Array, For Prototyping Only)	Available now	
CQ352 (Ceramic Quad Flat Pack)		Samples in July '17 Flight units in July '18

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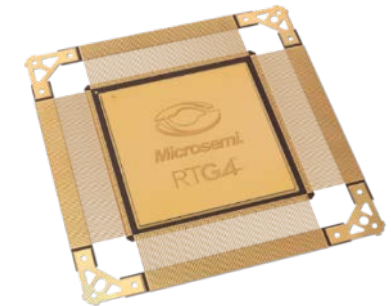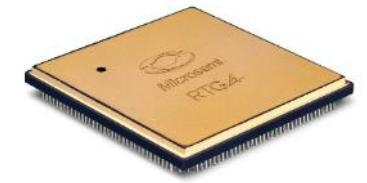
CQ352 Package Update

- CQ352 package will feature:
  - 166 MSIO supporting up to 3.3 V
  - 4 SpaceWire ports
  - 4 SerDes transceivers supporting EPCS and PCIE
  - Embedded Presidio Precious Metal Electrode (PME) 0508 decoupling capacitors
- Package size and weight:
  48 mm x 48 mm x 2.25 mm, 17.5 g
- Pin assignment table and package drawing available on the Microsemi website
- Software support available in Libero SoC v11.7 SP3 and later

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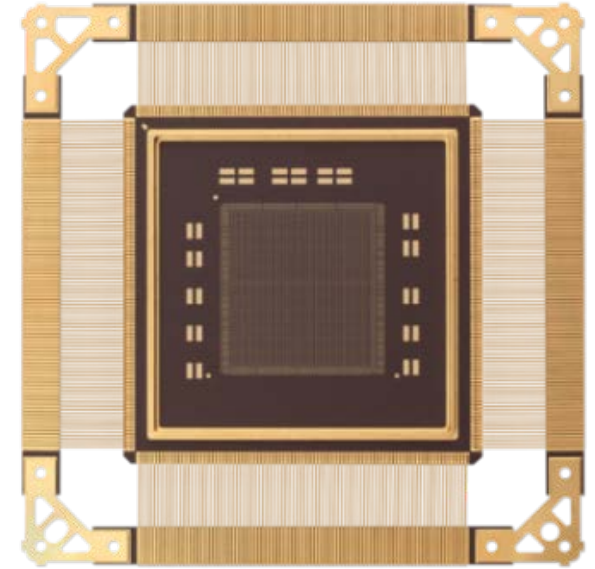
RTG4 Qualification Update

- MIL-STD-883B qualification completed successfully

- Qualification:
  - 3 wafer lots, 54 units
  - 54 units were functional during and after 1,000-hour life test at $T_J \geq 125$ °C, successfully completing qualification group C test
  - All units continued additional life test exceeding MIL-STD-883B requirements:
    54 units were functional during and after 4,000-hour life test at $T_J \geq 125$ °C

- Extensive reliability data set collected for 65nm Flash process from UMC
  - Overall 65nm product FIT rate calculated < 3.11 FIT (60% confidence level, EA = 0.7eV)
  - For more information see *Reliability Report Rev.14*

- ESD Class 1A
  - VDDAIO passed 250 V, other pins passed 2000 V

- Product retention: 20 years at $Tj \leq 115°$ C, or 10 years at $Tj \leq 125°$ C

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RTG4 High Temperature Retention

RTG4 High Temperature Retention (HTR)
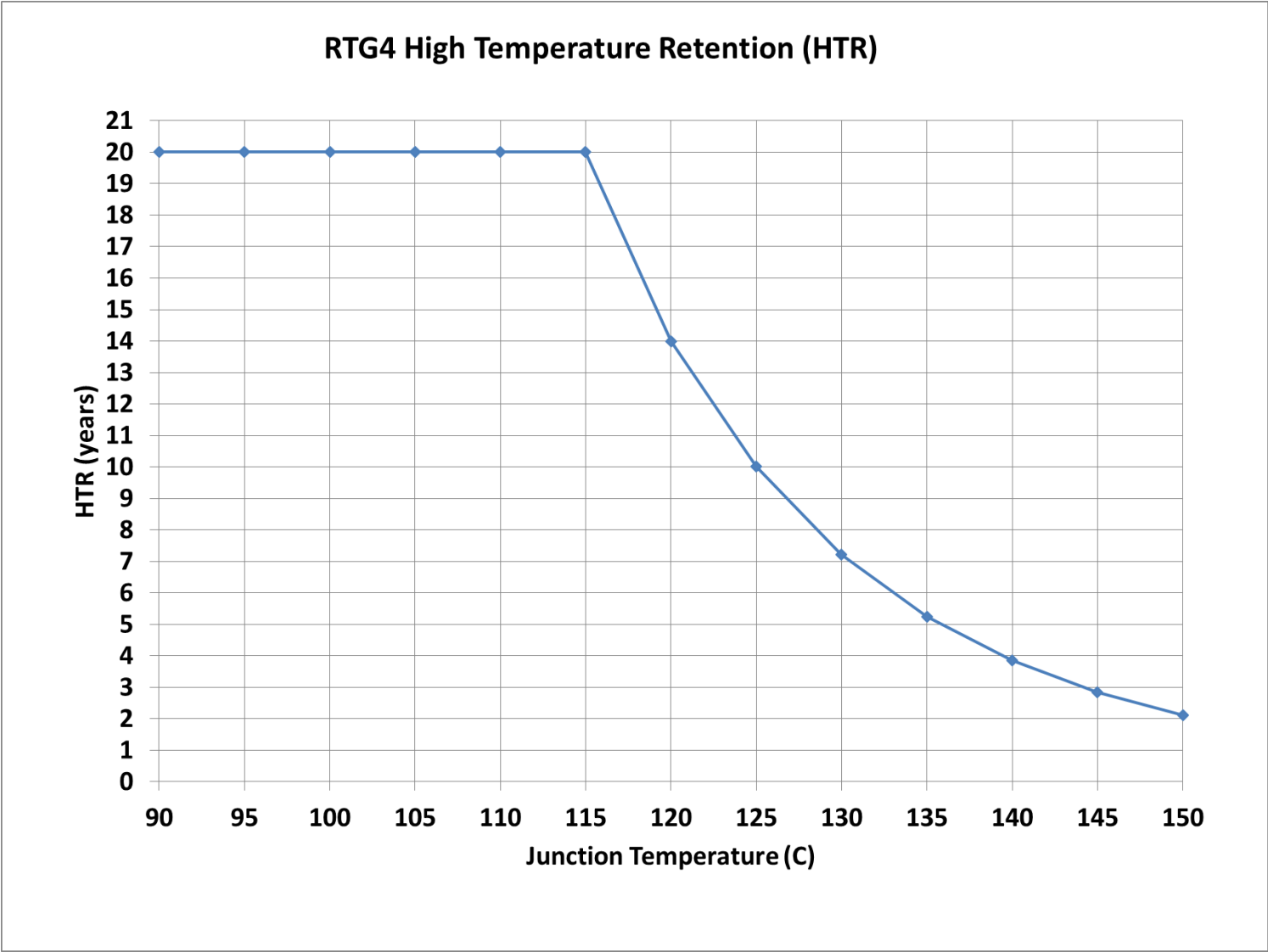
Tj (C)	HTR (Years)
90	20
95	20
100	20
105	20
110	20
115	20
120	14
125	10
130	7.2
135	5.3
140	3.9
145	2.8
150	2.1

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RTG4 Reliability Summary

- **High Temperature Operating Life (HTOL)**
  - 78 units from 4 wafer lots
  - 54 out of 78 units went through 2000-hour life test
  - $\Rightarrow$ Total 132,000 test hours at T_J > 125 °C. <u>Zero failures observed</u>

- **High Temperature Data Retention**
  - 54 units from 6 wafer lots went through 470+ programming test cycles for Non-Volatile Memory Cycling Endurance (NVCE)
    - Total test cycles go beyond datasheet limit of 200 programming cycles
  - After NVCE, 54 units went through 1000-hour life test
  - $\Rightarrow$ Total 54,000 test hours at T_J > 125 °C. <u>Zero failures observed</u>

Reference: *Reliability Report Rev.14*

<u>Note</u>: The latest 4000-hour data will be added in the next Reliability Report revision

RTG4 QML Qualification Status

- QML qualification planning and preparation
  - Technology insertion plan has been approved
  - Audits completed at Microsemi and at fab, bump, assembly, column subs
  - Standard Microcircuit Drawing (SMD) draft in progress
- QML Class Q qualification
  - Completion target: mid 2017
  - Qualification data submitted to DLA, using MIL-STD-883B qualification data
- QML Class V qualification
  - Completion target: early 2018
  - Qualification will use RT4G150 in 1657-pin LGA / CCGA package
    - 45 units from 1 wafer lot
    - 4,000 hour life test to be completed by end of 2017
    - Qualification data will be submitted to DLA after life test completion
    - EV-flow flight units to be available prior to life test completion

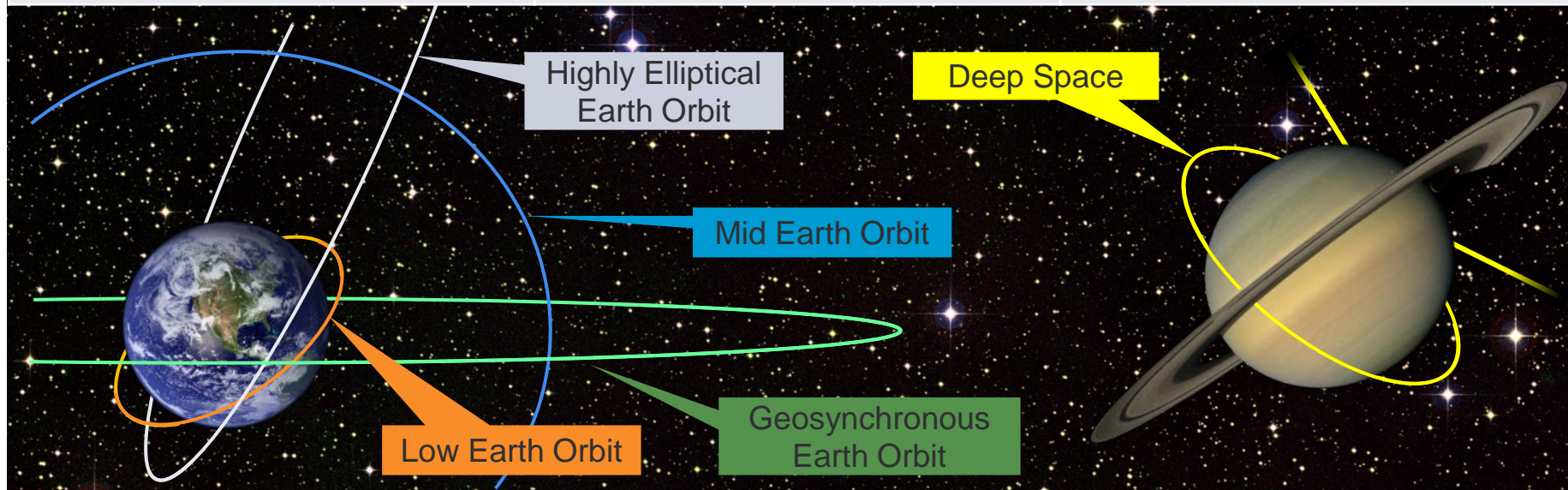# RTG4 Availability and Qualification Schedule

- RT4G150 PROTO FPGAs: Now
- RT4G150 development kit: Now
- Daisy chain packages: Now
- MIL-STD-883 Class B Qualification: Completed
- B-flow flight units: Available to lead time now
- E-flow flight units: Available to lead time now
- EV-flow flight units: Available to lead time now
- QML class Q qualification: Mid 2017
- QML class V qualification: Early 2018

RT4G150 Development Kit

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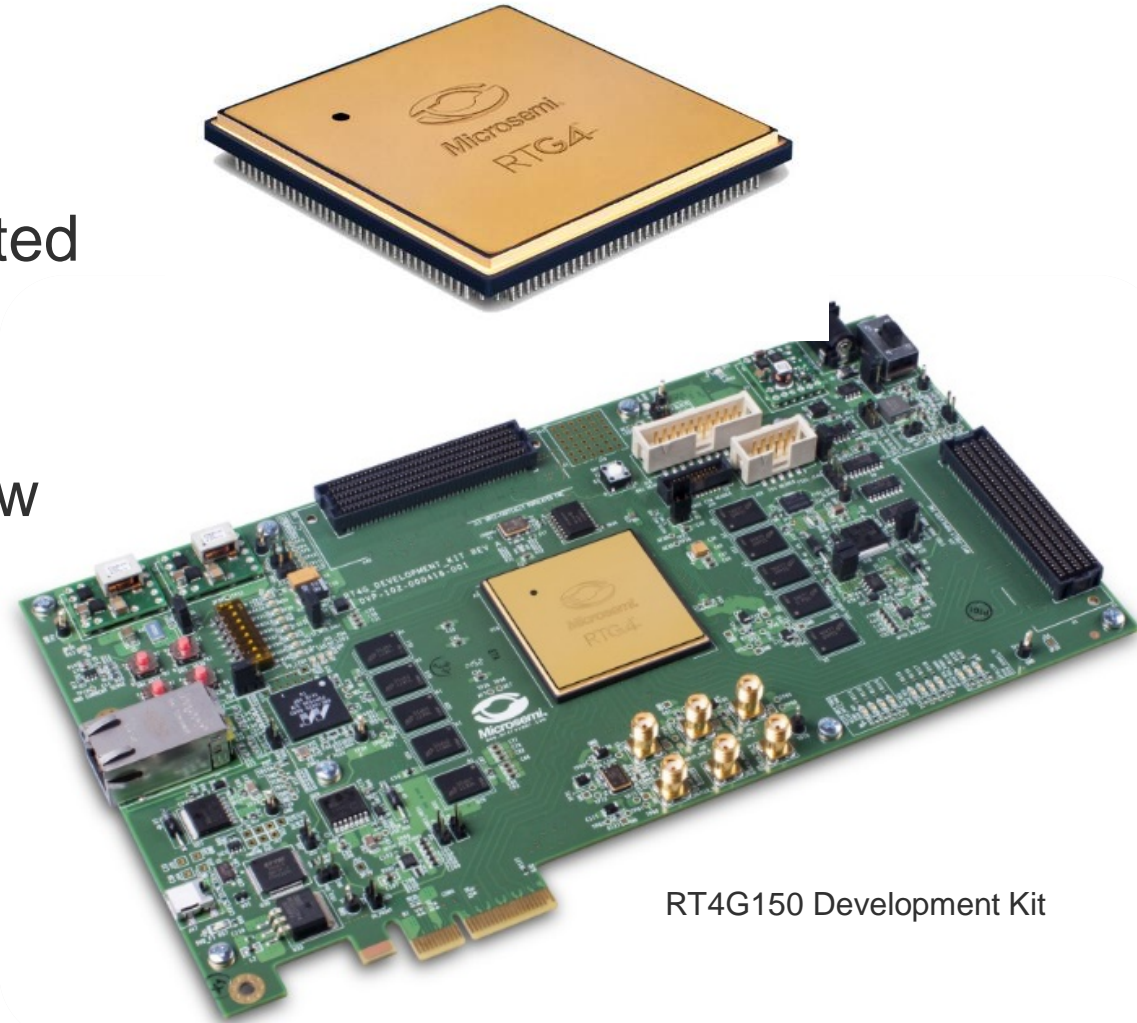
RTG4 Radiation Summary

Total Ionizing Dose	Stays within parametric limits > 125 Krad (Si)	
Single Event Latch-Up	No failure at facility limit of 103 MeV-cm^2/mg, 100 °C	
Configuration Upset	No failure at facility limit of 103 MeV-cm^2/mg, 100 °C	
Flip-Flop Single Event Upset	2.6E-12 errors/bit-day, GEO solar minimum, 1 MHz	
LSRAM Single Event Upset	2.0E-7 errors/bit-day, GEO solar min (no EDAC)	1.1E-11 errors/bit-day, GEO solar min (with EDAC)
uSRAM Single Event Upset	3.1E-8 errors/bit-day, GEO solar min (no EDAC)	2.7E-13 errors/bit-day, GEO solar min (with EDAC)

Highly Elliptical Earth Orbit

Deep Space

Mid Earth Orbit

Low Earth Orbit

Geosynchronous Earth Orbit

RTG4 Software and IP

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Libero SoC Software Highlights

- 11.7 SP2—Released in October 2016
  - Production Timing and Power
    - Timing data update—Preliminary to Production
    - Timing derating for TID 100 Krad reduced to 1% from 5%
    - Power data update—Preliminary to Production
  - Multiple Asynchronous Reset Placement Enhancement
    - Placer ensures that no more than one asynchronous reset drives the pins in each half-row area of the chip. A detailed message is printed for each half-row with violation
    - Placement algorithm was improved
- 11.7 SP3—Released in January 2017
  - CQ352 package support: STD speed grade, advance timing data
- 11.8—Released in March 2017
  - Include Synplify Pro ME (L2016.09M-2), which does not infer feed-through Write mode
- 11.8 SP1—Targeting August 2017
  - DirectC and .DAT file generation for RTG4 inflight programming
    - DirectC tool is free of charge

RISC-V

- **Free and open Instruction Set Architecture (ISA)**
  - 32-bit instructions, optional 16-bit compressed instructions
  - 32-bit, 64-bit, and 128-bit address-space options
  - Quad floating point, virtualization, many cores, heterogeneous computing

- **RISC-V is _not_ an on open-source processor: it is an ISA _specification_**
  - Covered under the Berkeley Software Distribution (BSD) open source license

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RISC-V for RTG4

- **RISC-V software tools**
  - GNU GCC, binutils, newlib stdc library, gdb JTAG/OpenPCD debug
  - LLVM/Clang
  - Linux and Windows dev environment
  - Verification Suite

- **RTG4 support**
  - Soft RISC-V IP is free of charge
  - Preliminary IP is running at 70 MHz in RT4G150 "-1"
  - Sample RISC-V project for RTG4 dev kit available now
  on GitHub website
  - For details, refer to RISC-V website

ARM Cortex M1 in RTG4

■ **ARM Cortex M1**
- 32-bit RISC microcontroller
- Supported by ecosystem from ARM and third-party vendors

■ **IP available now on MSCC website: End User Licensing Agreement (EULA) must be completed in order to download IP**
- Uses DDR controller, SPI, UART, AHB to SRAM, and timer peripherals
- Performance targeting RT4G150, Dash-1 speed grade

Design	RTG4 LUT	RTG4 DFF	RTG4 LSRAM Blocks	RTG4 uSRAM Blocks	MHz
ARM Cortex M1	11,600 (7.7%)	6,900 (4.5%)	2 (1.0%)	128 (61%)	50

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Other RTG4 IP Cores

- 1553 and PCIF—available now from Microsemi
- TSE and SGMII—available now from Microsemi
- JESD204B TX and RX—available now from Microsemi
- SpaceWire
  - STAR-Dundee IP available now
- SpaceFibre
  - STAR-Dundee IP available now,
    multi-lane operation at 3.125 Gbps per lane
- LEON3-FT and LEON4-FT
  - Cobham Gaisler IP available now
- Serial RapidIO—IP vendor evaluation in progress
  — contact Microsemi for details

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RTG4 Summary

- RTG4 now qualified to MIL-STD-883B
  - On track to reach QML-Q in mid 2017
  - On track to reach QML-V in early 2018
- New CQ352 with first samples in July 2017 and B-flow in July 2018

FPGAs in Remote Sensing Payload
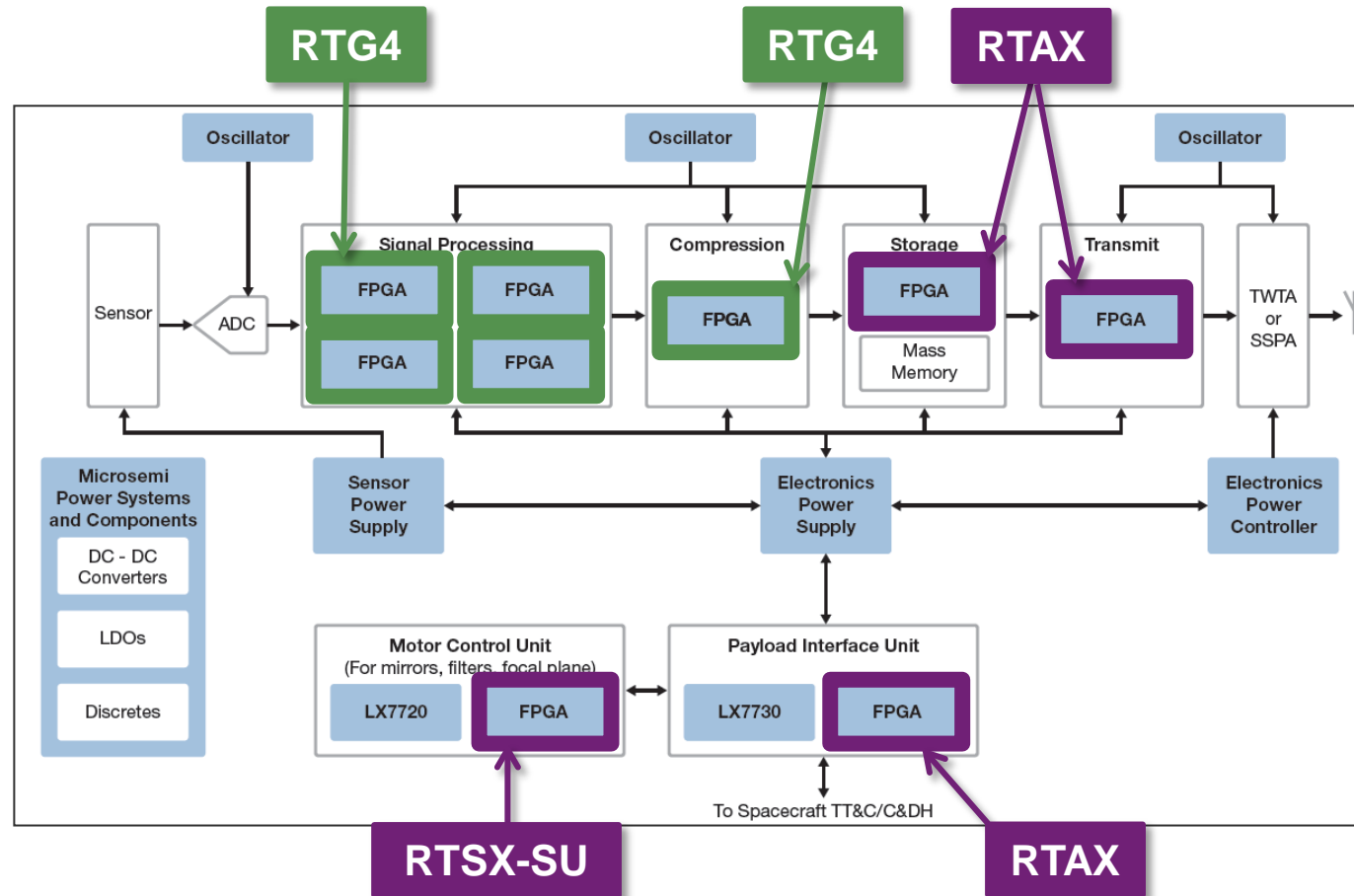
RTG4 complements existing Microsemi Radiation Tolerant FPGAs

Export Control Status

- RT FPGAs removed from US Munitions List

- All Microsemi RT FPGAs now under EAR control
  - Currently using the following Export Control Classification Numbers
    - RTSX-SU   9A515.e.1
    - RTAX-S/SL/DSP   9A515.e.1
    - RT ProASIC3   3A001.a.1.b
    - RTG4   9A515.e.1

For details, see http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-certifications

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