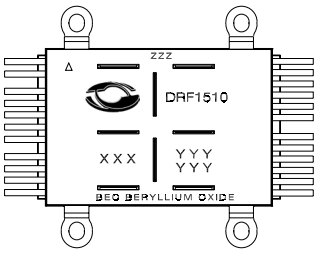
DRF1510

PRELIMINARY

500V, 25A, 13MHz

MOSFET Full Bridge Hybrid

The DRF1510 is a full bridge hybrid containing four high power gate drivers and four power MOSFETs. It was designed to provide the system designer increased flexibility, higher performance, and lowered cost over a non-integrated solution. This low parasitic approach, coupled with the Schmitt trigger input, Kelvin signal ground, provide improved stability and control in Kilowatt to Multi-Kilowatt, High Frequency ISM applications.



FEATURES

- **Switching Frequency: DC TO 13MHz**
- **Low Pulse Width Distortion**
- **Single Power Supply (Per Section)**
- **CMOS Schmitt Trigger Input 1V Hysteresis**
- **RoHS Compliant**
- **Switching Speed 3-4ns**
- **B_{Vds} = 500V**
- **I_D = 25A avg. Per-section**
- **$R_{ds(on)} \leq$ 0.33 Ohm**
- **P_D = 550W Per-section**

TYPICAL APPLICATIONS

- **Class D Full Bridge**
- **Switch Mode Power Amplifiers**
- **HV Pulse Generators**
- **Ultrasound Transducer Drivers**
- **Acoustic Optical Modulators**

Driver Absolute Maximum Ratings (per-Section)

Symbol	Parameter	Ratings	Unit
V_{dd}	Supply Voltage	15	V
IN	Input Voltage	-5 to V_{dd} + 0.3	
T_{JMAX}	Operating Temperature	175	°C

Driver Specifications (Per-Section) @ T_c = 25

Symbol	Parameter	Min	Typ	Max	Unit
V_{dd}	Supply Voltage	10		15	V
IN	Input Voltage High	-5		V_{dd} + 0.3	
$IN_{(R)}$	Input Voltage Rising Edge		2.5		ns
$IN_{(F)}$	Input Voltage Falling Edge		2.5		
I_{DDQ}	Quiescent Current @ V_{dd} = 12V		15	25	mA
I_O	Output Current		15		A
C_{oss}	Output Capacitance		2500		pF
C_{iss}	Input Capacitance Input		35		
R_{IN}	Input Parallel Resistance, V_{in} = 5V, V_{dd} = 12V	1			MΩ
$V_{th\ off}$	V Threshold Off, V_{dd} = 12V, V_{in} = 5 to 0V Ramp	1.0		1.9	V
$V_{th\ on}$	V Threshold On, V_{dd} = 12V, V_{in} = 0 to 5V Ramp	2.2		3.2	
R_g	Gate Resistance	0.4	0.5	0.6	Ω

ESD Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
ESD Protection	Human Body Model		1.5		kV

MOSFET Absolute Maximum Ratings (Per-Section)

Symbol	Parameter	Min	Typ	Max	Unit
BV_{DSS}	Drain Source Breakdown Voltage, V_{dd} = 12V, V_{in} = 0, I_{DS} = 250µA	500			V
I_D	Continuous Drain Current @ T_C = 25°C			30	A
$R_{DS(on)}$	Drain-Source On Resistance V_{dd} = 12V, I_{DD} = 10A		0.25	0.33	Ω
T_{jmax}	Operating Temperature			175	°C
I_{DSS}	Zero Gate Voltage Current V_{DS} = 500V, V_{GS} = 0V			25	µA

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MOSFET Thermal Characteristics (Per-Section Applicable to Per-Module)

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case (Thermal Joint Compound)	.137	°C/W
$R_{\theta JHS}$	Thermal Resistance Junction to Heat Sink	.270	
T_{JSTG}	Storage Temperature	-55 to 150	°C
P_D	Maximum Power Dissipation @ T_{SINK} = 25°C	550	W
P_{DC}	Total Power Dissipation @ T_C = 25°C	1095	

Driver Thermal Characteristics (Per-Section)

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case	1.4	°C/W
$R_{\theta JHS}$	Thermal Resistance Junction to Heat Sink	2.5	
T_{JSTG}	Storage Temperature	-55 to 150	°C
P_D	Maximum Power Dissipation @ T_{SINK} = 25°C	60	W
P_{DC}	Total Power Dissipation @ T_C = 25°C	100	

MOSFET Specification (Per-Section) @ T_C = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
C_{iss}	Input Capacitance (V_{gs}= 0V, V_{DS}= 150V)		1810		pF
C_{oss}	Output Capacitance (V_{gs}= 0V, V_{DS}= 150V)		210		
C_{rss}	Reverse Transfer Capacitance (V_{gs}= 0V, V_{DS}= 150V)		48		

Per Section Output Switching Performance, All Silicon Devices are Die Selected Temp = 25°C

All DATA IS COLLECTED USING THE TEST CIRCUIT AS SHOWN IN FIGURE 2

Symbol	Characteristic	Min	Typ	Max	Typ
t_f	Fall Time 90% to 10% V_{dd} = 12V, V_{in} = 0 to 5V , V_{DS} = 100V, RL = 16.6Ω, CL = 0.4µF	1	TBD	2.5	ns
t_r	Rise Time 10% to 90% V_{dd} = 12V, V_{in} = 0 to 5V , V_{DS} = 100V, RL = 16.6Ω, CL = 0.4µF	10	TBD	35	
$t_{DLY(ON)}$	ON Delay Time, 50% to 50% V_{dd} = 12V, V_{in} = 0 to 5V , V_{DS} = 100V, RL = 16.6Ω, CL = 0.4µF	35	TBD	55	
$t_{DLY(OFF)}$	OFF Delay Time, 50% to 50% V_{dd} = 12V, V_{in} = 0 to 5V, V_{DS} = 100V, RL = 16.6Ω, CL = 0.4µF	50	TBD	70	

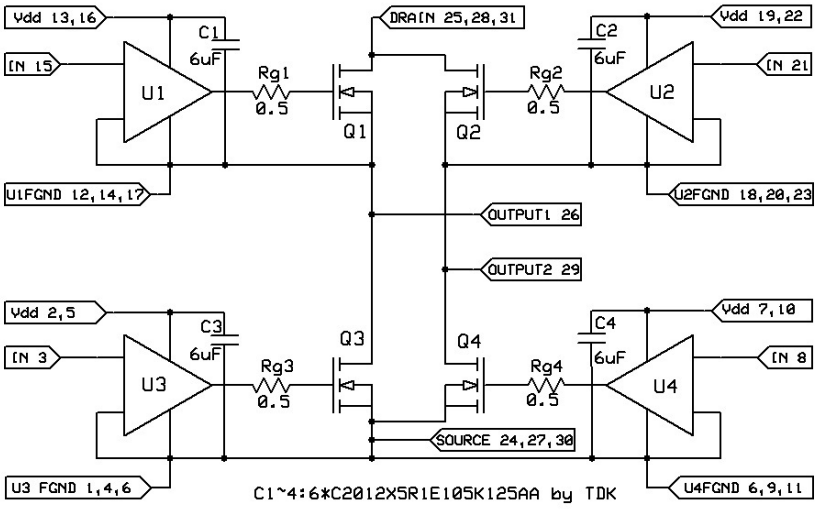

Figure 1, DRF1510 Simplified Circuit Diagram

The DRF1510 is a full bridge power hybrid, see Figure 1 above. Each half bridge of the hybrid consists of two Gate Drivers and two HV Power MOSFETs. In the left HB of the hybrid, U1, U3 is the Gate Driver for Q1, Q3. The input to U1, U3 (IN) with respect to ground (SG) is a CMOS level. C1, C3 provides internal high speed bypassing for the drivers power input +Vdd. Both pins (2, 5 & 13,16) must be attached to the 15V supply and bypassed near each pin. By including the driver high speed by-pass capacitors (C1-C4), their contribution to the internal parasitic loop inductance of the driver output is greatly reduced. This, coupled with the tight geometry of the hybrid, allows optimal gate drive to the MOSFET. The right HB of the hybrid is constructed in an identical manner, U2,4,C2,4 and Q2,4.

None of the inputs to U1 of the DRF1510 are isolated for direct connection to a ground referenced power supply or control circuitry. **Isolation appropriate to full bridge configuration is the responsibility of the end user.** The IN pin is the input for the control signal and is applied to a Schmitt Trigger. **The SG pin, a Kelvin return, is reserved for the control signal ground return only** (Pin 4, 9, 14, 20). On the output side are the Drain (25, 28, 31), Source (24, 27, 30) and Output (26, 29) connections. It is imperative that output currents be restricted to these pins by design.

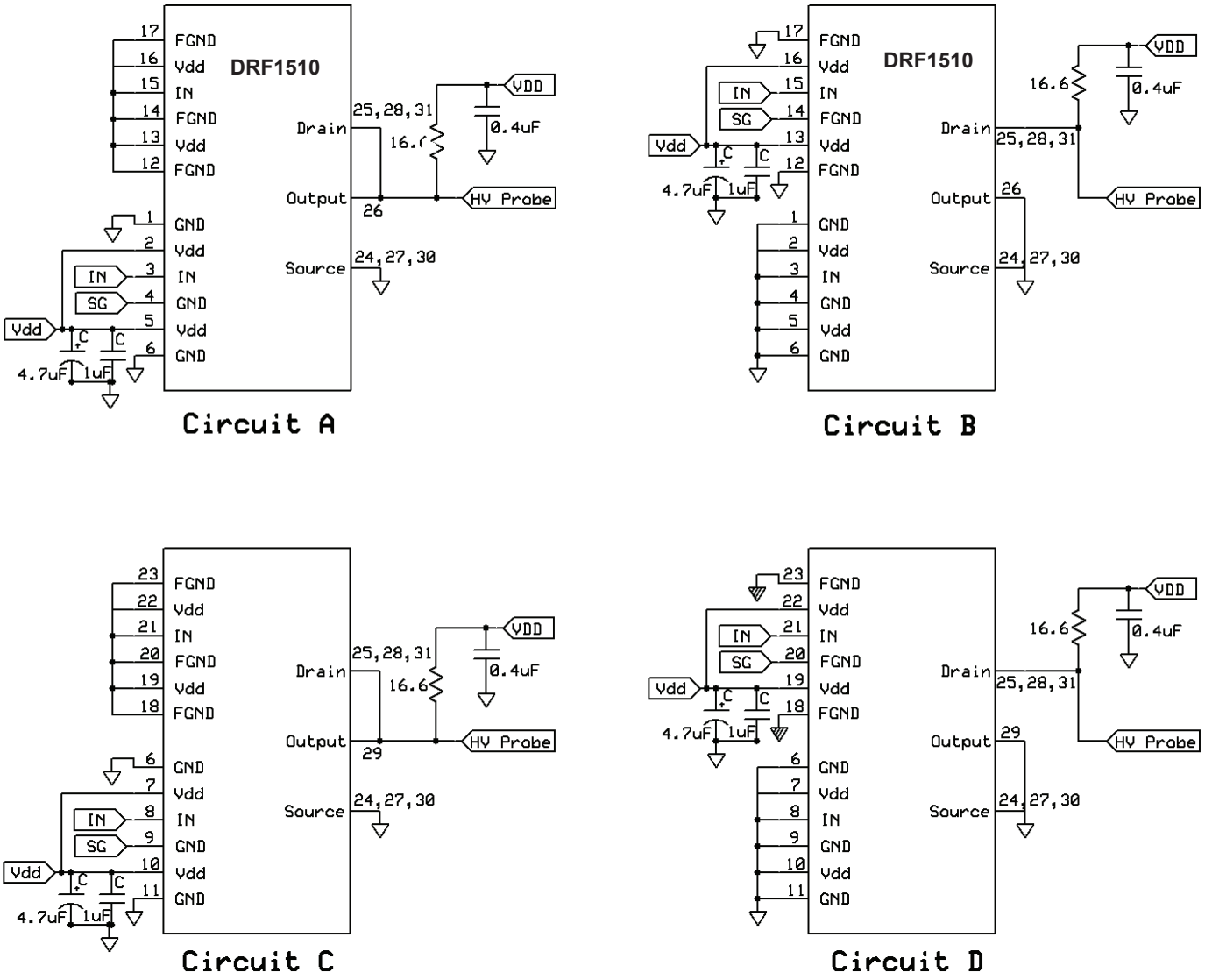

Figure 2, DRF1510 Test Circuit

The DRF1510 Test Circuits illustrated above are **for reference only**. These four circuits allow each of the sections in the Full Bridge to be tested independently. CKT A, C is configured to test the lower or negative supply section of the DRF1510 and CKT B, D is configured to test the upper or positive supply section. This method ties all pins of the unused section to the output CKT A , C or the ground CKT B, D. The internal sub circuit Test Configurations are shown below for the four test circuits above, A for A, B for B and C for C.

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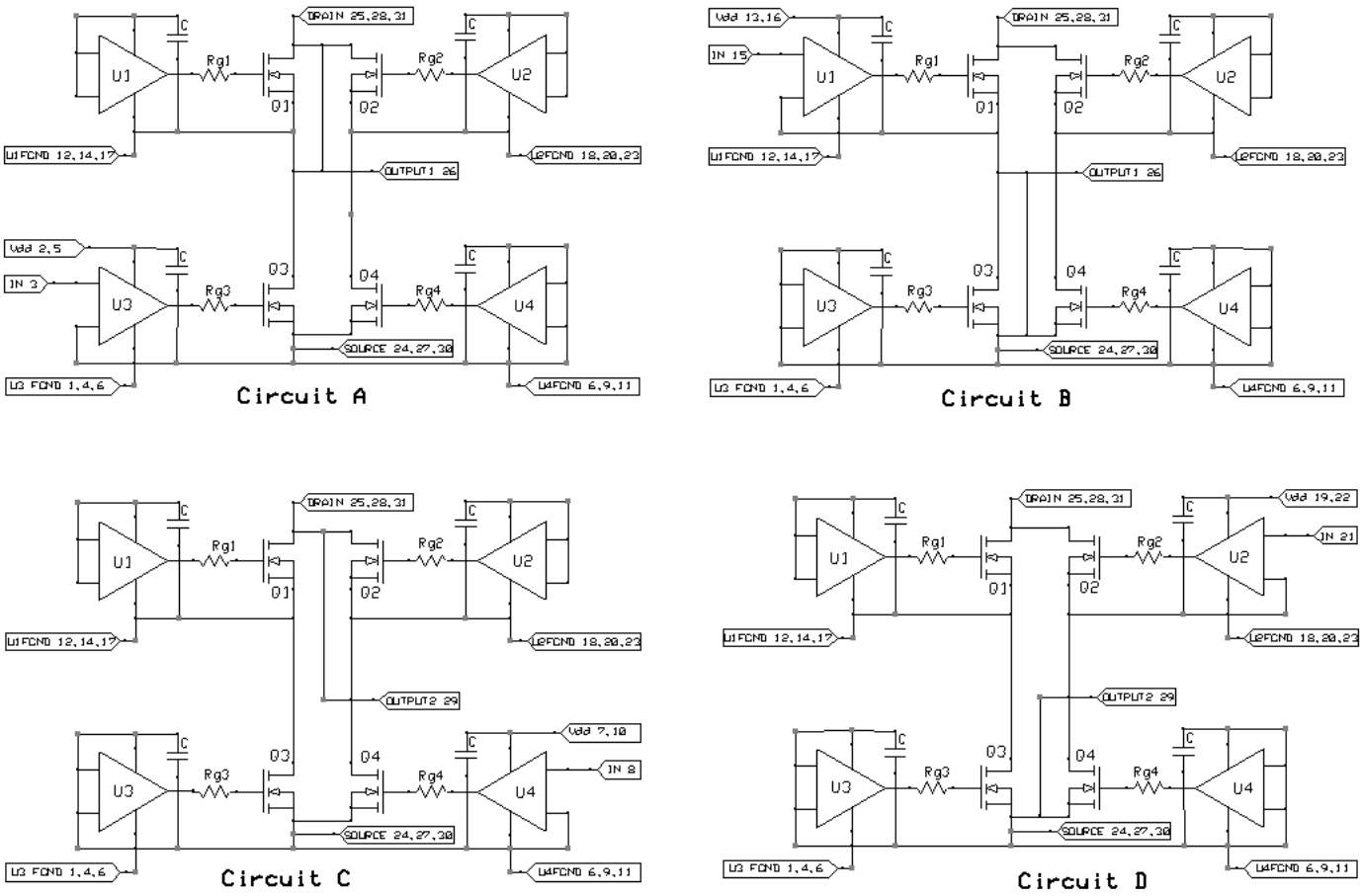

Figure 3, DRF1510 Test Configurations

The DRF1510 Test configurations illustrated above are **for reference only**.

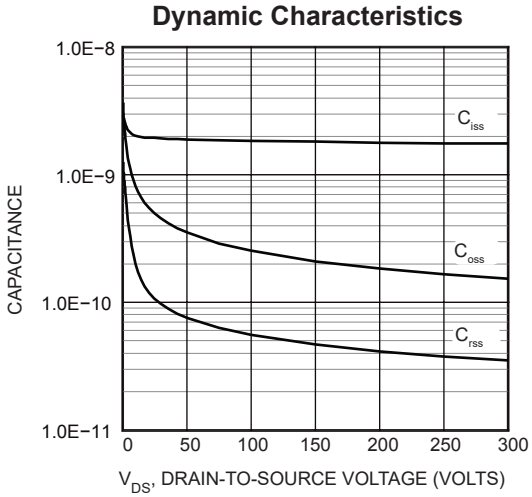

Figure 4, Typical Capacitance vs. Drain-to-Source Voltage

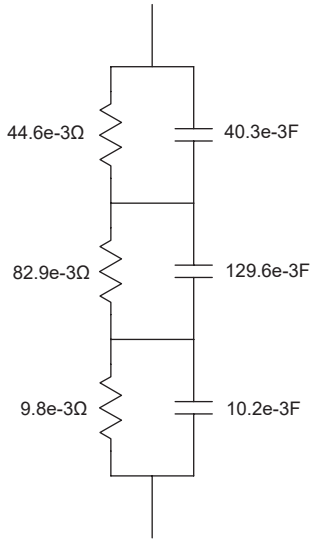

Figure 5a, Transient Thermal Impedance Model

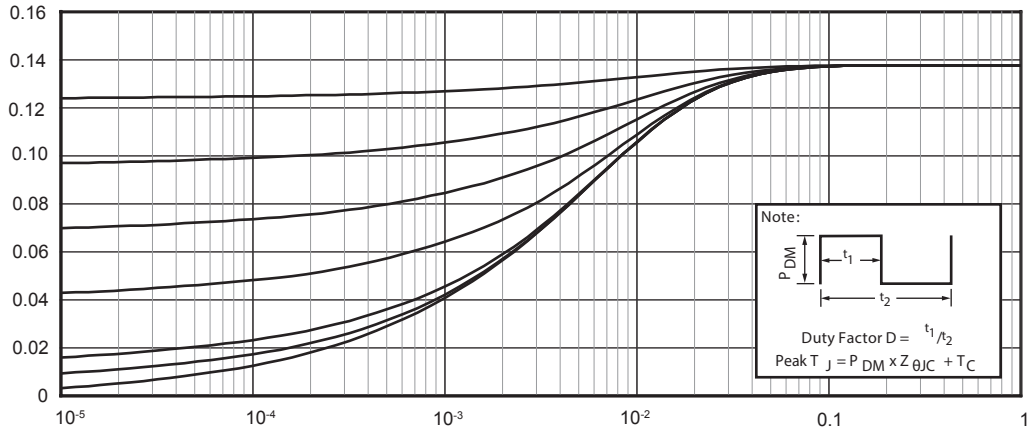

Figure 5, Thermal Impedance Model and Effective Transient Thermal Impedance, Junction -To-Case vs Pulse Duration

DRF1510 Pin Assignments			
Pin 1	PGND_Low Side 1	Pin 17	FGND_High Side 1
Pin 2	Vdd_Low Side 1	Pin 18	FGND_High Side 2
Pin 3	IN_Low Side 1	Pin 19	Vdd_High Side 2
Pin 4	PGND_Low Side 1	Pin 20	FGND_High Side 2
Pin 5	Vdd_Low Side 1	Pin 21	IN_High Side 2
Pin 6	PGND	Pin 22	Vdd_High Side 2
Pin 7	Vdd_Low Side 2	Pin 23	FGND_High Side 2
Pin 8	IN_Low Side 2	Pin 24	Source
Pin 9	PGND_Low Side 2	Pin 25	Drain
Pin 10	Vdd_Low Side 2	Pin 26	Output 1
Pin 11	PGND_Low Side 2	Pin 27	Source
Pin 12	FGND_High Side 1	Pin 28	Drain
Pin 13	Vdd_High Side 1	Pin 29	Output 2
Pin 14	FGND_High Side 1	Pin 30	Source
Pin 15	IN_High Side 1	Pin 31	Drain
Pin 16	Vdd_High Side 1	**FGND: Floating Ground / PGND: Power Ground**	

HAZARDOUS MATERIAL WARNING: The ceramic portion of the device is beryllium oxide. Beryllium oxide dust is highly toxic when inhaled. Care must be taken during handling and mounting to avoid damage to this area. These devices must never be thrown away with general industrial or domestic waste. BeO substrate weight: 5.1g. Percentage of total module weight which is BeO: 32%.

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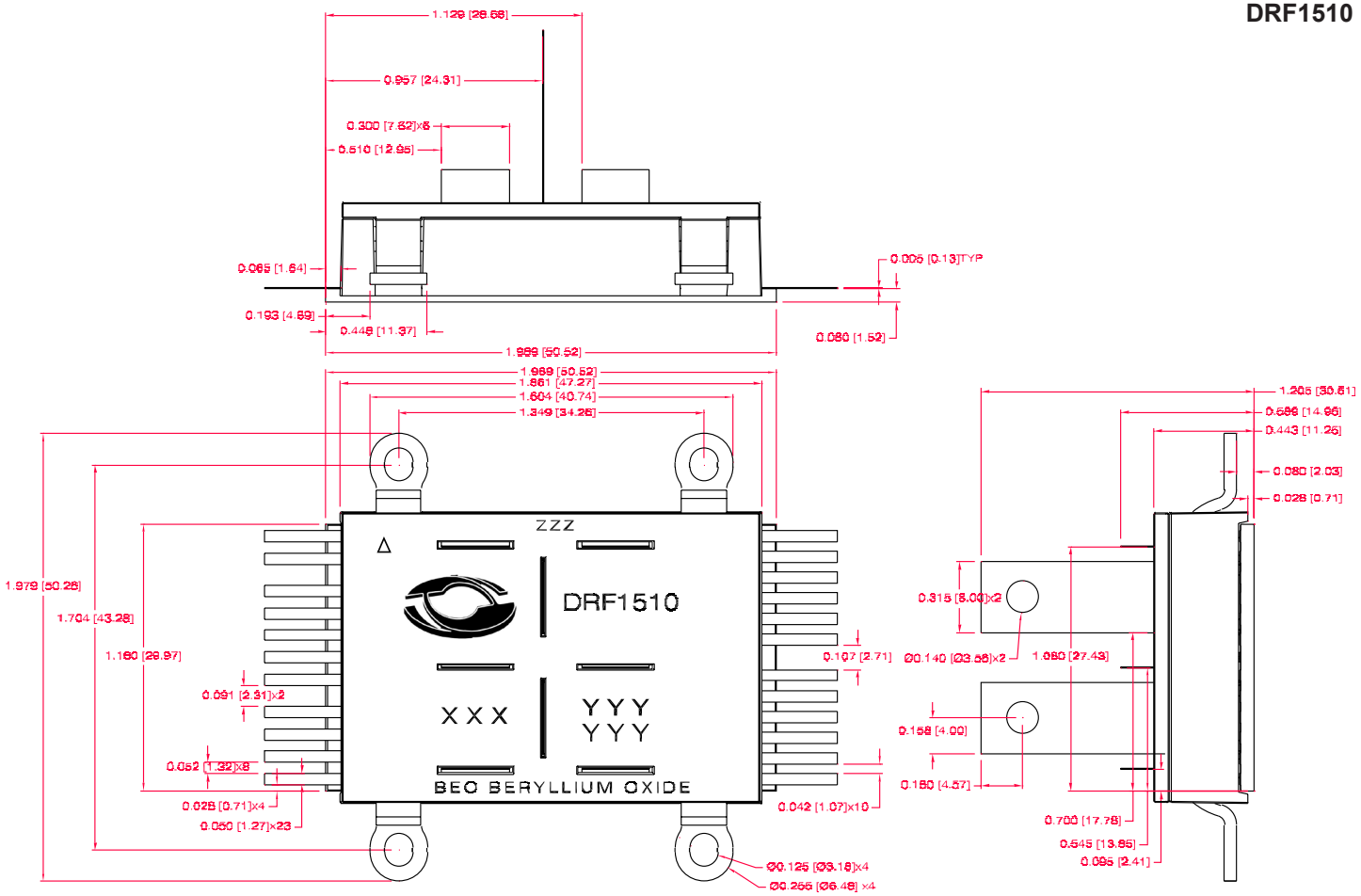

Figure 6, DRF1510 Mechanical Outline
Dimensions are in inches (± 0.008) and mm in brackets
Package withstand voltage 2500V

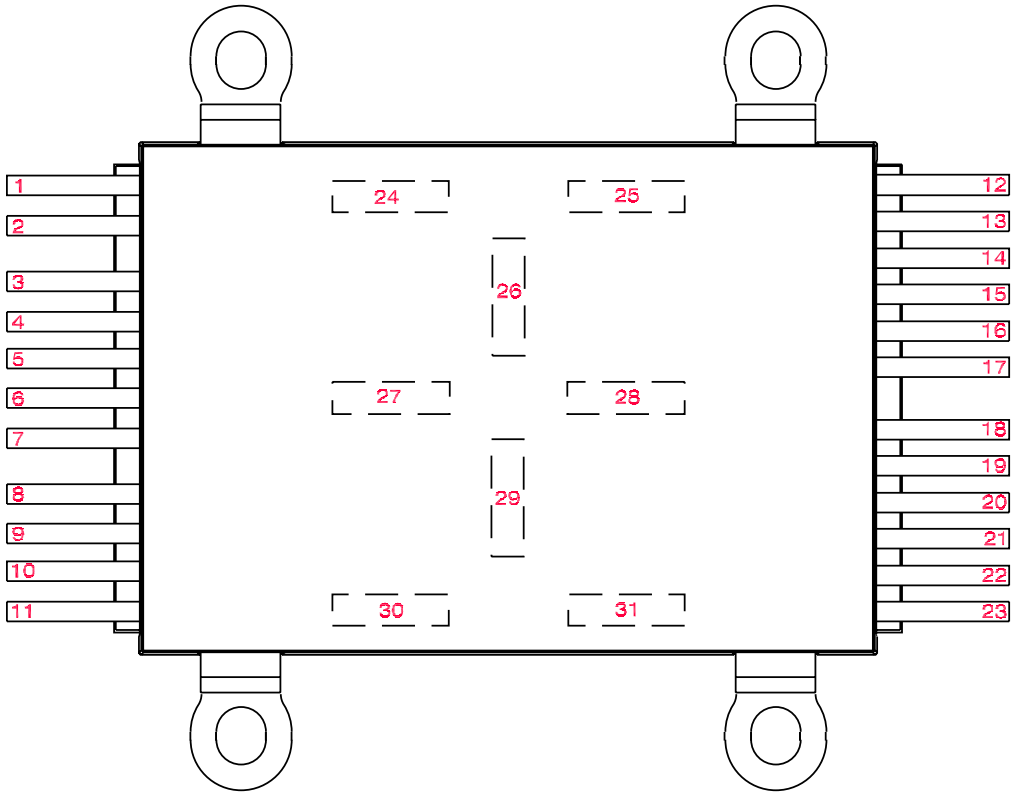

Figure 7, DRF1510 Pin Call Out

Disclaimer:

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