



Classical Constraint Flow for SmartFusion[®] 2, IGLOO[®] 2, and RTG4[™] Devices

Introduction

Block Flow is a bottom-up design methodology that enables you to use design blocks (“components” in generic terms) as building blocks for your top-level design. These building blocks may have already completed layout and been optimized for timing and power performance for a specific Microchip device. Using these blocks as part of your top-level design can cut down design time as well as improve timing and power performance. Using blocks has the following advantages:

- Helps you focus on the timing of critical blocks and ensure the timing across the blocks meets requirements before proceeding to integrate your blocks at the top-level.
- Helps re-using blocks without re-optimization for timing closure; changes in other blocks have no impacts.
- Helps re-using blocks in multiple designs.
- Allows shorter verification time.

Blocks can be used in the following scenarios:

- You have multiple team members working on different parts of the same design.
- The design is congested (uses 90% or more of the resources on a given die).
- You have difficulty in meeting timing by doing the design in its entirety. Blocks enable you to compartmentalize the design and optimize sections before you optimize the entire design.
- You want to re-use some elements of your design.
- You want to use the identical elements multiple times in a single design.
- You want to make small changes in your design and expect to keep most of the design unchanged with ensured performance.

You cannot use blocks with all families, they are family and die specific. If your block has I/Os, it is also package specific.



Important: The classical block flow user guide is applicable for v 11.8.

Features

The key features of blocks are:

- A block can be synthesized, simulated, and place-and-route in the same way as a regular design.
- The place-and-route of the block can be locked to ensure repeatable performance.
- Performance, placement, and routing can be fixed absolutely; however these rules can be relaxed gradually, if necessary, to ensure that you can integrate the block into your top-level project.
- The block flow supports the following HDLs:
 - Verilog
 - VHDL

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- The block flow supports SynplifyPro synthesis tool.
 - Nested blocks (blocks instantiated inside other blocks) are supported. When publishing, only one file will be published that contains all the required information (including the nested block).

Table of Contents

Introduction.....	1
Features.....	1
1. Creating Blocks - Options and Settings.....	5
1.1. Synthesis Tool Settings.....	5
1.2. Compile.....	5
1.3. Guidelines for Creating Blocks.....	6
2. Instantiating Blocks in your Top-Level Design.....	9
2.1. Import the Block.....	9
2.2. Create a Top-Level Design that Uses Blocks.....	9
3. Publishing Blocks After Compile or Layout.....	11
3.1. Publish After Compile.....	11
3.2. Publish After Layout.....	11
3.3. Published Content.....	11
4. Hierarchical Structure Resolution in Top-Level Projects.....	12
4.1. Duplicate Block Definition.....	12
4.2. Conflicting Definitions in top.v and Your Imported Block File.....	12
4.3. Resolving top.v and Block Instantiations.....	12
5. EDIF Netlist in the Top-Level Design.....	13
6. Synthesis.....	14
7. Resolving Place and Route Conflicts.....	15
7.1. Resolving Place and Route Conflicts in Compile.....	15
7.2. Compile - SmartFusion2, IGLOO2, and RTG4.....	15
8. Block PDC Commands.....	18
8.1. move_block.....	18
8.2. set_block_options.....	19
9. Publish Block - Configuration Options.....	21
9.1. Publish Block Configuration.....	21
9.2. Publish Options/Settings.....	21
10. Revision History.....	22
Microchip FPGA Support.....	23
Microchip Information.....	23
The Microchip Website.....	23
Product Change Notification Service.....	23
Customer Support.....	23
Microchip Devices Code Protection Feature.....	23
Legal Notice.....	24
Trademarks.....	24

Quality Management System.....	25
Worldwide Sales and Service.....	26

1. Creating Blocks - Options and Settings

Blocks can be created for a new as well as for the existing projects:

New Project

To enable **Block Creation** for a new project, go to **Project > New Project**. Check the **Enable Block Creation** check box.

Existing Project

To enable **Block Creation** for an existing project, go to **Project > Project Settings**. Click **Design Flow** and check the **Enable Block Creation** check box.

1.1 Synthesis Tool Settings

In SynplifyPro, the **I/O Insertion** option is disabled when the block is synthesized.



Important: Libero® automatically disables **I/O Insertion** for you before invoking SynplifyPro.

1.2 Compile

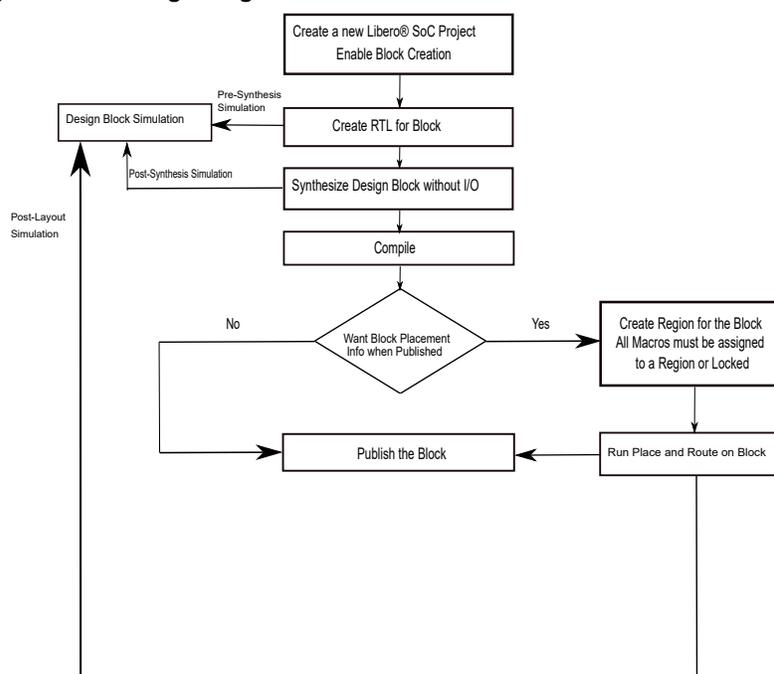
During compile, Libero SoC software adds `BLOCK_INTERFACE_I*` instances to the block. These instances are virtual buffers added to:

- Improve timing values for the block
- Provide a clear interface to floorplan
- Help with clustering constraints



Important: The `BLOCK_INTERFACE_I*` instances are removed when the block is published.

Figure 1-1. Creating and Publishing Design Blocks



1.3 Guidelines for Creating Blocks

Few guidelines for creating blocks are to check on the number of globals allowed, DRC rules, floorplanning, and architecture limitations.

1.3.1 Macros/IPs Not Supported in Blocks

The following macros are not allowed when creating a block for instantiation in a top-level design:

- MSS
- SERDESIF
- FDDR
- FLASH_FREEZE
- SYSRESET
- UJTAG
- μPROM

1.3.2 Synthesis Tool and Global Management

The synthesis tool may promote all clocks to global. The number of globals in your top-level design should be same as number of globals allowed in the device (8 or 16 depending on the device size) you are targeting. You may need to reduce or limit the number of globals in your block by adding row global or plan to share globals in the top-level design with the block. Add a row global, directly to your HDL (RCLKINT).

1.3.3 Blocks and Design Rule Check (DRC)

Based on the regular Libero design flows, DRC rules are applied to the blocks. For example, some DRC rules assume that some pins must be connected to the power nets. These rules are enforced on the blocks in the block flow just as in the regular design flow.

1.3.4 Blocks and Floorplanning

When creating a block, floorplanning is essential if you plan to publish placement information. Before running layout on the block, you must floorplan the design block. Use Libero's MultiView Navigator (MVN) or PDC commands for floorplanning.

If you do not create a region and constrain the block to the region (floorplanning) or lock the macros before place and route, a warning message appears when you publish the block. It warns you that not all macros in the block have been constrained to regions or locked and therefore your design netlist is only exported when the block is published.

1.3.4.1 Block Features in MVN

Following are the block features in MVN:

- **Block Ports Tab:** Lists all the ports in a design block even if they are not connected to I/Os.
- **Interface Instances in Design Block (Active Lists, Tools > Active List > Interface Instances):** Lists all macros connected to ports. These macros must be placed on the boundary of your block region, as they will be connected to the <top> design.
- **Block content available when you instantiate a Block in the <top> design (Tools > Active List > Designer Block Content):** Lists all macros in the block.
- **Block Tab:** Lists all the blocks in your design.
- **Search Support:** Enables you to find a specific block in your design.

1.3.4.2 Floorplanning with MVN

Following are the steps for floorplanning with MVN:

1. Create a new region. In the **Design Flow** tab, right click **Floorplan Constraints** and choose **Open Interactively** to open **ChipPlanner**.
2. From the **Region**, menu choose **Create Inclusive/Exclusive**.
3. Assign and constrain all your block macros to this region.
 - Click and drag to create a region.
 - Select all instances except the `BLOCK_INTERFACE_I*` instances added by Libero.
 - Right click and choose **Assign all Instances**.
 - From the **File** menu, choose **Commit and Check**.
4. Create a separate region; it must be outside the region created in the preceding steps. Assign and constrain all the `BLOCK_INTERFACE_I*` instances (added by Libero) to this separate region. Use the prefix `BLOCK_INTERFACE_I*` to search for all the block interface instances. Do not use exclusive regions for the block interface instances; they may limit the usage of the clusters in the top design.
5. Ensure that the new regions you created do not overlap with the existing regions.
6. From the **File** menu, choose **Commit and Check**.

1.3.4.3 Floorplanning with PDC Commands

Floorplanning reduces the risk of placement conflicts of the blocks at the top-level. If you do not constrain your block placement, its components may be placed anywhere on the die.

You can use the `define_region` PDC command to create a rectangular or rectilinear region, and then use the `assign_region` PDC command to constrain all the macros to that region. For details of command, see [Libero SoC v11.8 PDC Commands User Guide](#). Refer to the Libero Help for the `command syntax`.

It is also important to consider the placement of all block interface instances at the boundaries of block regions. This facilitates the interconnection of the block to the top-level design. If the block is highly optimized (densely packed), there may be no routing channels available to connect to any internal block interface instances. Placing all interfaces at block boundaries helps you eliminate routing congestion and failure.

1.3.5 Architecture Limitations - Managing Blocks and Globals

Architecturally, the silicon has 8 or 16 globals per device, depending on the device size. If you create a block used in the top level design that uses the maximum number of globals close to the device, then it is a good practice to minimize the number of globals when you create the block.

Examine the global report to see the number of globals that been used for the block. To reduce the number of globals used in the block, you may consider clock sharing and the use of row global for the block.

To add an internal global on a port, use either the Synplify constraints editor (SCOPE) or an SDC file.

To add a CLKINT after a CLK port, the command is: `define_attribute {n:CLK}`
`syn_insert_buffer {CLKINT}`.

2. Instantiating Blocks in your Top-Level Design

You can instantiate multiple instances of the same block or multiple blocks in the top-level design. Microchip recommends that you create a new project for your top-level design. To do so:

1. From the **Project** menu, choose **New Project**.
2. Deselect the **Enable Designer Block Creation** check box.
3. Choose the **Family/Die/Package** for the new project for the top-level as follows:
 - If the block is a netlist only and was not published with place and route information, choose the same **Family** as the block for the new project. Choose any **Die** and **Package**.
 - If the block contains placement information, choose the same **Family** and **Die** as the block for the new project, and choose any **Package**.
 - If the netlist contains I/O and Placement Information, choose the same **Family**, **Die**, and **Package** as the block for the new project.

2.1 Import the Block

Following are the steps to import a block:

1. From the **File** menu choose **Import > Blocks**.
2. Browse to the directory that contains your `<design_block_name>.cxz` file and select it.
3. Click **Open**.

`<design_block_name>` is imported into the `top_level` project. Version control is not supported for imported blocks. If you import the same block twice, the existing block is overwritten by the new one.

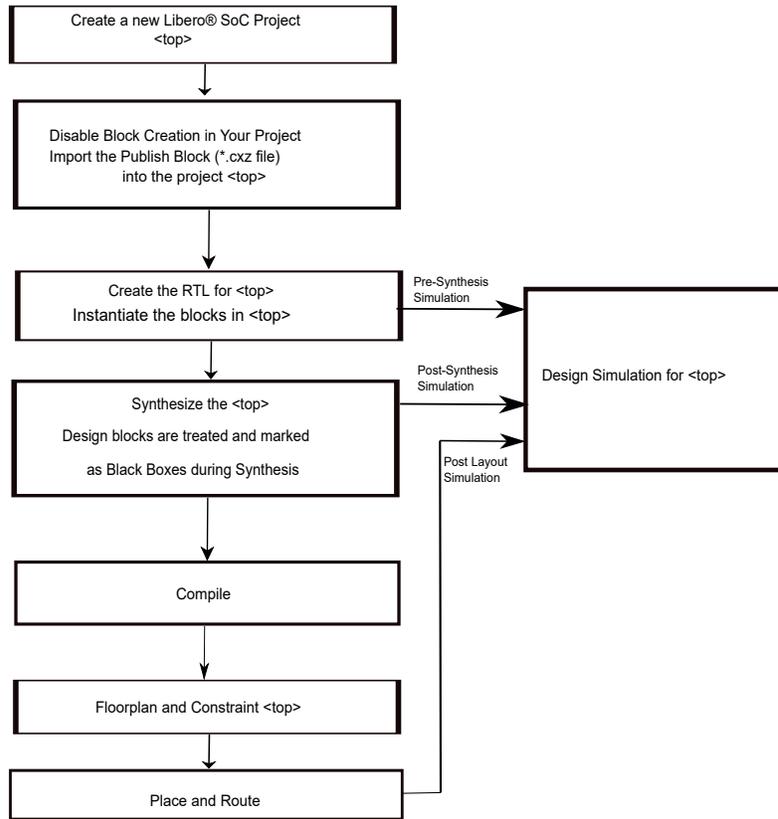
The files will be imported under `<design>\component\work\<design_block_name>`.

Review the files in the preceding directory to view block reports.

2.2 Create a Top-Level Design that Uses Blocks

Use SmartDesign or HDL to create your top-level design. If you use HDL, you can create HDL for the top-level or import a top-level HDL file.

Figure 2-1. Instantiating Blocks in your Top-Level Design



3. Publishing Blocks After Compile or Layout

You can publish your block after Compile or Layout.

3.1 Publish After Compile

If you publish a block after compile but before layout, a netlist is exported for the block when published. No place and route information or region constraint information is included in the block when published. A warning message appears when you publish a block before place and route.

3.2 Publish After Layout

If you publish a block after layout, the placement, routing and/or region constraint information will be published along with the netlist. You can always open the configurator and change the options to publish what you want. All macros must be locked or assigned to regions in order to publish the placement information.

3.3 Published Content

Libero exports the `<design>.cxz` file to `<project folder>/designer/<design_block_name>/export` folder when a block is published. The `<design>.cxz` file is a zip file that contains the following files:

- `<design_block_name>_syn.v` | `<design_block_name>_syn.vhd`: A timing shell file passed to synthesis tools when the top-level design is synthesized. The block is marked and treated as a black box when the top-level design is synthesized.
- `<design_block_name>_sim.v` | `<design_block_name>_sim.vhd`: A structural HDL netlist for post synthesis simulation of the block.
- `header_report.log`: A log file that contains header information on what and how a block is published, including the options you selected to configure the publication.
- `<design_block_name>_compile.xml`: Compile report detailing resource usage, device info, and a list of high-fanout nets.
- `<design_block_name>_gp_report.xml`: Global placement and routing report.
- `<design_block_name>_compile_netlist_combinational_loops.xml`: Combinational loops report.
- `<design>.cdb`: Internal proprietary file containing the optimized netlist, placement, routing or timing constraint information.

The `<design_block_name>.cxz` file is your published block. You can move it to another folder, transfer it to other team members, and so on. When you want to instantiate the block, you need to **Import >design_block_name> .cxz file** in your top level design.

4. Hierarchical Structure Resolution in Top-Level Projects

If you import multiple conflicting definitions for your *.v files, Libero resolves the conflicts.

4.1 Duplicate Block Definition

If you import two versions of your block file, you must choose which one you want to use. For example:

- Import `top.v` and `block1.v` files as HDL (**File > Import HDL Source Files**) into the top-level project.
- Import `<block1>` (**File > Import > Blocks**).

Libero recognizes a duplicate definition of `<block1>`; one from the HDL and another in the imported block file. The **Design Hierarchy** tab shows a `<block1>.cdf` and `<block1>.v` file under Duplicate Modules; Libero uses the HDL `<block1>` by default.

To override the default behavior and select the block definition, right click the `<block1>.cdf` file and choose **Use This File**. When you update the behavior, the block icon appears in the **Design Hierarchy**.

4.2 Conflicting Definitions in top.v and Your Imported Block File

You can introduce a conflict if you import a `top.v` file and a block file. Libero does not support HDL definition of low level blocks inside top-level HDL files and subsequent importing of block files. For example, the following scenarios cause an error:

- Import a `top.v` file (**File > Import HDL Source Files**) that contains a definition for `<top>` and a module definition for `<block1>`.
- Import the block `<block1>` (**File > Import > Blocks**).

Libero passes two duplicate files to your synthesis tool because the definition for `<block1>` is duplicated. To continue, you must remove the definition of `<block1>` from `top.v` and then re-import it.

4.3 Resolving top.v and Block Instantiations

Libero integrates your `top.v` file and block file if there is no definition for the block file in `top.v`. For example:

- Import your `top.v` (**File > Import HDL Sources Files**) that contains instantiations but no definition of `<block1>`.
- Import `<block1>` (**File > Import > Blocks**).

Libero resolves the hierarchy for you and puts `<block1>` under `top.v`.

5. EDIF Netlist in the Top-Level Design

If the top-level design is in EDIF, you must convert the EDIF to HDL and then import the HDL into Libero. To convert the top-level EDIF to HDL:

Write a Tcl script as follows:

```
set_device -fam SmartFusion2
read_edif -file {E:\top.edn}
write_verilog -file {E:\top.v} -skip_empty_modules 1
write_vhdl -file {E:\top.vhd}
## -skip_empty_modules 1 is to instruct the tool not to insert module
## definition for the empty modules in the HDL created.
```

From the Windows® Command Prompt or the Linux shell, run `rwnetlist` as follows (this executable is located in the same location as Libero):

```
rwnetlist --script "E:/run_export_netlist.tcl"
```

6. Synthesis

Libero passes the block timing to your synthesis tool when the top-level is synthesized. This timing shell enables the synthesis tool to produce more accurate timing numbers for top-level synthesis.

The timing shell also instructs the synthesis tool to treat the design block as a black box; this is done automatically - no action is required.

7. Resolving Place and Route Conflicts

To resolve place and route conflicts at the top-level:

- Examine the block compile report. Identify the cause of the problem and manually place and constrain the placement with MultiView Navigator or with PDC commands.
- If you instantiate a block (published with placement) multiple times, then placement between multiple block instances will overlap. To remove overlapping, move the block placement of one or more instances to another area using the PDC command `move_block`.
- The compiler enforces global sharing. If there is a global driving a CLKINT in the block, it will be deleted. Reduce the number of globals at the top-level by sharing global clock resources. Globals in the blocks may also be re-routed (not preserved).

7.1 Resolving Place and Route Conflicts in Compile

See [7.2. Compile - SmartFusion2, IGLOO2, and RTG4](#) for an explanation about the block conflict resolution options in compile.

7.2 Compile - SmartFusion2, IGLOO2, and RTG4

Compile contains a variety of functions that perform legality checking and basic netlist optimization. Compile checks for netlist errors (bad connections and fan-out problems), removes unused logic (gobbling), and combines functions to reduce logic count and improve performance. Compile also verifies that your selected device has sufficient resources to fit your design.

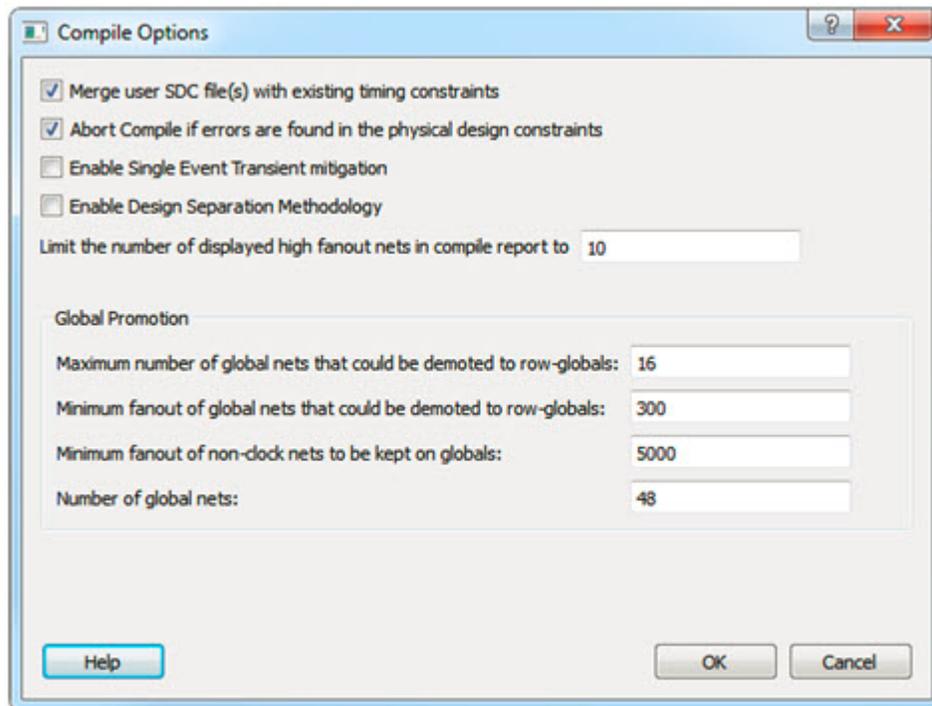
To compile your device with default settings, right click **Compile** in the Design Flow window and choose **Run**.

During compile, the Log window displays information about your design, including warnings and errors. Libero SoC issues warnings when your design violates recommended Microchip design rules. Microchip recommends that you address all warnings, if possible, by modifying your design before you continue.

If the design fails to compile due to errors, you must modify the design to remove the errors and re-compile.

To compile your design with custom settings, right click **Compile** in the Design Flow window and choose **Configure Options**.

Figure 7-1. Compile Options Dialog Box



7.2.1 Configure Options

The **Compile Options** dialog box enables you to control SDC file merge behavior, PDC error reporting, and limit the number of high fanout nets in the compile report.

7.2.1.1 Merge User SDC file(s) with existing timing constraints

Select **Merge User SDC file(s) with existing timing constraints** to preserve all existing timing constraints that you have entered using either the constraints editor or in a previously imported SDC file.

If you import new SDC files and you have this checkbox selected, the software merges the existing constraints and the constraints from the new SDC files. In case of a conflict, the new constraints have priority over the existing constraints.

This option is **ON** by default. When this option is **OFF**, all the existing timing constraints are replaced by the constraints in the newly imported SDC files.

7.2.1.2 Abort Compile if errors are found in the physical design constraints

Controls the compile flow behavior if errors are encountered in the PDC file. Select this option to stop the flow if any error is reported in reading your PDC file. If you deselect this option, the tool skips errors when reading your PDC file and reports them as warnings. The default is ON.

This option is useful if you do not wish to debug your PDC commands before you run Compile.



Tip:

- If there is a PDC command syntax error, the compile fails even if you deselect this option (for example, the command does not exist or the syntax of the command is incorrect)
- Every time you invoke this dialog box, this option is reset to its default value ON. This is to ensure that your PDC file is correct.

- **Enable Single Event Transient mitigation (RTG4 only)**

Controls the mitigation of Single Event Transient (SET) in the FPGA fabric. When this box is checked, SET filters are turned on globally to help mitigate radiation-induced transients. By default, this box is unchecked.

- **Enable Design Separation Methodology**

Check this box if your design is for security and safety critical applications and you want to make your design's individual subsystems (design blocks) separate and independent (in terms of physical layout and programming) to meet your design separation requirements. When checked, Libero generates a parameter file (`MSVT.param`) that details design blocks present in the design and the number of signals entering and leaving a design block. Microchip provides a separate tool, known as Microchip Separation Verification Tool (MSVT), which checks the final design place and route result against the `MSVT.param` file and determines whether the design separation meets your requirements.

- **Limit the number of displayed high fanout nets in compile report to**

The number of high fanout nets to be displayed is controlled using the **Limit the number of displayed high fanout nets**; the default value is 10. This means the top 10 nets with the highest fanout will appear in the **Compile Report**.

7.2.2 Global Promotion/Demotion Options

These options allow you to set the maximum/minimum values for promotion and demotion of globing routing resources.

- **Maximum number of globals that could be demoted to row-globals**

Specifies the maximum number of global nets that could be demoted to row-globals. The default is 16.

- **Minimum fanout of global nets that could be demoted to row-globals**

Specifies the minimum fanout of global nets that could be demoted to row-global. The default is 300. If you run out of global routing resources for your design, reduce this number (to allow more globals to be demoted) or select a bigger die for your design.

- **Minimum fanout of non-clock nets to be kept on globals**

Specifies the minimum fanout of non-clock (data) nets to be kept on globals (no demotion). The default is 5000. If you run out of globing routing resource for your design, increase this number or select a bigger die for your design.

- **Number of global nets**

The number of available global nets for the die is reported in this field. It varies with the die size you have selected for the Libero project.

7.2.3 Block Instantiation Compile Options

If there are multiple blocks instantiated in your top-level design, the software uses the Compile Options to resolve the conflicts. These options appear only if there are blocks in your design.

Placement Conflicts

- **Error if conflict:** Compile times out if any instance from a designer block is unplaced. This is the default option.
- **Resolve conflict:** Further categorized into three parts:
 - **Keep non-conflicting placement:** If some instances get unplaced for any reason, the remaining non-conflicting elements are preserved but not locked (you can move them).
 - **Keep and lock non-conflicting placement:** If some instances get unplaced for any reason, the remaining non-conflicting elements are preserved and locked.
 - **Discard placement from all blocks:** Placement information will be discarded from all blocks even if there is no conflict.

Routing Conflicts

There are three methods to resolve a conflict:

- **Error if conflict:** Compile times out due to an errors if any preserved net routing in a designer block is deleted.
- **Resolve conflict:** Further categorized into three parts:
 - **Keep non-conflicting routing:** If a nets' routing is removed for any reason, the routing for the non-conflicting nets is preserved but not locked (so that they can be rerouted). This is the default option.
 - **Keep and lock non-conflicting routing:** If the routing is removed for any reason, the remaining non-conflicting nets are preserved and locked; they cannot be rerouted. This is the default option.
 - **Discard routing from all blocks:** Routing information will be discarded from all blocks even if there is no conflict.

8. Block PDC Commands

`move_block` and `set_block_options` are two PDC commands available specifically for working with design blocks at the top-level.

Use the `move_block` and `set_block_options` commands to make changes in your top-level design.

In the top-level design, put the `move_block` and `set_block_options` commands in an NDC file (**Design Flow Window > Manage Constraints > Open Manage Constraints View > Netlist Attributes > New > Create New Compile Netlist Constraints NDC**) and associate the NDC file with synthesis.

8.1 move_block

PDC command; moves a block from its original, locked placement by preserving the relative placement between the instances. You can move the block to the left, right, up, or down.

```
move_block -inst_name instance_name -up y -down y -left x -right x -non_logic value
```

Argument

- inst_name instance_name** Specifies the name of the instance to move. If you do not know the name of the instance, run a Compile report or look at the names shown in the **Block** tab of the MultiView Navigator Hierarchy view.
- up y** Moves the block up the specified number of rows. The value must be a positive integer.
- down y** Moves the block down the specified number of rows. The value must be a positive integer.
- left x** Moves the block left the specified number of columns. The value must be a positive integer.
- right x** Moves the block right the specified number of columns. The value must be a positive integer.
- non_logic value** Specifies what to do with the non-logic part of the block if one exists.

The following table lists the acceptable values for this argument:

Table 8-1. Acceptable Values

Value	Description
move	Moves the entire block.
keep	Moves only the logic portion of the block (COMB/SEQ) and keeps the rest locked in the same previous location, if there is no conflict with other blocks.
unplace	Moves only the logic portion of the block (COMB/SEQ) and unplace the rest of it, such as I/Os and RAM.

Supported Families

The `move_block` PDC command supports the following families:

- SmartFusion2
- IGLOO2
- RTG4
- SmartFusion
- IGLOO

- ProASIC3Fusion
- Fusion

Descriptions

This command moves a block from its original, locked position to a new position.

You can move the entire block or just the logic part of it. You must use the `-non_logic` argument to specify what to do with the non-logic part of the block. You can find placement information about the block in the Block report. From the **Tools** menu in the designer software, choose **Reports > Block > Interface** to display the report that shows the location of the blocks.

The `-up`, `-down`, `-left`, and `-right` arguments enable you to specify how to move the block from its original placement. You cannot rotate the block, but the relative placement of macros within the block will be preserved and the placement will be locked. However, routing will be lost. You can either use the ChipPlanner tool or run a block report to determine the location of the block.

The `-non_logic` argument enables you to move a block that includes non-logic instances, such as RAM or I/Os that are difficult to move. Once you have moved a part of a block, you can unplace the remaining parts of the block and then place them manually as necessary.



Important: Microchip recommends to move the block left or right by increments of 12, and move the blocks up and down by increments of three. If not, placement may fail because it violates clustering constraints.

Exceptions

Following are the exceptions:

- You must import this PDC command as a source file, not as an auxiliary file.
- You must use this PDC command if you want to preserve the relative placement and routing (if possible) of a block you are instantiating many times in your design as only one instance will be preserved by default. To preserve other instances, move them using PDC command.

The following example moves the entire block (instance name `instA`) 12 columns to the right and 3 rows up: `move_block -inst_name instA -right 12 -up 3 -non_logic move.`

The following example moves only the logic portion of the block and unplaces the rest by 24 columns to the right and 6 rows up: `move_block -inst_name instA -right 24 -up 6 -non_logic unplace.`

8.2 set_block_options

PDC command; overrides the compile option for placement or routing conflicts for an instance of a block.

```
set_block_options -inst_name instance_name -placement_conflicts value -
routing_conflicts value.
```

Argument

- inst_name instance_name** Specifies the block instance name. If you do not know the name of the instance, run a block report (**Design > Reports > Blocks > Interface**) or look at the names shown in the **Block** tab of the **MultiView Navigator Hierarchy** view.
- placement_conflicts value** Specifies what to do when the software encounters a placement conflict.
- routing_conflicts value** Specifies what to do when the software encounters a routing conflict.

The following table lists the acceptable values for this argument:

Table 8-2. Acceptable Values

Value	Description
error	Compile times out due to an error if any route in any preserved net from a Designer block is deleted.
resolve	If a route is removed from a net for any reason, the routing for the non-conflicting nets is also deleted. Basically, if there are any conflicts, no routes from the block are kept.
keep	If a route is removed from a net for any reason, the routing for the non-conflicting nets is kept unlocked. Therefore, the router can re-route these nets.
lock	If routing is removed from a net for any reason, the routing for the non-conflicting nets is kept as locked, and the router will not change them. This is the default compile option.
discard	Discards any routing from the block, even if there are no conflicts.

Supported Families

The `set_block_options` PDC command supports the following families:

- SmartFusion2
- IGLOO2
- RTG4
- SmartFusion
- IGLOO
- ProASIC3Fusion
- Fusion

Descriptions

This command enables you to override the compile option for placement or routing conflicts for an instance of a block.

Guidelines

Observe the following guidelines:

- You must import this PDC command as a source file, not as an auxiliary file.
- If placement is discarded, the routing is automatically discarded too.

This example makes the designer software display an error if any instance from a block becomes unplaced or the routing is deleted: `set_block_options -inst_name instA -placement_conflicts ERROR -routing_conflicts ERROR.`

9. Publish Block - Configuration Options

To view this dialog box you must first Enable Block Creation in the **Libero SoC Project Settings** or **New Project Creation Wizard**. After **Block Creation** is enabled, **Publish Block** appears in the **Design Flow** window.

Expand **Publish Design**, right click **Publish Block**, and choose **Configure Options**.

9.1 Publish Block Configuration

Publish Placement: Check this box to publish the placement information for the block.



Important: Assign all macros to regions or lock them to publish placement.

If checked, the published block can be instantiated and used in a top-level design only with the same family and device. If the block contains I/Os, the published block can only be instantiated and used in a top-level design with the same family, device and package.

If unchecked, only a netlist is published for the block. The published block can be instantiated and used in a top-level design for any device and package in the same device family as the block.

Publish Routing: Check this box to retain the routing information with the block when published.

Publish Region: Check this box to retain the region constraint information with the block when published.

9.1.1 Language

Select your **Block Hardware Description Language**. The default is the **Preferred HDL** type set in your **Project Settings**.

9.2 Publish Options/Settings

Use the [9. Publish Block - Configuration Options](#) to configure the block for publication.

10. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	08/2022	<p>The following is the list of changes in revision A of the document:</p> <ul style="list-style-type: none">• The document was migrated to the Microchip template.• The document number was updated to DS50003361 from 502005262.• Updated: 1.3.1. Macros/IPs Not Supported in Blocks.

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ISBN: 978-1-6683-1099-1

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