DG0755
Demo Guide
PolarFire FPGA JESD204B Standalone Interface

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 11.0

Added Appendix 2: Running the TCL Script, page 32.

1.2 Revision 10.0

The following is a summary of the changes made in this revision.

- Updated the document for Libero SoC v12.2.
- Removed the references to Libero version numbers.

1.3 Revision 9.0

Updated the document for Libero SoC v12.0.

1.4 Revision 8.0

The following is a summary of the changes made in this revision.

- Updated the document for Evaluation and Splash kit.
- Updated the document for Libero SoC PolarFire v2.3.

1.5 Revision 7.0

The document was updated for Libero® SoC PolarFire v2.2.

1.6 Revision 6.0

The document was updated for Libero SoC PolarFire v2.1.

1.7 Revision 5.0

The following is a summary of the changes made in this revision.

- The document was updated to include IP core.
- Design Requirements, page 4 was edited to add CORERESET_PF details and Figure 3, page 6,JESD204B Interface Design, was updated with CORERESET_PF IP core.

1.8 Revision 4.0

The following is a summary of the changes made in this revision.

- The document is updated to include features and enhancements introduced in the Libero SoC PolarFire v2.0 release.
- Updated the GUI screens and COM port details with respect to the Libero SoC PolarFire v2.0 release.

1.9 Revision 3.0

The following is a summary of the changes made in this revision.

- The document was updated to include features and enhancements introduced in the Libero SoC PolarFire v1.1 SP1 release.
- Information about resource utilization was updated. For more information, see Table 5, page 18.
- List of reference was added. For more information, see Appendix 3: References, page 33.

1.10 Revision 2.0

The following is a summary of the changes in this revision.

- The document was updated for Libero SoC PolarFire v1.1 release.
- Information about resource utilization was added.

1.11 Revision 1.0

The first publication of this document.

2 PolarFire FPGA JESD204B Standalone Interface

This document describes the Microsemi JESD204B standalone interface design and how to run the demo on a PolarFire Evaluation or Splash kit.

The main components of the demo design are as follows:

- CoreJESD204BTX and CoreJESD204BRX IP cores implement the transmitter and receiver interfaces of the JESD204B standard. These IP cores are easy to integrate with the JESD204B-based data converters to develop high-bandwidth applications such as wireless infrastructure transceivers, software-defined radios, medical imaging systems, and radar and secure communications.They support link widths from x1 to x8, and link rates from 250 Mbps to 12.5 Gbps per lane using subclass 0, 1, and 2.
- PolarFire transceiver interface can handle data rates ranging from 250 Mbps to 12.5 Gbps. It integrates several functional blocks to support multiple high-speed serial protocols within the FPGA.

The design operates in the loopback mode by sending the CoreJESD204BTX data to the CoreJESD204BRX IP core through one or more transceiver lanes, which are looped back on the board. A user-friendly GUI is provided for selecting the input data and error injection, and for monitoring the JESD204B link status.

For Evaluation kit, two designs are provided as follows:

- SMA-based loopback design that runs at 6.25 Gbps lane rate (with single XCVR lane for TX and RX).
- PCB-based loopback design that runs at 5 Gbps lane rate (with two XCVR lanes, where one lane is for TX and the other for RX).

For Splash kit, PCB-based loopback design is provided that runs at 5 Gbps lane rate (with single XCVR lane for TX and RX).

For more information about the JESD204B interface design implementation, and all the necessary blocks and IP cores instantiated in Libero SoC, see Demo Design, page 5.

The JESD204B design can be programmed using any of the following options:

- **Using the job file:** To program the device using the job file provided along with the design files, see Appendix 1: Programming the Device Using FlashPro Express, page 29.
- **Using Libero SoC:** To program the device using Libero SoC, see Libero Design Flow, page 16. Use this option when the demo design is modified.

2.1 Design Requirements

The following table lists the resources required to run the demo:

Table 1 • **Design Requirements**

Requirement	Version
Operating System	Windows 7, 8.1, or 10
Hardware	
PolarFire Evaluation Kit (MPF300-EVAL-KIT)	Rev D or later
Or	
PolarFire Splash Kit (MPF300T-1FCG484)	Rev 2 or later
2 SMA-to-SMA cables (not provided with the kit) Optional: User can also test with on board loop back	Required only for Evaluation kit.
Software	
FlashPro Express	
Libero SoC	
ModelSim ME Pro	
SynplifyPro	

Note: Refer to the readme.txt file provided in the design files for the software versions used with this reference design.

2.2 Prerequisites

Before you begin:

1. Download and install Libero SoC (as indicated in the website for this design) on the host PC from the following location.
   https://www.microsemi.com/product-directory/design-resources/1750-libero-soc
   The latest versions of ModelSim and Synplify Pro are included in the Libero SoC installation package.

Note: A Libero Gold license is required to evaluate your designs on the MPF300 device.

2. Download the demo design files from the following location:
   For Evaluation Kit:
   http://soc.microsemi.com/download/rsc/?f=mpf_dg0755_eval_df
   For Splash Kit:
   http://soc.microsemi.com/download/rsc/?f=mpf_dg0755_spl_df

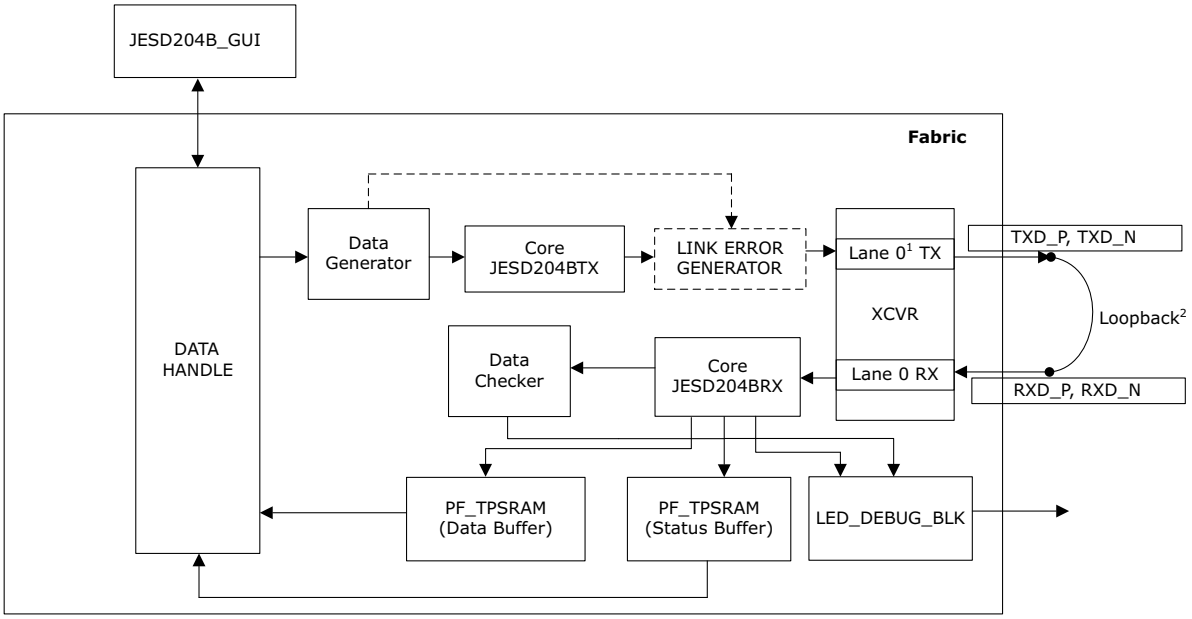
2.3 Demo Design

The PolarFire JESD204B demo design interfaces JESD204B compliant data converters with PolarFire devices. In this design:

1. The DATA_HANDLE_0 block interfaces with the GUI. The GUI enables the selection of PRBS or waveform input.
2. The DATA_HANDLE_0 block passes the input selection to the DATA_GENERATOR_0 block, which generates and sends the corresponding input data to the CoreJESD204BTX IP core.
3. The CoreJESD204BTX IP core performs the JESD204B transmitter functions based on the configuration, and sends the data to the PF_XCVR (transceiver) IP core.
4. The encoded data is received by the CoreJESD204BRX IP core because the TX and RX lanes of the PF_XCVR block are looped back. The CoreJESD204BRX IP core performs the JESD204B receiver functions based on the configuration, and sends the data to the GUI for viewing the selected input.
5. The JESD204B GUI displays data and status received from the JESD204BRX IP.

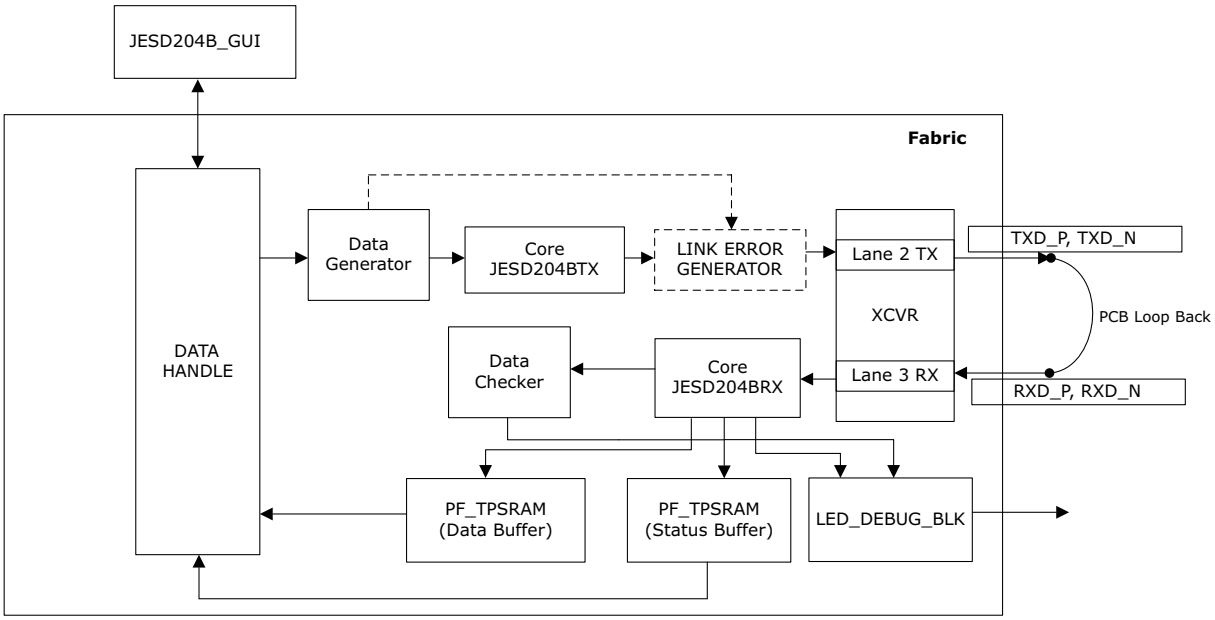
Note: When a data error or link error is selected on the GUI, the error generator block generates that error and displays it on the GUI.

Figure 1 • **SMA and PCB Loop Back (Evaluation and Splash kit) Block Diagram**



1. On SPLASH kit, Lane 1 is used.
2. On Evaluation kit the loopback is SMA-based. On SPLASH kit, the loopback is PCB-based.

Figure 2 • **PCB Loop Back (Evaluation kit) Block Diagram**

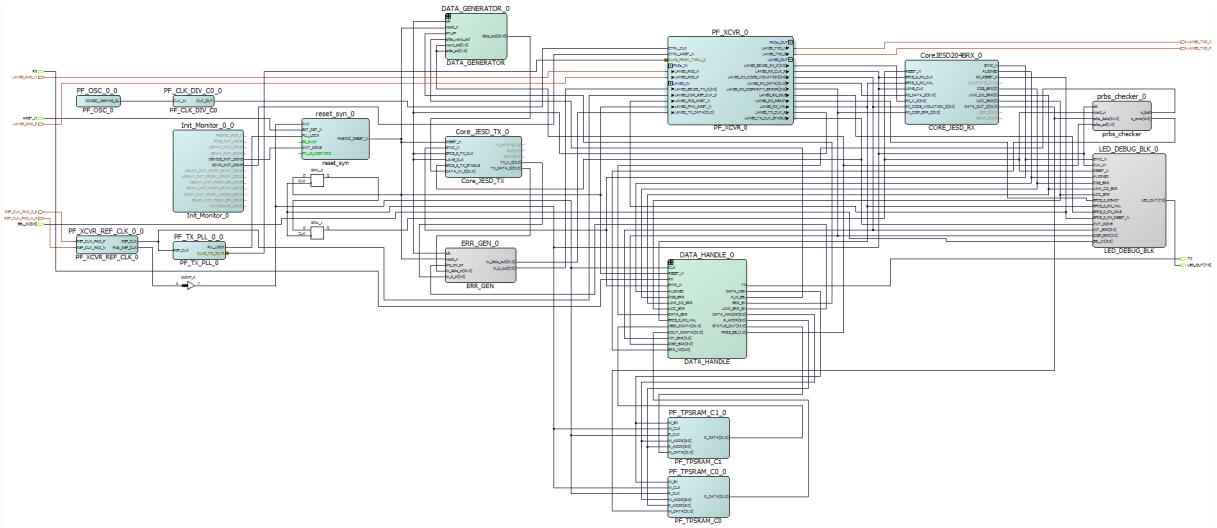


2.3.1 Design Implementation

This section shows the Libero design implementation, describes the IPs used and their configurations, and important input/output signals.

The following figure shows the design implementation of JESD204B interface in Libero:

Figure 3 • **JESD204B Interface Design**



Note: The Evaluation and Splash kit has the same designs, except for the transceiver configuration. For the latest SmartDesign, see the design files provided.

As shown in the figure, the design consists of the following parts:

- Transmit, page 7
- Receive, page 8

2.3.1.1 Transmit

The following IPs form the transmit part of the design:

1. **DATA_GENERATOR**— This block has a PRBS generator and a waveform generator. The PRBS generator generates PRBS7, PRBS15, PRBS23, and PRBS31 patterns. An error insertion mode implemented in the PRBS generator, inserts an error into the PRBS sequence. The waveform generator generates sine, sawtooth, triangle, and square waveforms. The data generator feeds the 64-bit test pattern to the JESD204BTX core, which then transmits data to the transceiver.
2. **CoreJESD204BTX**— This IP is the transmitter interface of the JEDEC JESD204B standard. For the SMA-based loopback design, the Core Configuration of this IP core is as follows:
   - Encoder: Removed
   - Data Width: 32
   - Serdes Mode: 1
   - Scrambling: Disabled
   - Device Subclass version: Disabled
   - JESD204 version: JESD204B
   - Number of Lanes:1
   - Number of octets per frame: 2
   - Number of frames for multi-frame: 9
   - Number of multi-frames in ILA sequence: 4

   The Link Configuration of CoreJESD204BTX is as follows:
   - Number of converters per device: 2
   - Converter resolution: 16
   - Total Number of bits per sample: 16
   - Number of samples per converter per frame cycle: 1

   For more information about CoreJESD204BTX, see *CoreJESD204BTX Handbook*.
3. **ERR_GEN_0**— This block generates link errors by sending random data between CoreJESD204BTX and PF_XCVR, when the link error generation is selected on the GUI.
4. **DATA_HANDLE_0**— This block receives the input data selection and link or data error generation information from the GUI. Also, the block sends the data output received from the CoreJESD204BRX core and the data or link status error to the GUI for viewing.
5. **PF_XCVR_ERM**— This is a hard IP block that supports high-speed data rates ranging from 250 Mbps to 12.5 Gbps. The following points summarize the configuration of the transceiver interface:

- For the SMA loopback design, the transceiver block (PF_XCVR) is configured in 8b10b mode with a CDR reference clock of 156.25 MHz to support 6.25 Gbps data rate. XCVR configuration settings are as follows:
  - Number of Lanes: 1; Enhanced receiver management: Enabled; Receiver calibration: None (CDR)
  - Transceiver data rate: 6.25 Gbps; TX clock division factor: 1; TX PPLL base data rate: 6.25 Gbps; TX PLL bit lock frequency: 3.125 Gbps
  - CDR Lock Mode: Lock to data; CDR reference clock source: Dedicated; CDR reference clock frequency: 156.25 MHz
  - PCS-Fabric interface width: 32-bit; 8b/10b Encoding/Decoding: Enabled
  - FPGA interface frequency: 156.25 MHz
- For PCB loop back demo, the transceiver block (PF_XCVR) is configured for two lanes in 8b10b mode with a CDR reference clock of 125 MHz to support 5 Gbps data rate.
  The PolarFire transmit PLL (PF_TX_PLL) is used to send the reference clock feed to the transceiver. The dedicated reference clock (PF_XCVR_REF_CLK) drives the PF_TX_PLL to generate the desired output clock for the 6.25 Gbps or 5 Gbps data rate.

Note: For the Splash kit design, XCVR is configured for the single lane in 8b10b mode with the 5 Gbps data rate.

2.3.1.2 Receive

The following IPs form the receive part of the design:

1. **CoreJESD204BRX**—This is the receiver interface of the JEDEC JESD204B standard. For the SMA-based loopback design, the Core Configuration of this IP core is as follows:
   - Decoder: Removed
   - Data Width: 32
   - Serdes Mode: 1
   - Scrambling: Disabled
   - Device Subclass Version: Subclass 0
   - JESD204 version: JESD204B
   - No. of Lanes (L+1): 1
   - Checksum calculation type: Octet
   - Frame Alignment Correction: Enabled
   - Link Configuration Error: Enabled
   - RAM Implementation: In FPGA Fabric

   The CoreJESD204BRX and CoreJESD204BTX IPs have the same Link configuration.For more information about CoreJESD204BRX, see *CoreJESD204BRX Handbook*.
2. **prbs_checker_0**— This block receives the 64-bit data from the CoreJESD204BRX IP core and checks if the received data is correct. It generates an error count and a status signal, which are sent to the GUI for status indication. The data checker checks only the PRBS sequences of the data generator.
3. **LED_DEBUG_BLK_0**— This block is used to debug the JESD204B link status and other errors. When the link is up, LEDs 4, 5, 6, 7, 8, 9 glow and LEDs 10 and 11 does not glow (with DIP 1, 2, 3, and 4 set low on the SW11 dip slide switch).

There are two instances of PF_URAM blocks, the PF_URAM_0 block stores the JESD204B link status before sending it to the GUI. The PF_URAM_1 block stores the data received from the CoreJESD204BRX before sending the data to the GUI.

PF_INIT_MONITOR and CoreReset_PF IPs handle the reset mechanism as summarized in the following points.

- When the DEVICE_INIT_DONE signal from Init_monitor block goes high, the transceiver is completely configured. This signal is anded with ARST_N signal to get proper reset signal for the design.
- CoreReset_PF synchronizes resets to the respective user-specified clock domain. This ensures that when the assertion is asynchronous, the deassertion is synchronous to the clock.

The following table lists the important I/O signals of the JESD204B design.

Table 2 • **I/O Signals of the JESD204B Design**

Signal	Description
Input Signals	
LANE0_RXD_P and LANE0_RXD_N	Receiver differential inputs of the transceiver
ARST_N	Reset signal obtained from the SW6 push-button switch on the board
RX	Receiver of UART interface
REF_CLK_PAD_P_0 and REF_CLK_PAD_N_0	Differential reference clock obtained from the on-board 156.25 MHz oscillator
SEL_IN[3:0]	Signal mapped to DIPs 1, 2, 3, and 4 of SW11 dip slide switch used to debug the status and errors
Output Signals	
LANE0_TXD_P and LANE0_TXD_N	Transmitter differential outputs of the transceiver
LED_OUT[7:0]	LEDs 4, 5, 6, 7, 8, 9, 10, and 11 on the board that indicate whether link is up or down
TX	Transmitter of the UART interface

2.4 Clocking Structure

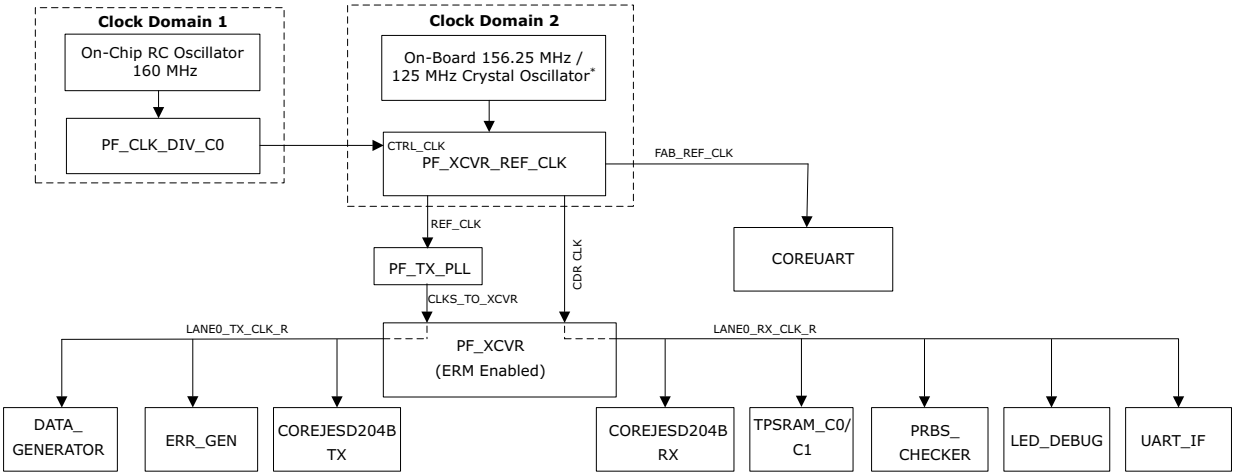
For the Evaluation kit design, the on-board 156.25 MHz crystal oscillator (for SMA loopback design) and the 125 MHz crystal oscillator (for PCB loop back design) drives the XCVR reference clock, which provides clock to the DATA_GENERATOR, CoreJESD204BTX, ERR_GEN, CoreJESD204BR, LED_DEBUG, PRBS_CHECKER, PF_TPSRAM_C0 and PF_TPSRAM_C1, COREUART, and UART_IF blocks.

For the Splash kit design, the on-board 125 MHz crystal oscillator drives the XCVR reference clock. The XCVR reference clock provides clock to the DATA_GENERATOR, CoreJESD204BTX, ERR_GEN, CoreJESD204BR, LED_DEBUG, PRBS_CHECKER, PF_TPSRAM_C0 and PF_TPSRAM_C1, COREUART, and UART_IF blocks.

An on-chip RC oscillator (PF_OSC) is used to drive the enhanced receiver management logic of the transceiver.

Note: If there is any change in the data rate or XCVR reference clock of the transceiver; reconfigure COREUART.

Figure 4 • **Clocking Structure**



*For Evaluation kit, 156.25 MHz oscillator is used for the SMA loopback design and 125 MHz oscillator is used for the PCB loopback design. For SPLASH kit, 125 MHz oscillator is used.

For the JESD204B design, LANE0_TX_CLK_R and LANE0_TX_CLK_R clocks are set to Regional (Deterministic) in the XCVR configurator.

The following table lists all of the clocks used in the design, their source, frequency, and purpose.

Table 3 • **Clocks**

Clock Name	Source	Frequency	Purpose
FAB_REF_CLOCK	Reference clock from the oscillator	156.25 MHz/125 MHz[1]	Clock for the fabric logic (UART)
REF_CLK	Reference clock from the oscillator	156.25 MHz/125 MHz[1]	CDR reference clock for the transceiver
LANE0_TX/RX_CLK_R	Transceiver generated TX/RX clock	156.25 MHz/125 MHz[1]	Clock for the transmit and receive modules in the fabric
CTRL_CLK	On-chip RC oscillator (PF_OSC)	40 MHz (through clock divider PF_CLK_DIV_C0)	Clock for the enhanced receiver management logic

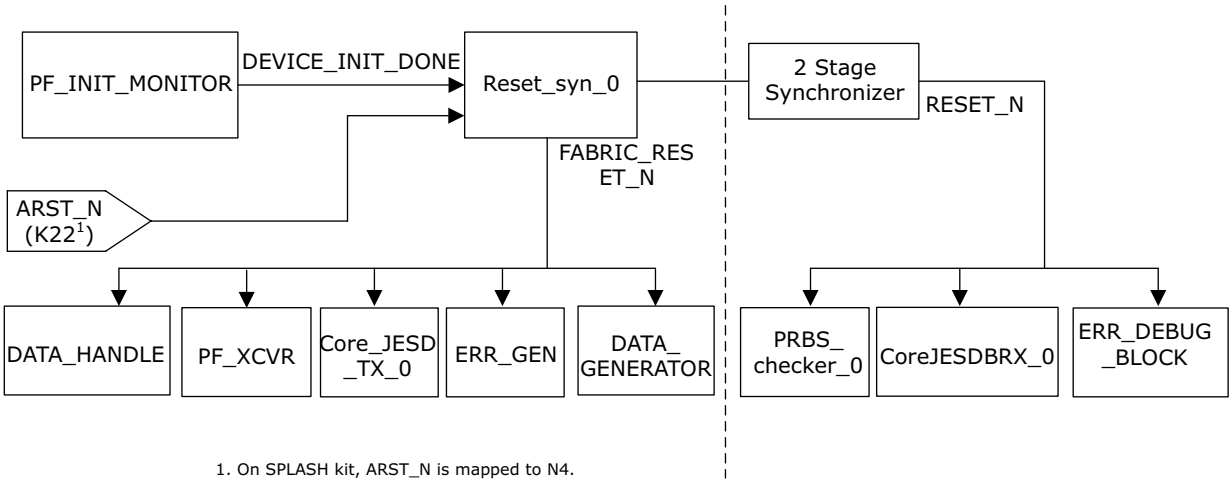
1. For SMA and PCB loopback designs (Evaluation kit), the frequency is 156.25 MHz and 125 MHz respectively. For the Splash kit design the frequency is 125 MHz.

2.5 Reset Structure

The DEVICE_INIT_DONE and the ARST_N signal mapped to K22 (evaluation board) and N4 (Splash kit) initiates the reset signal (FABRIC_RESET_N) from the res_syn_0 block, which synchronizes with the TX clock of the PF_XCVR block to reset the TX modules of the design.

A two-stage synchronizer (D Flip-Flop) synchronizes the reset of the RX modules with the RX clock of PF_XCVR. Figure 5 shows the reset structure.

Figure 5 • **Reset Structure**



1. On SPLASH kit, ARST_N is mapped to N4.

2.6 Simulating the PolarFire JESD204B Design

Before you begin:

1. Start Libero SoC and select **Project** -> **Tool Profiles...**.
2. In the **Tool Profiles** window, select **Synthesis** and **Simulation** on the **Tools** panes and select the latest active installation directory paths for these two tools.
3. In the **Project** menu, click **Open Project**.
   The **Open Project** dialog box opens.

Browse the design files folder,

`mpf_dg0755_eval_df\Libero_Project\External_loopback and Internal_loopback`, and select the `External_loopback\Libero_Project` folder and then select `Libero_Project.Prjx file. Similarly,` select the `Internal_loopback\Libero_Project` folder and then select `Libero_Project.prjx` file.

4. Click **Open**.
   The PolarFire JESD204B project opens in Libero SoC.

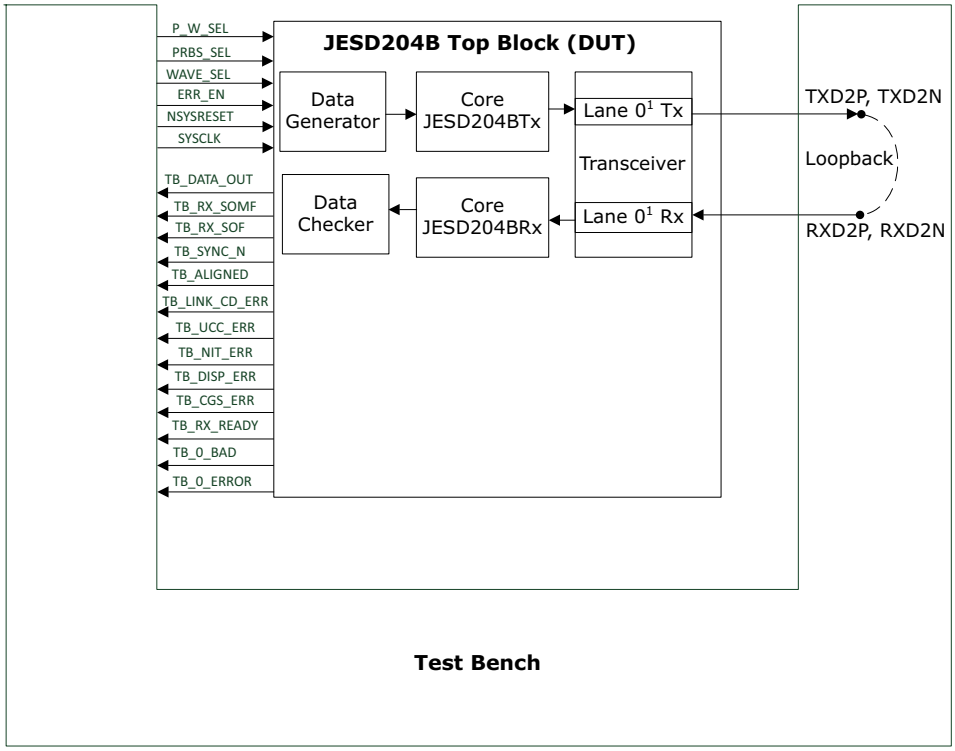
Note: To simulate the Splash kit design, browse the

`mpf_dg0755_spl_df\Libero_Project` folder.

5. Download the following IP cores from **Libero SoC** -> **Catalog**:
   - CoreJESD204BTX
   - CoreJESD204BRX
   - PF_XCVR
   - PF_TX_PLL
   - PF_XCVR_REF_CLK
   - PF_TPSRAM
   - COREUART
   - PF_INIT_MONITOR

A testbench is provided to simulate the JESD204B PRBS pattern and waveform selection. Figure 6 shows the interaction between testbench and the design.

Figure 6 • **Testbench and JESD204B Demo Design Interaction**



1. In the PCB loopback design for Evaluation kit , Lane 2 and 3 are looped back.

The testbench generates the test selection for the PRBS input (PRBS7, PRBS15, PRBS23, and PRBS31) and waveform input (sine wave, sawtooth wave, triangle wave, and square wave). It also monitors the JESD204B output status signals (SYNC_N, ALIGNED, and CGS_ERR) for the verification of JESD204B phases, and PRBS checker output status signals O_BAD and O_ERROR[4:0].

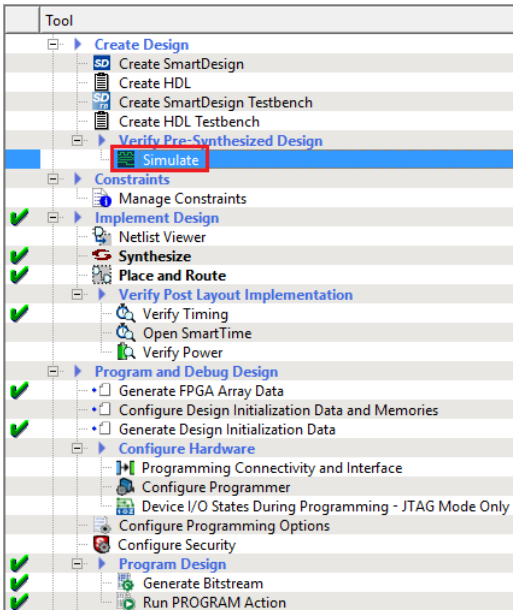
The following table lists the simulation signals.

Table 4 • **Simulation Signals**

Signal	Description
Input Signals	
P_W_SEL	Input to select the PRBS pattern or waveform
WAVE_SEL[1:0]	Input to select the type of waveform
PRBS_SEL[1:0]	Input to select the type of PRBS pattern
ERR_EN	Input to enable error in the PRBS pattern
NSYSRESET	Active low reset signal
SYSCLK	• 156.25 MHz generated clock for external loop back design • 125 MHz generated clock for internal loop back design
Output Signals	
TB_DATA_OUT	Output data from CoreJESD204BRX
TB_RX_SOMF	SOMF_0[3:0] signal received from the CoreJESD204BRX block
TB_RX_SOF	SOF_0[3:0] signal received from the CoreJESD204BRX block
TB_SYNC_N	SYNC_N signal, which indicates the link status
TB_ALIGNED	ALIGNED signal, which indicates that all transceiver lanes are aligned
TB_LINK_CD_ERR	LINK_CD_ERR[0] signal, which indicates a link configuration data mismatch error
TB_UCC_ERR	UCC_ERR[0] signal, which indicates an unexpected control character error
TB_NIT_ERR	NIT_ERR[3:0] signal, which indicates the “not in table” error. This signal is controlled by LANE0_RX_CODE_VIOLATION[3:0]
TB_DISP_ERR	DISP_ERR[3:0] signal which indicates the disparity error. This signal is controlled by LANE0_RX_DISPARITY_VIOLATION[3:0]
TB_CGS_ERR	CGS_ERR signal, which indicates the code group synchronization error. This signal is controlled by the CGS_ERR[0] signal.
TB_RX_READY	LANE0_RX_READY signal received from the transceiver block
TB_0_BAD	Error flag
TB_O_ERROR[4:0]	Number of errors occurred during PRBS check

In the **Design Flow** tab, under **Verify Pre-Synthesized Design,** double-click **Simulate** to simulate the design. The **Simulate** option is highlighted in Figure 7.

Figure 7 • **Simulating the Design**



When the simulation is initiated, ModelSim compiles all the design source files, runs the simulation, and configures the waveform viewer to show the simulation signals.

2.6.1 Simulation Flow

The following steps describe the JESD204B testbench simulation flow:

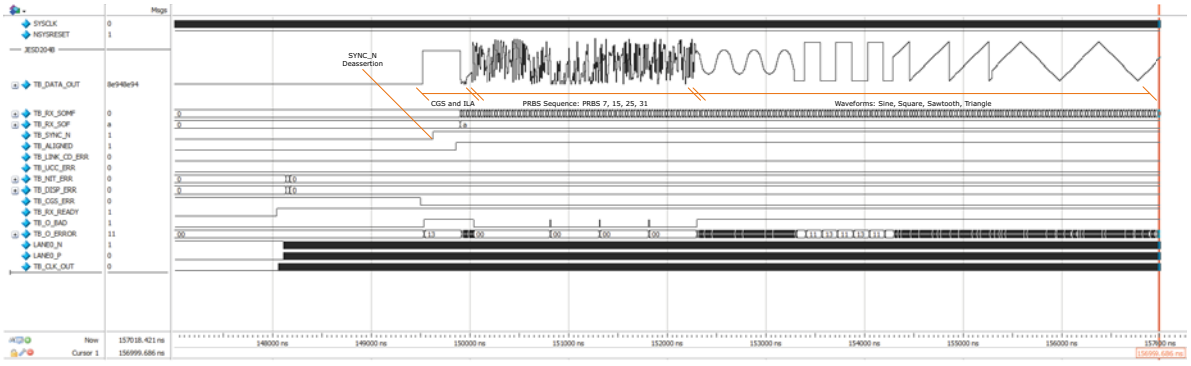
1. At the start, the NSYSRESET signal resets all of the components.
2. After the transceiver block is initialized, the TB_RX_READY signal is asserted high.
3. The JESD204BRX issues a synchronization request by driving the TB_SYNC_N pin low.
4. The JESD204BRX block checks the k28.5 characters transmitted by the JESD204BTX block.
5. The Code Group Synchronization (CGS) and ILA (Initial Lane Alignment) phase starts after the TB_SYNC_N signal is asserted high.
6. The testbench checks whether the CGS_ERR signal asserts low or not, and completes the CGS phase.
7. The JESD204BRX link asserts the TB_SYNC_N signal to high.
8. After the successful completion of the CGS phase, the JESD204BTX block starts the ILA sequence by transmitting four multi-frames in the following sequence:
   - First frame at TB_TX_SOMF = 0x8
   - Second frame at TB_TX_SOMF = 0x2
   - Third frame at TB_TX_SOMF = 0x8
   - Fourth frame at TB_TX_SOMF = 0x2
9. The JESD204BRX link starts receiving four multi-frames in the following sequence:
   - First frame at TB_TX_SOMF = 0x8
   - Second frame at TB_TX_SOMF = 0x2
   - Third frame at TB_TX_SOMF = 0x8
   - Fourth frame at TB_TX_SOMF = 0x2

   The ILA phase test passes if all JESD204BRX DATA_OUT is properly received with frame alignment.
10. After successful completion of the ILA phase, the JESD204BTX block enters in to the data phase.
11. In the data phase, the following data is fed to the JESD204BTX block:
    PRBS7, PRBS15, PRBS23, and PRBS31 using the PRBS generator.
12. Sine, Square, Saw, and triangular waves are generated from the waveform generator.
13. The data checker checks the received PRBS pattern against the expected PRBS pattern.
14. The waveform output can be viewed in the Simulation window on corresponding wave selection as shown in Figure 8.
15. If no error is detected by the data checker, the testbench issues a TESTBENCH PASSED message stating that the simulation was successful. If an error is detected, the testbench issues a TESTBENCH FAILED message to indicate that the testbench has failed.

While the simulation is running, you can see the status of the test cases in the **Transcript** window of ModelSim.

After simulation, the **Waveform** window displays the simulation waveforms as shown in the following figure.

Figure 8 • **Simulation Waveform Window**



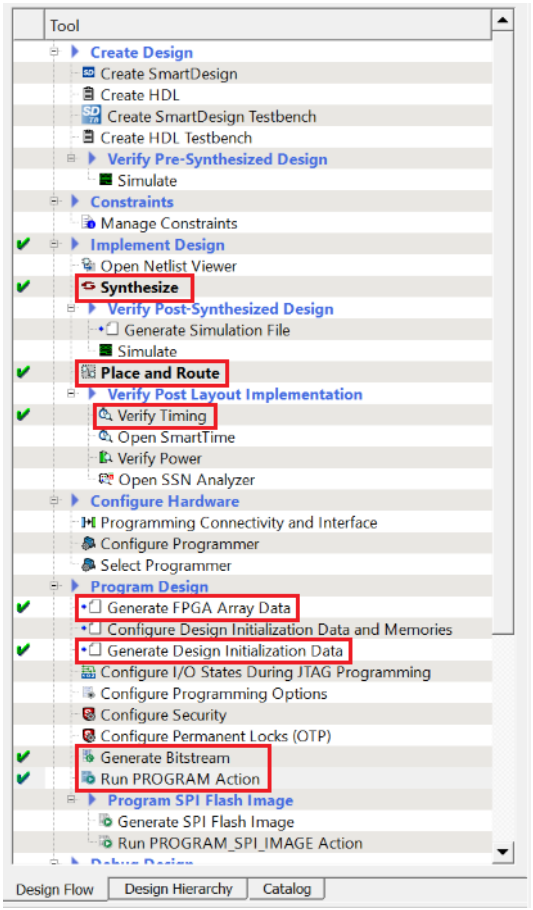
3 Libero Design Flow

This chapter describes the Libero design flow, which involves the following options:

- Synthesize, page 16
- Place and Route, page 17
- Verify Timing, page 19
- Generate Bitstream, page 19
- Device Programming, page 19

The following figure shows these options in the **Design Flow** tab.

Figure 9 • **Libero Design Flow Options**



3.1 Synthesize

To synthesize the JESD204B design, perform the following steps:

1. In the **Design Flow** tab, double-click **Synthesize**.
   When the synthesis is successful, a green tick mark appears as shown in the preceding figure.
2. Right-click **Synthesize** and select **View Report** to view the synthesis report and log files in the **Reports** tab.

3.2 Place and Route

For Evaluation kit SMA loopback design, the transceiver is placed in Quad 2, Lane 0 (as shown in Figure 10). For the PCB loopback design, the transceiver is placed in Quad2, Lane 2 and Lane 3 (as shown in Figure 11). For more information about the PolarFire Transceiver, see *UG0677: PolarFire FPGA Transceiver User Guide*.

For the Splash kit design, the transceiver is placed in Quad 1, Lane 1 as shown in Figure 12.

To place and route the JESD204B design, perform the following steps:

1. Use I/O Editor from Libero SoC -> Constraint Manager and place TX_PLL, XCVR_REF_CLK, and PF_XCVR as shown in Figure 10 or Figure 11.

Figure 10 • **I/O Editor XCVR View (SMA Loopback Design)**

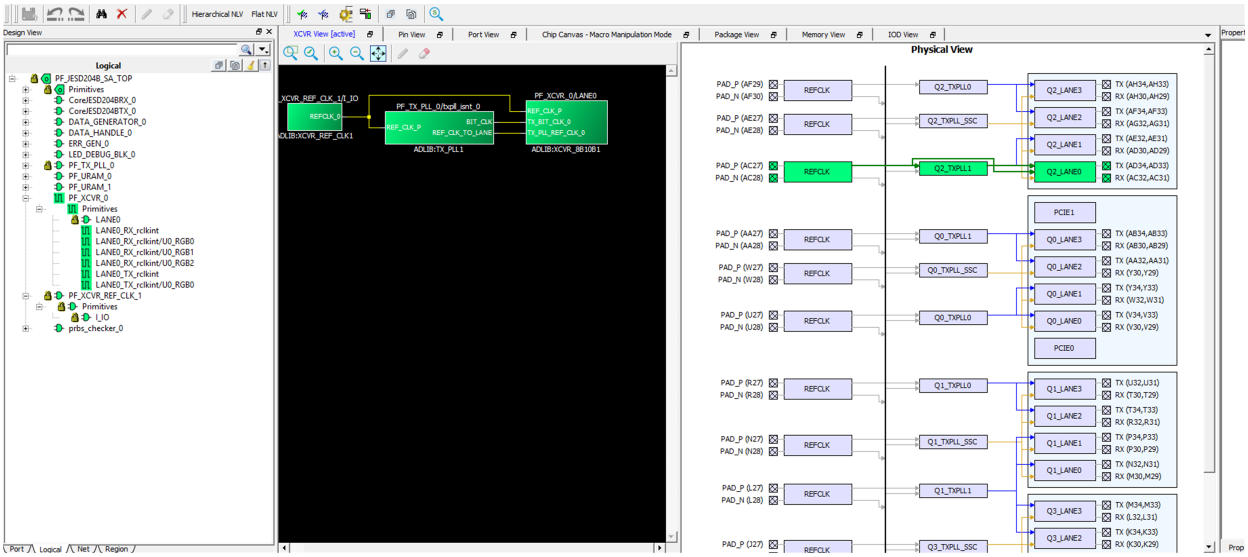


Figure 11 • **I/O Editor XCVR View (PCB Loopback Design)**

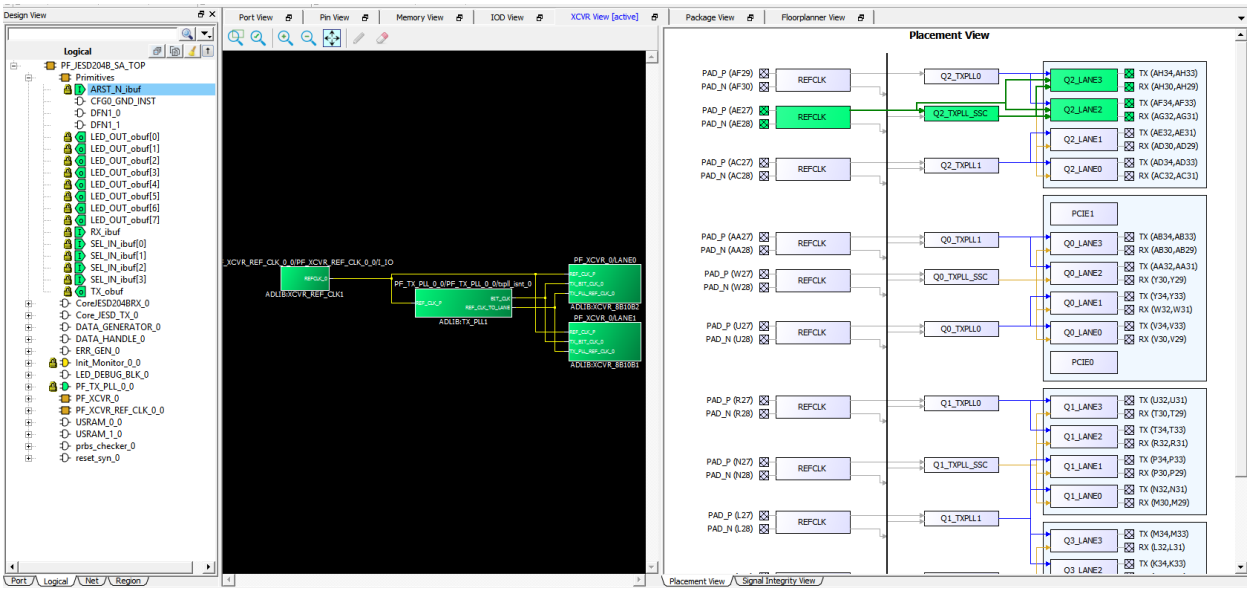
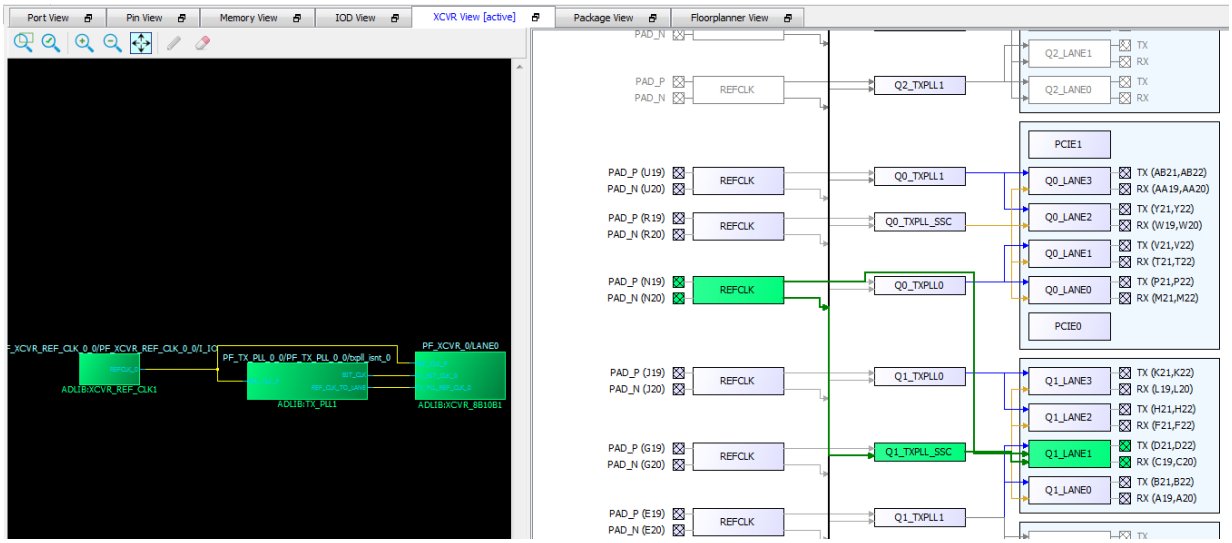


Figure 12 • **I/O Editor XCVR View (Splash Kit)**



2. Click **Save**. The PDC file required for placing and routing the design is generated.
3. In the **Design Flow** tab, double-click **Place and Route**.
   When place and route is successful, a green tick mark appears as shown in the Figure 9.
4. Right-click **Place and Route** and select **View Report** to view the place and route report and log files in the **Reports** tab.

3.2.1 Resource Utilization

The following tables list the resource utilization of the JESD204B loopback design after selecting place and route option. These values may vary slightly for different Libero runs, settings, and seed values. For IP-wise utilization, see the respective handbooks.

Table 5 • **Resource Utilization (SMA Loopback Evaluation Kit)**

Type	Used	Total	Percentage
4LUT	4226	299544	1.41
DFF	4091	299544	1.37
I/O Register	0	510	0.00
Logic Element	6362	299544	2.12

Table 6 • **Resource Utilization (PCB Loopback Evaluation Kit)**

Type	Used	Total	Percentage
4LUT	4299	299544	1.44
DFF	4171	299544	1.39
I/O Register	0	510	0.00
Logic Element	6435	299544	2.15

Table 7 • **Resource Utilization (Splash kit)**

Type	Used	Total	Percentage
4LUT	4197	299544	1.40
DFF	4088	299544	1.36
I/O Register	0	242	0
Logic Element	6321	299544	2.11

3.3 Verify Timing

To verify timing, perform the following steps:

1. In the **Design Flow** tab, double-click **Verify Timing**.
   When the design successfully meets the timing requirements, a green tick mark appears as shown in Figure 9.
2. Right-click **Verify Timing** and select **View Report** to view the verify timing report and log files in the **Reports** tab.

3.4 Generate Bitstream

To generate the bitstream, perform the following steps:

1. In the **Design Flow** tab, double-click **Generate Bitstream**.
   When the bitstream is successfully generated, a green tick mark appears as shown in Figure 9.
2. Right-click **Generate Bitstream** and select **View Report** to view the corresponding log file in the **Reports** tab.

3.5 Device Programming

After generating the bitstream, the PolarFire device must be programmed. To program the device, see any of the following sections based on the kit used.

- Programming the Device on Evaluation kit, page 20
- Programming the Device on Splash Kit, page 22

3.5.1 Programming the Device on Evaluation kit

To program the PolarFire device on Evaluation kit, perform the following steps:

1. Ensure that the jumper settings on the board are same as listed in the following table.

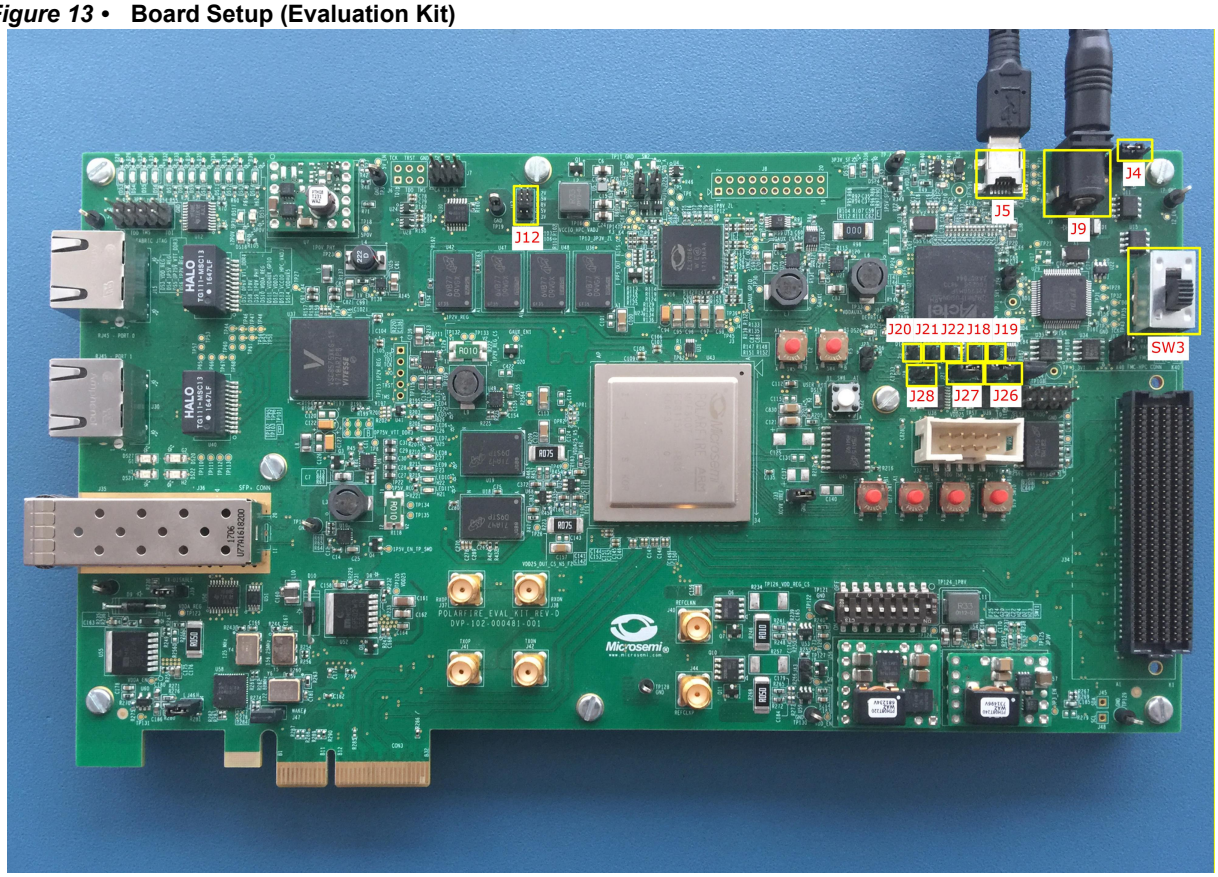
Table 8 • **Jumper Settings**

Jumper	Description
J18, J19, J20, J21, J22	Close pin 2 and 3 for programming the PolarFire FPGA through FTDI
J28	Close pin 1 and 2 for programming through the on-board FlashPro5
J26	Close pin 1 and 2 for programming through the FTDI SPI
J27	Close pin 1 and 2 for programming through the FTDI SPI
J4	Close pin 1 and 2 for manual power switching using SW3
J12	Close pin 3 and 4 for 2.5 V

2. Connect the power supply cable to the J9 connector on the board.
3. Connect the USB cable from the host PC to the J5 (FTDI port) on the board.
4. Power on the board using the **SW3** slide switch.
5. For external loop back demo, connect **TXN** to **RXN** and **TXP** to **RXP** using the 2 SMA to SMA cables as shown in the following figure.

The following figure shows the board setup for external loop back demo.

Figure 13 • **Board Setup (Evaluation Kit)**



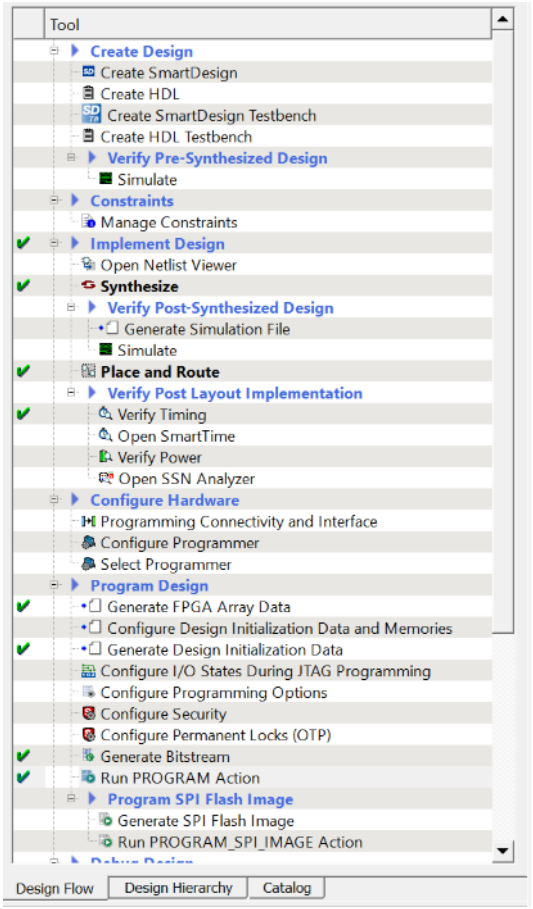
When the board is powered up, power supply LEDs DS3 to DS14 glow. For more information about LEDs on the PolarFire Evaluation Board, see *UG0747: PolarFire FPGA Evaluation Kit User Guide.*

Note: For PCB loop back demo, SMA cables are not required. User can skip Step 5.

6. Double-click **Run PROGRAM Action** from the **Libero** > **Design Flow** tab.
7. Right-click **Run Program Action** and select **View Report** to view the corresponding log file in the **Reports** tab.

When the device is successfully programmed, a green tick mark appears as shown in the following figure. See Running the Demo, page 23 to run the JESD204B standalone demo.

Figure 14 • **Programming the Device**



3.5.2 Programming the Device on Splash Kit

To program the PolarFire device on Splash kit, perform the following steps:

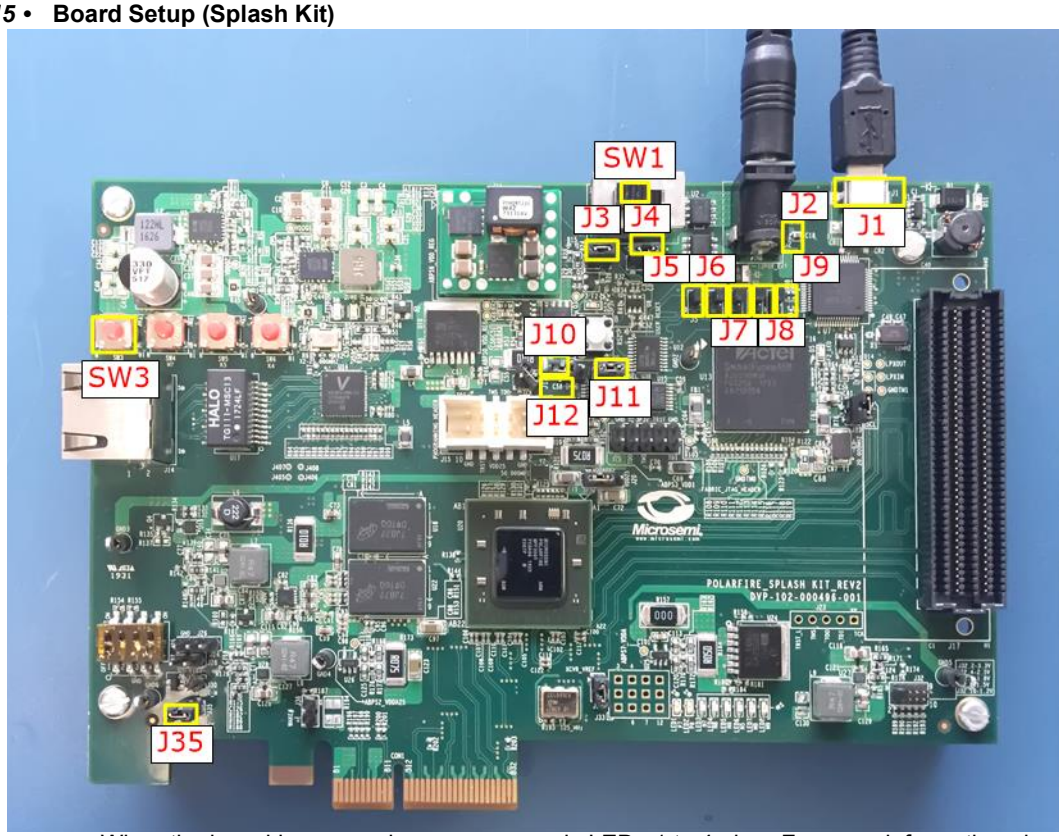
1. Ensure that the jumper settings on the board are same as listed in the following table.

Table 9 • **Jumper Settings**

Jumper	Description	Default
J11	Jumper to select either external JTAG or on-board FTDI chip for programming the device.	Closed
J3	Jumper to select the core voltage.	Open
J10	Jumper to select either FTDI chip or external SPI Flash for programming the device.	Open

2. Connect the power supply cable to the J2 connector on the board.
3. Connect the USB cable from the host PC to the J1 (FTDI port) on the board.
4. Power on the board using the SW1 slide switch.

Figure 15 • **Board Setup (Splash Kit)**



When the board is powered up, power supply LEDs 1 to 4 glow. For more information about LEDs on the PolarFire Splash Board, see *UG0786: PolarFire FPGA Splash Kit User Guide*.

5. Double-click **Run PROGRAM Action** from the **Libero** > **Design Flow** tab.
6. Right-click **Run Program Action** and select **View Report** to view the corresponding log file in the **Reports** tab.

When the device is successfully programmed, a green tick mark appears as shown in Figure .

After programming the device, see Running the Demo, page 23.

4 Running the Demo

This chapter describes how to install and use the JESD204B GUI to select the test patterns and monitor the loopback data. The GUI enables the selection of different PRBS test patterns as input, and displays the JESD204B status signals and PRBS status received from the board. The **Waveform** tab displays the output waveform samples received from the board for each waveform selected as input.

The following procedure assumes that:

- The PolarFire Evaluation or Splash board is connected.
- The PolarFire FPGA is programmed with the JESD204B design.

To run the JESD204B demo, perform the following steps:

1. Install the **JESD204B_GUI** application (setup.exe) from the following design files folder:
   `mpf_dg0755_eval_df\GUI`
   `or`
   `mpf_dg0755_spl_df\GUI`
2. Double-click the JESD204B_GUI application from the installation directory to start the GUI application.
3. Select the COM port number that is detected to configure the serial port.

Note: In **Device Manager** on the host PC, the COM port associated with the USB serial converter C. To determine the COM port, check the **Location** field in the properties of each COM port.

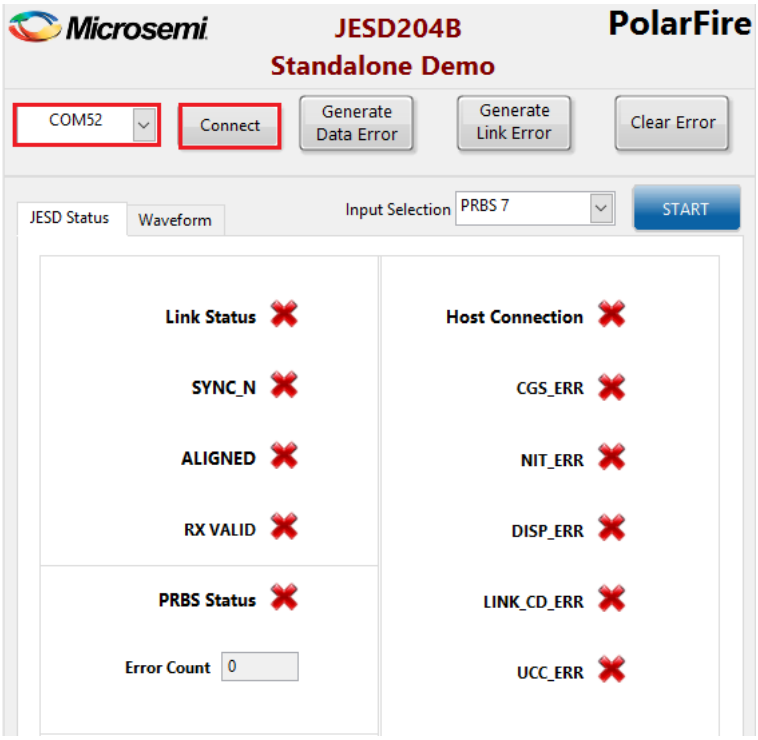
The following table lists the status signals displayed in the JESD204B GUI.

Table 10 • **Status Signals in JESD204B GUI**

Status	Description
Host Connection	Status of the UART communication
Link Status	Communication link status between TX and RX
SYNC_N	Signal which indicates the JESD link status
ALIGNED	Indicates that all transceiver lanes are aligned
RX VALID	Indicates that the Rx data is valid. In 8b10b mode, the RX VAL is qualified, comma alignment has occurred and the CDR is locked.
PRBS status	Indicates the occurrence of PRBS error. If green tick mark then no PRBS error occurred.
Error count	Number of errors that occurred during PRBS check
CGS_ERR	Indicates status of the code group synchronization error. If green tick mark then no CGS error occurred.
NIT_ERR	Indicates the “not in table” error. If green tick mark then no NIT error occurred.
DISP_ERR	Indicates the disparity error. If green tick mark then no DISP error occurred.
LINK_CD_ERR	Indicates a link configuration data mismatch error. If green tick mark then no LINK_CD error occurred.
UCC_ERR	Indicates an “unexpected control character” error. If green tick mark then no UCC error occurred.

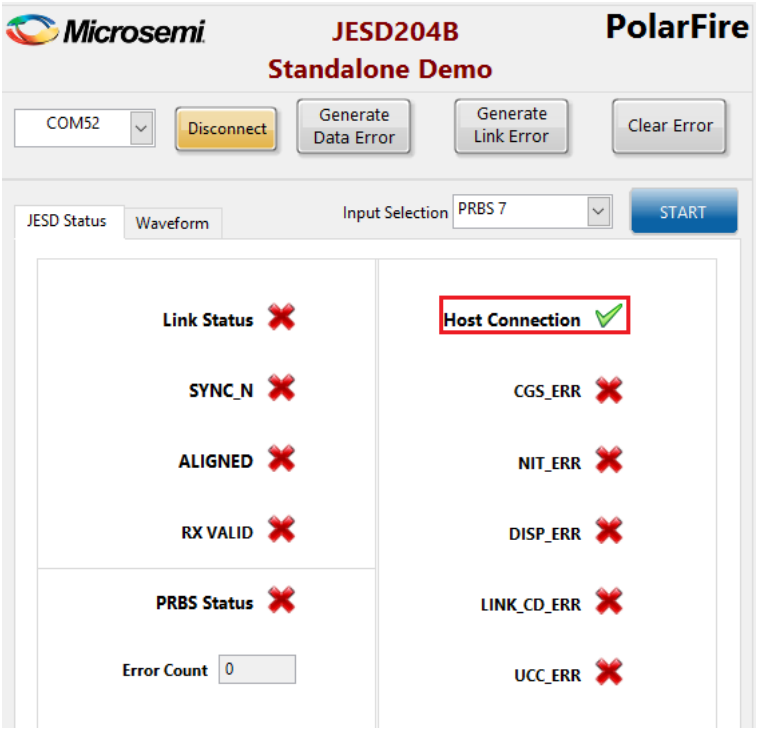
4. Click **Connect** to connect the GUI to the board through the selected port, as shown in the following figure.

Figure 16 • **Selecting COM Port and Connecting**



After successfully connecting, the **Host Connection** status changes to a green tick mark as shown in the following figure.

Figure 17 • **Host Connection Status**

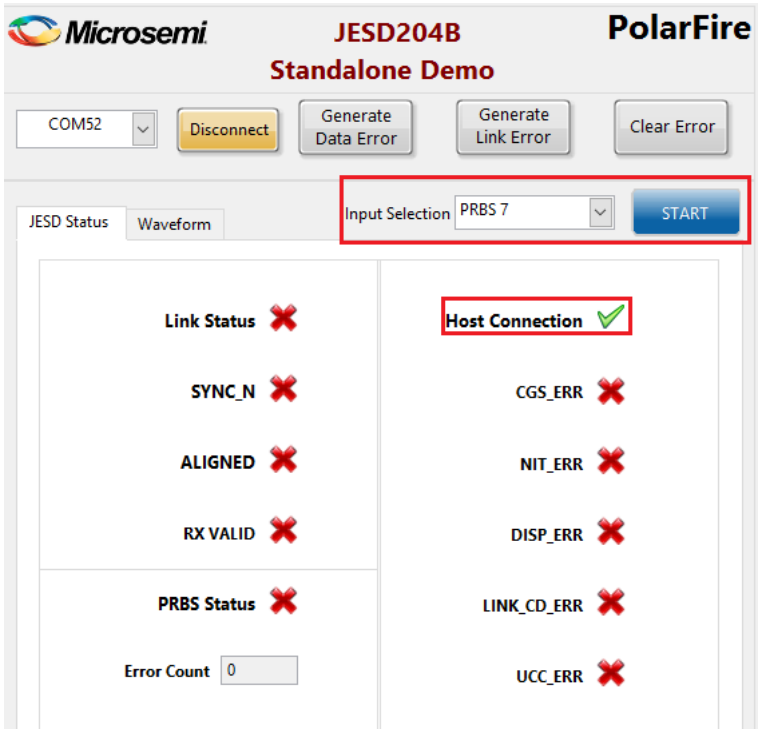


Note: Port numbers may vary. Select the correct port number from the list.

5. Reset the system using the push-button K22 (Evaluation kit) or N4 (Splash kit).

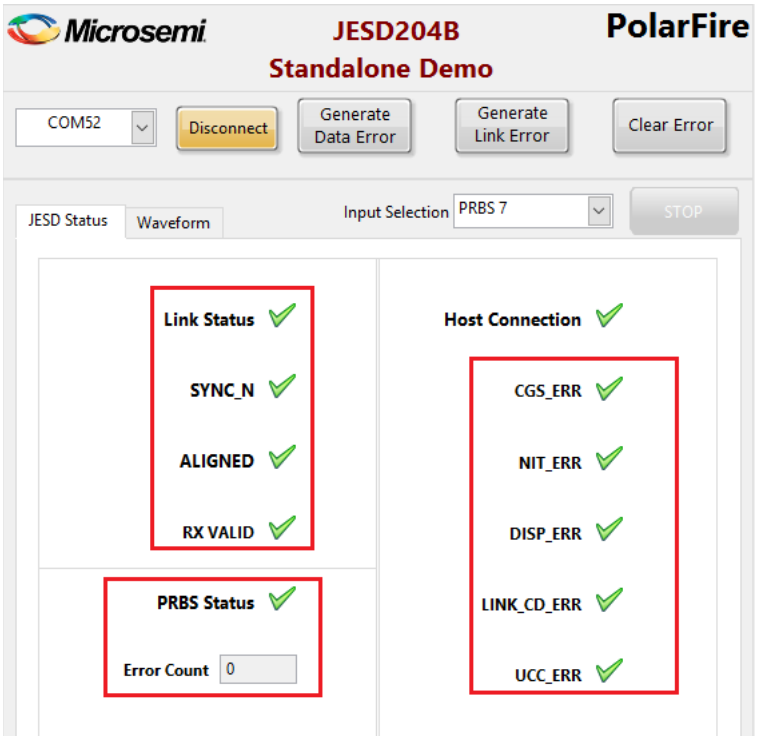
6. Select the pattern to be transmitted using the **Input selection** drop-down and click **START**. The following figure shows the PRBS7 selection.

Figure 18 • **PRBS7 Input Selection**



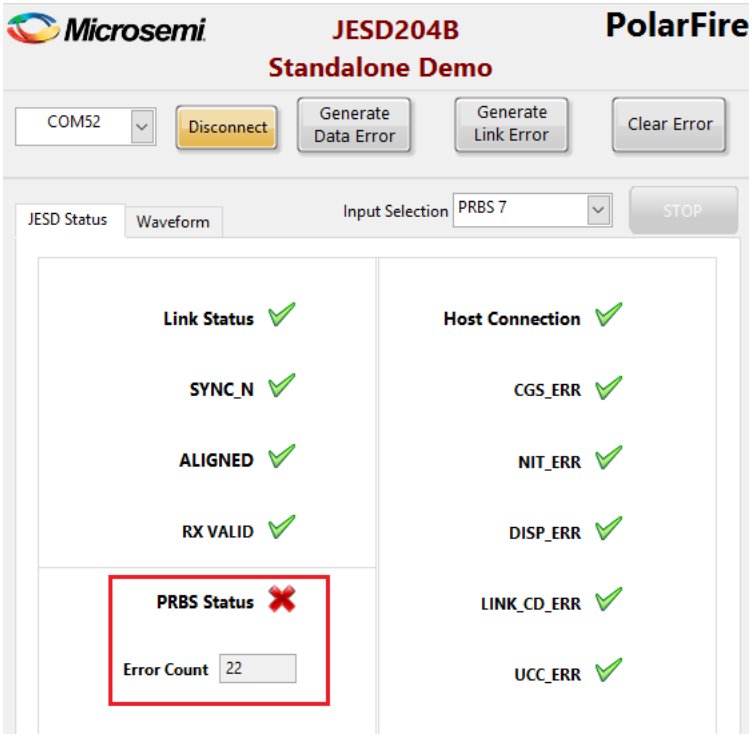
The selected pattern is sent over the serial transmit link. The looped back data is received by the receiver and checked for errors. The status can be monitored using the status signals on the GUI at any time as shown in the following figure.

Figure 19 • **Link Status and JESD204B Status**



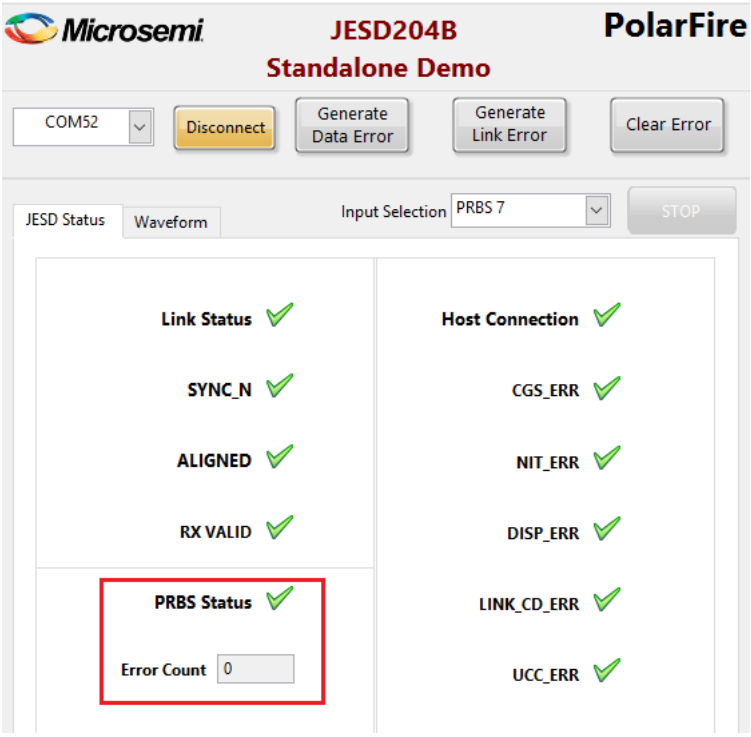
7. Click **Generate Data Error** to generate error in the PRBS data and observe the error status using **PRBS Status** and **Error Count** as shown in the following figure.

Figure 20 • **Generate Data Error**



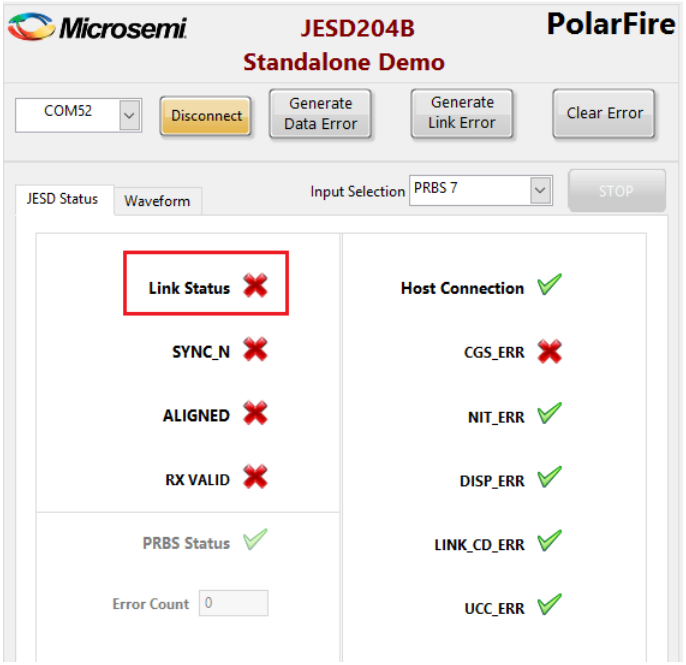
8. Click **Clear Error** to stop generate error in the PRBS data and observe that **PRBS Status** turns green, and the **Error Count** is zero as shown in the following figure.

Figure 21 • **Clear Data Error**



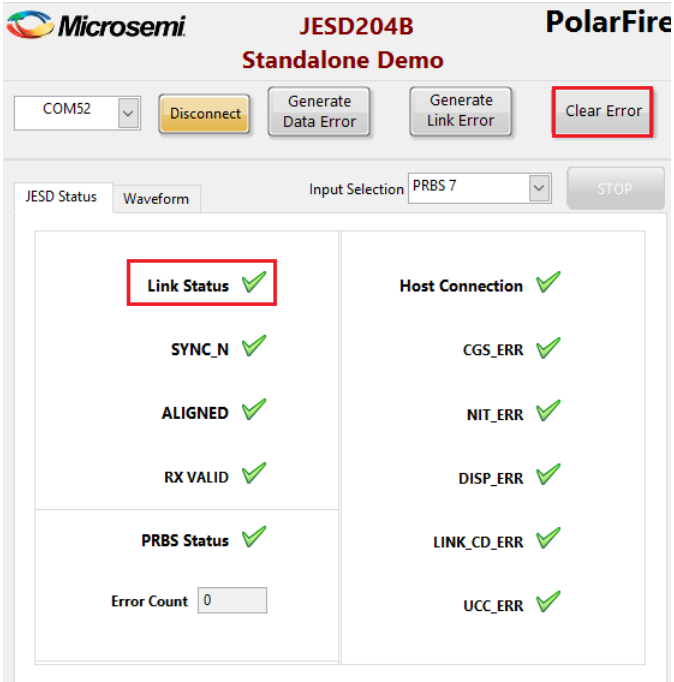
9. Click **Generate Link Error** to generate error between the CoreJESD204BTX and the transceiver lane and observe Link Status, SYNC_N, ALIGNED, RX VALID, DISP_ERR, and CGS_ERROR indicators turn red as shown in the following figure.

Figure 22 • **Generating Link Error**



10. Click **Clear Error** to stop generating the link error and observe the **Link Status** and JESD204B status signals change to green tick marks as shown in the following figure.

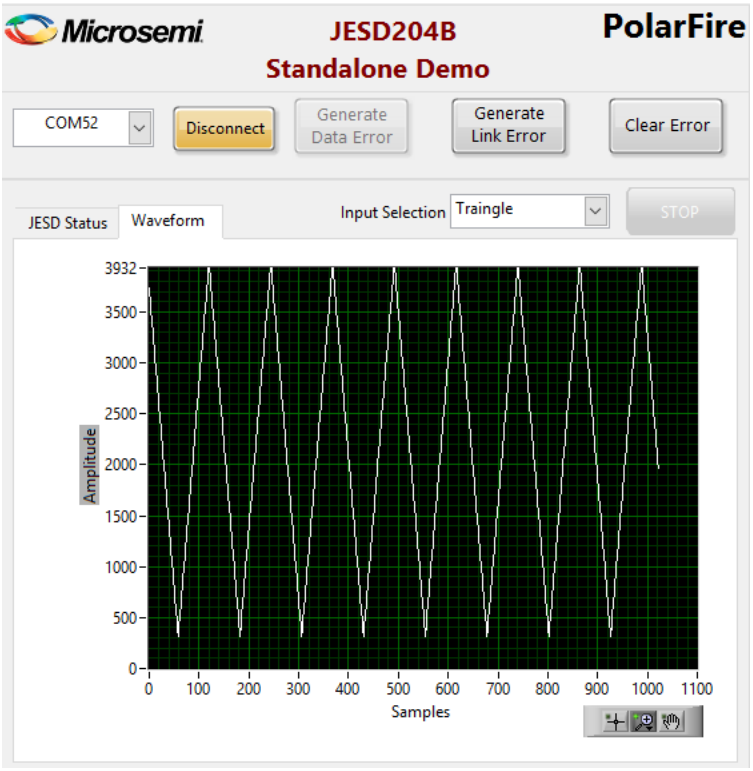
Figure 23 • **Clearing Link Error**



11. Select **Triangle** from the **Input Selection** drop-down to change the pattern. The selected pattern is sent over the serial transmit link and received by the CoreJESD204BRX. The status can be monitored using the status signals on the GUI.

12. Click **Waveform** tab to view the Triangle waveform received from CoreJESD204BRX as shown in the following figure.

Figure 24 • **Triangle Waveform**



13. Click **Stop** to end the demo and close the GUI.

This concludes the demo. The demo described the PolarFire JESD204B design and how to run the demo using the GUI.

5 Appendix 1: Programming the Device Using FlashPro Express

This chapter describes how to program the PolarFire device with the job file using Flashpro Express. The job file is available at the following design files folder location:

```
mpf_dg0755_eval_df\Programming_Job
```

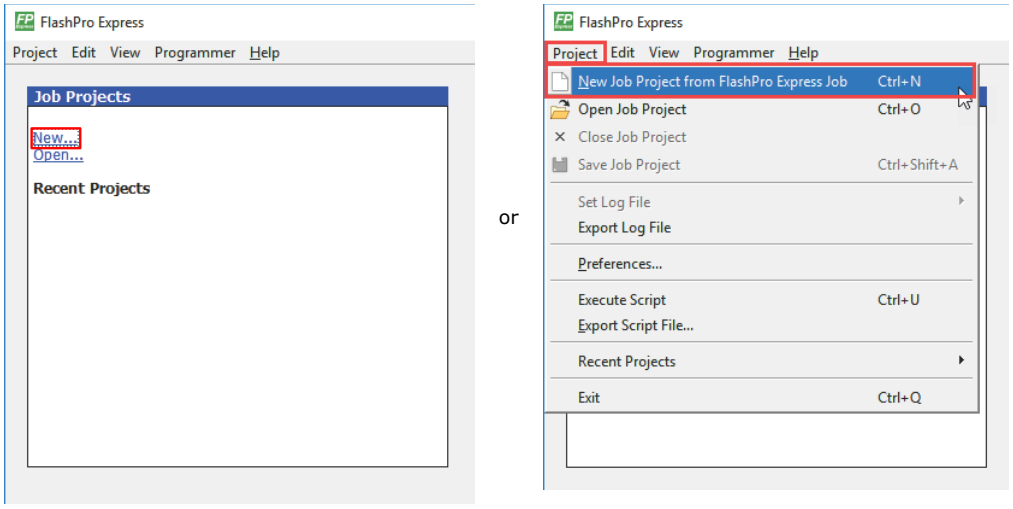
or

```
mpf_dg0755_spl_df\Programming_Job
```

To program the PolarFire device using Flashpro Express, perform the following steps:

1. Connect the jumpers and set up the PolarFire Evaluation Kit Board as described in steps 1 to 5 of Device Programming, page 19 and as shown in Figure 13.
2. Connect the jumpers and set up the PolarFire Splash Kit Board as described in steps 1 to 4 of Device Programming, page 19 and as shown in Figure 15
3. On the host PC, start FlashPro Express software.
4. Under **Project** menu, select **New** or **New Job Project from FlashPro Express Job** to create a new job project, as shown in Figure 25.

Figure 25 • **FlashPro Express Job Project**

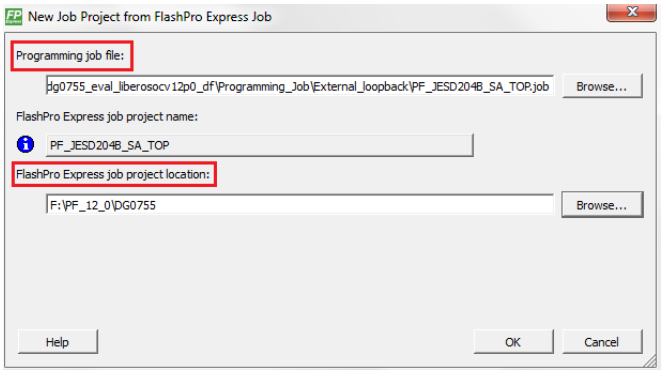


5. Enter the following details in the New Job Project from FlashPro Express Job dialog box:
   - **Programming job file**: Click **Browse**, navigate to the location where the job file is located, and select the file. The default file locations are:

     For Evaluation kit: `mpf_dg0755_eval_df\Programming_Job`

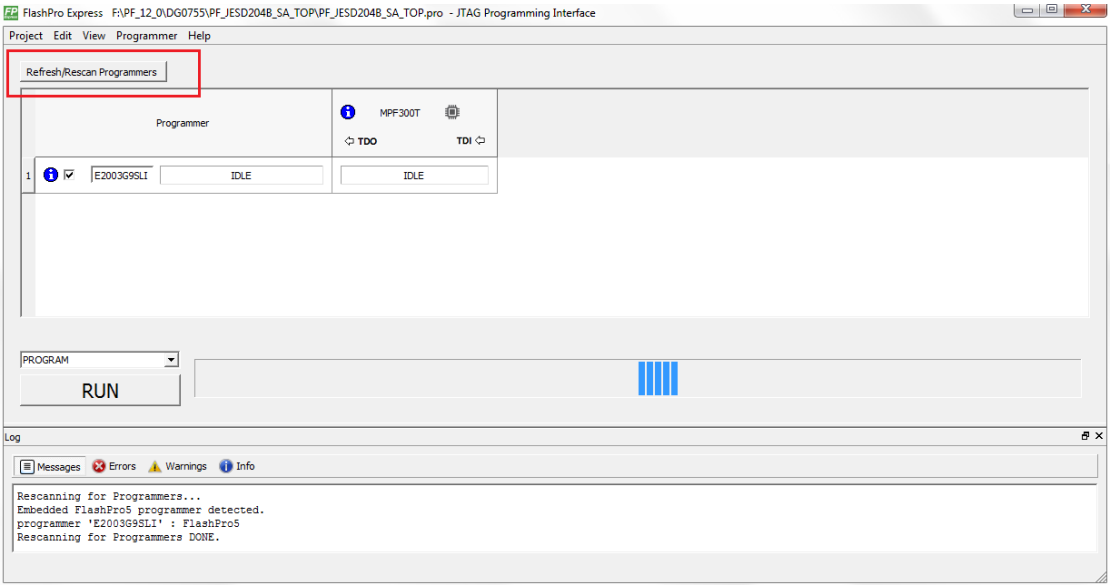
     For Splash kit: `mpf_dg0755_spl_df\Programming_Job`
   - **FlashPro Express job project location**: Select **Browse** and navigate to the location where you want to save the project.

Figure 26 • **New Job Project from FlashPro Express Job**



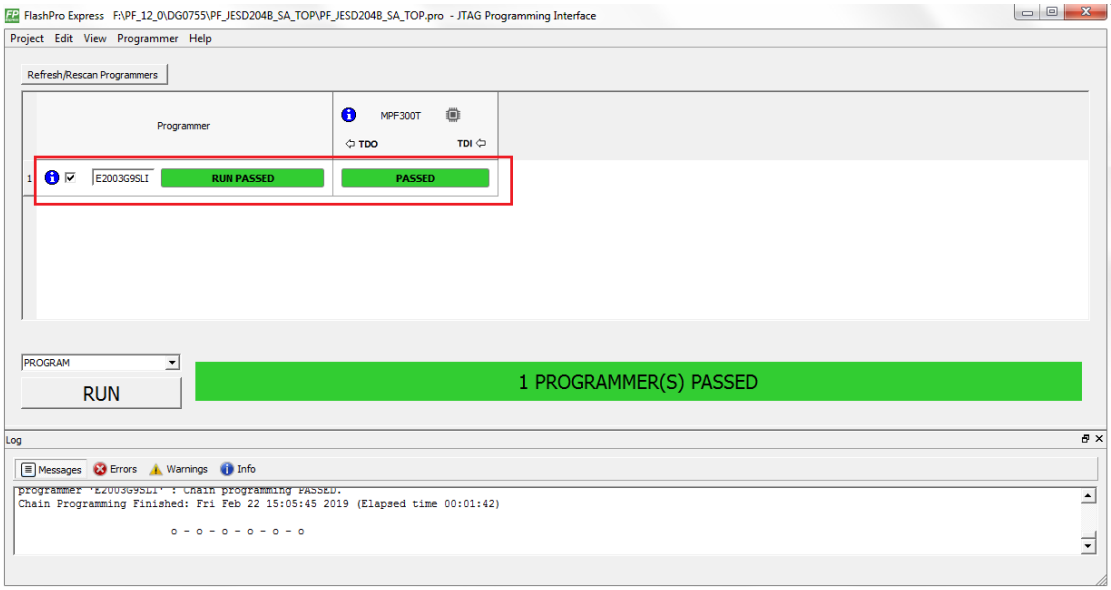
6. Click **OK**. The required programming file is selected and ready to be programmed in the device.
7. The FlashPro Express window appears as shown in Figure 27. It confirms that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan Programmers**.

Figure 27 • **Programming the Device**



8. Click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed as shown in Figure 28. For more information, see Running the Demo, page 23 to run the JESD204B demo.

Figure 28 • **FlashPro Express—RUN PASSED**



9. Close FlashPro Express or in the **Project** tab, click **Exit**.

6 Appendix 2: Running the TCL Script

TCL scripts are provided in the design files folder under directory TCL_Scripts. If required, the design flow can be reproduced from Design Implementation till generation of job file.

To run the TCL, follow the steps below:

1. Launch the Libero software
2. Select **Project > Execute Script....**
3. Click Browse and select `script.tcl` from the downloaded TCL_Scripts directory.
4. Click **Run**.

After successful execution of TCL script, Libero project is created within TCL_Scripts directory.

For more information about TCL scripts, refer to **mpf_dg0755_df/TCL_Scripts/readme.txt.**

Refer to *Libero® SoC TCL Command Reference Guide* for more details on TCL commands. Contact Technical Support for any queries encountered when running the TCL script.

7 Appendix 3: References

This section lists the documents that provide more information about the JESD204B standard and IP cores used in the demo design.

- For information about the JESD204B interface standard, see *JEDEC website*.
- For information about PolarFire transceiver blocks, PF_TX_PLL, and PF_XCVR_REF_CLK, see *UG0677: PolarFire FPGA Transceiver User Guide.*
- For more information about PF_TPSRAM (Two-Port Large SRAM), see *UG0680: PolarFire FPGA Fabric User Guide*.
- For more information about CoreJESD204BTX, see *CoreJESD204BTX Handbook*.
- For more information about CoreJESD204BRX, see *CoreJESD204BRX Handbook*.
- For more information about Libero, ModelSim, and Synplify, see Microsemi Libero SoC PolarFire web page.
- For more information about PolarFire FPGA Evaluation Kit, see *UG0747: PolarFire FPGA Evaluation Kit User Guide*.
- For more information about the Splash kit, see *UG0786: PolarFire FPGA Splash Kit User Guide*.