MAICMMC40X120

Application Note

Power Core Module Thermal Characteristics and Efficiency

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first publication of this document.

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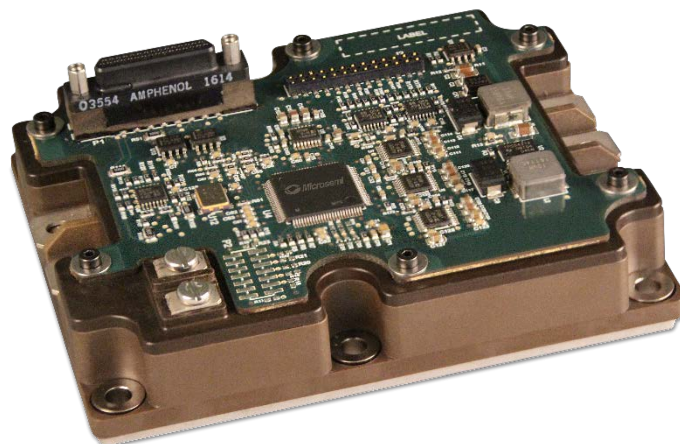
2 PCM Efficiency and Thermal Characteristics

This application note describes the thermal characteristics and efficiency of the MAICMMC40X120 [Power Core Module (PCM) with embedded MAICMMC40C120 Hybrid Power Drive (HPD) containing a SiC power bridge]. For more information, see *MAICMMC40X120 Power Core Module with SiC Power Bridge* (http://www.microsemi.com/existing-parts/parts/137208). This application note presents the power loss analysis (PLA) for the three phase bridge with SiC MOSFETs, driver printed wiring assembly (PWA), and controller PWA. Thermal performance based on power dissipation estimates is analyzed to evaluate the maximum junction temperature of the PCM PWA components and the power substrate. The following analysis is based on the requirements at 5 kVA power level for the three phase inverter with solenoid drive. The document also provides guidance based on power and thermal performance for assessing the suitability of the PCM for various power conversion applications.

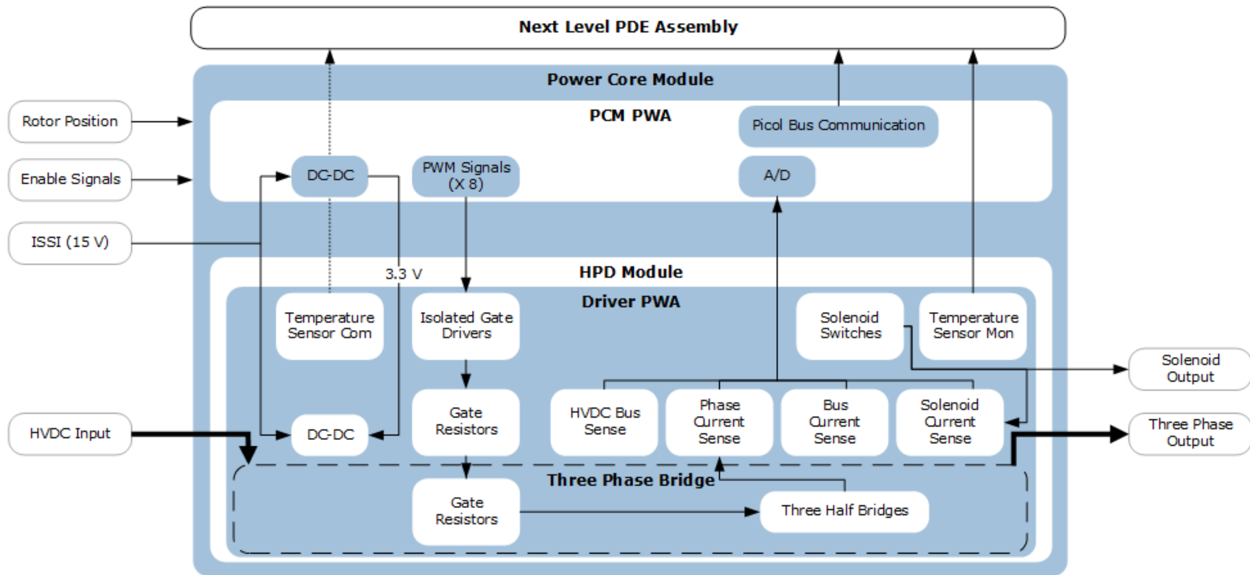
Figure 1 MAICMMC40X120 PCM



2.1 PCM Architecture

The PCM is an intelligent power solution comprising an HPD module (driver PWA and power substrate assembly with embedded SiC MOSFETs) and controller PWA. The following illustration shows the functional block diagram of the PCM.

Figure 2 PCM Block Diagram



Preliminary theoretical analysis includes PLA, stress analysis, and stability analysis of internal power supplies. These analyses are performed at each sub-assembly level (power substrate, driver PWA, and controller PWA) for different operating conditions. For PLA, efficiency is calculated based on the sum of the total power losses of the three sub-assemblies. This application note will focus on the efficiency and thermal characteristics of the PCM based on PLA.

2.2 Power Dissipation Characteristics

This section describes the power dissipation characteristics in the PCM sub-assemblies for the following operating conditions:

- Maximum peak phase current at 20 °C ambient temperature is 25 A
- Maximum peak phase current at 110 °C ambient temperature is 12.5 A

PCM characterization is also performed at –55 °C to cover the entire ambient temperature range of –55 °C to 110 °C.

2.3 Power Substrate Loss Estimation

The PLA at the substrate level comprises the conduction loss and the switching loss in the power transistors and diodes. The PLA is performed for the maximum R_{DSon} value (80 mΩ) with two free-wheeling diodes per SiC MOSFET to compute the worst case power dissipation in the PCM. SiC MOSFETs with lower R_{DSon} values and single free-wheeling diode will result in lower power dissipation. The following table shows the primary characteristics of these devices.

Table 1 Device Characteristics

Sic MOSFET	SiC Diode
Drain—Source voltage (Vdss): 1200 V	Maximum DC reverse voltage (Vr): 1200 V
Drain—Source turn on resistance (R_{DSon}): 80 mΩ at 25 °C	Diode resistance (R_D): 0.132 Ω at 25 °C

Sic MOSFET	SiC Diode
Maximum drain current (I_D): 40 A at 25 °C	Maximum forward DC current (I_F): 43 A at 25 °C

2.4 Assumptions

The following assumptions are made for the power loss calculation:

- The system delivers an output power of 5 kVA according to the peak current demand over the entire temperature range.
- The DC bus voltage is modulated to meet the 5 kVA load demand using space vector modulation (SVM) as the pulse-width modulation (PWM) technique.
- Power factor is 0.95.
- Effect of ripple current is included in the analysis.
- Switching frequency is 10 kHz.

2.5 Methodology

The total power loss per switching element is the sum of the conduction and switching losses. Equations 1 and 2 compute the conduction losses in the MOSFETs and diodes, respectively. For more information, see Infineon (2006) *MOSFET Power Losses - Calculation using datasheet parameters*.

Equation 1

$$P_MOSFET_{conduction} = R_{DSon} * I_O{}^2 * \left(\left(\frac{1}{8}\right) + \left(\frac{M_a * Cos\varphi}{3 * \pi}\right)\right)$$

Equation 2

$$P_DIODE_{conduction} = U_{D0} * I_O * \left(\left(\frac{1}{2 * \pi}\right) - \left(\frac{M_a * Cos\varphi}{8}\right)\right) + R_D * I_O{}^2 * \left(\left(\frac{1}{8}\right) - \left(\frac{M_a * Cos\varphi}{3 * \pi}\right)\right)$$

Where,

R_{DSon} = ON resistance of the MOSFET (from datasheet)

I_o = Peak output current of the inverter

M_a = Modulation index (SVPWM)

Cosϕ = Power factor

U_{D0} = Diode on-state voltage (calculated from datasheet)

R_D = On-state resistance of the diode (from datasheet)

The conduction loss at –55 °C is significantly higher than the conduction loss at 20 °C and 110 °C. The behavior of the SiC MOSFET is caused by its on-resistance variation over temperature. The on-resistance (R_{DSon}) for the SiC MOSFET and the on-state resistance (R_D) for the SiC diode are temperature dependent. For increasingly negative temperatures (below –10 °C), the on-resistance in SiC MOSFETs increases exponentially. For positive temperatures above –10 °C, the resistance increases linearly with temperature increase. After initial start-up at –55 °C, this behavior is self-correcting because the dissipation warms up the PCM until stability is reached.

For the analysis, the modulation index is calculated based on the assumption that the SVM modulation strategy is used. The following equation calculates the modulation index.

Equation 3

$$M_a = \frac{P_{out} * 2}{\sqrt{3} * V_{dc} * I_o * cos\varphi}$$

Where,

P_{out} = Output power of the converter (5 kVA)

V_{dc} = Input DC bus voltage (540 VDC)

The switching loss depends on turn-on energy, turn-off energy, and switching frequency of the inverter. The switching loss is calculated only for the SiC MOSFET. The SiC diode exhibits negligible switching loss due to very low reverse recovery losses. The turn-on and turn-off losses are averaged over the switching period. The following equation computes the switching losses. For switching losses, spice-based simulations were performed for different load cases to compute the turn-on and turn-off energies dissipated during the switching transitions.

Equation 4

$$P_{sw} = (E_{on} + E_{off}) * F_{sw}$$

Where,

E_{on} = Turn-on energy

E_{off} = Turn-off energy

F_{sw} = Switching frequency

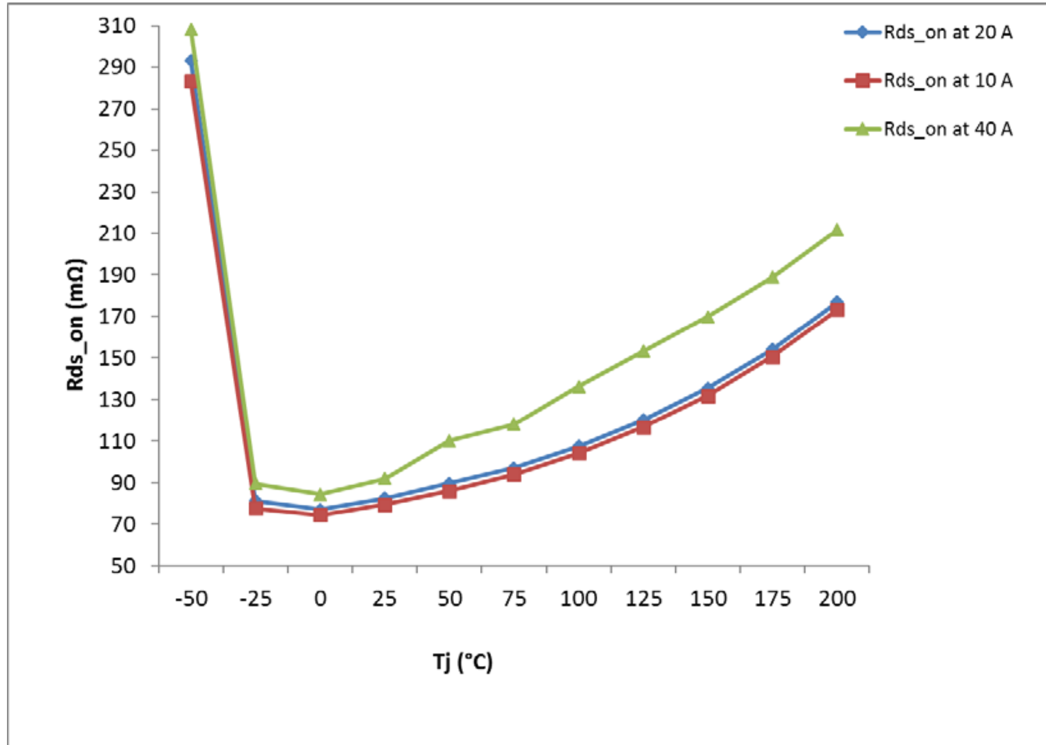
The following table represents the losses of the power substrate for the required operating conditions.

Table 2 Power Loss per Power Module at 5 kVA Load Power

Peak Current (A)	Temperature (°C)	Modulation Index	Conduction Loss (per MOSFET + diode) (W)	Switching Loss (per MOSFET)(W)	Total Loss (W)
12.5	–55	0.9	9.27	0.98	10.25
25	–55	0.45	28.18	2.26	30.44
12.5	20	0.9	1.9	0.91	2.81
25	20	0.45	7.06	2.04	9.1
12.5	110	0.9	2.6	0.93	3.53

The following illustration shows the variation of R_{DSon} with temperature.

Figure 3 Variation of R_{DSon} with Junction Temperature



Note: Various design optimizations are performed internally before finalizing the power substrate design. This includes optimizing the gate resistance to minimize the dv/dt transients while not increasing switching losses significantly, and comparing switching devices with different R_{DSon} over a range of switching frequencies and operating conditions.

2.6 Power Loss Estimation in Driver PWA

The dissipation calculation for the driver PWA is performed at –55 °C, 20 °C, and 110 °C ambient temperatures. Each component loss is assessed, which includes transistors, diodes, magnetics, passives, and ICs such as gate drivers, current sensors, and operational amplifiers. The calculations also account for losses in the high current traces through the PWA based on trace areas.

The variation in power dissipation is given in the following table.

Table 3 Driver PWA Dissipation

Peak Load Current (A)	Total Power Dissipation in Driver PWA (W)
12.5	3.57
25	4.64

Note: The variation in power dissipation estimates over the temperature range is negligible, thus the table shows the variation based on load currents only. The power loss variation is primarily seen in the current sensors and the PWA trace losses due to the change in the load current magnitude.

2.7 Power Dissipation Estimation in Controller PWA

The dissipation calculation for the controller PWA was performed at –55 °C, 20 °C, and 110 °C ambient temperatures. Each component loss is assessed, which includes passives, FPGAs, and ICs such as operational amplifiers, power converters, and analog-digital converters.

The FPGA is the main component that shows variation in power dissipation over the temperature range. The controller PWA power dissipation is independent of the load current magnitude, as it comprises low voltage circuitry only. The FPGA power loss is computed through the Smart Power Analysis tool for Microsemi FPGAs based on the utilization of resources post design optimization. For more information, see *ProASIC3 Power Calculator: SmartPower, Power Calculation Tool for FPGAs* (http://www.microsemi.com/products/fpga-soc/design-resources/power-calculator).The following table summarizes the power dissipation data in the controller PWA.

Table 4 Controller PWA Dissipation

Operating Temperature (°C)	Power Loss in FPGA (W)	Total Power Dissipation in Controller PWA (W)
–55	0.0368	0.5318
20	0.0431	0.5382
110	0.1221	0.6171

2.8 PCM Efficiency

Based on the power dissipation calculations described previously, the theoretical efficiency of the PCM is shown in the following table.

Table 5 Efficiency of SiC MOSFET Inverter

Peak Current (A)	Efficiency at –55 (°C)	Efficiency at 20 (°C)	Efficiency at 110 (°C)
12.5	98.6	99.58	99.4
25	96.24	98.8	N/A

The power dissipation calculations are inputs to the thermal model for analysis, as described in the following section.

2.9 Thermal Characteristics

Efficient thermal performance of the PCM is a critical factor in product reliability, and so thermal simulations were conducted using finite element analysis (FEA) to determine the resulting temperatures based on worst-case operating conditions (that is, an ambient temperature of 110 °C and a convection coefficient of 2 W/m^2K). The component power dissipation estimations from the PLA discussed in the previous section were used in the thermal model to generate the surface temperature profiles. The thermal model that generated the component temperatures is based on the following assumptions:

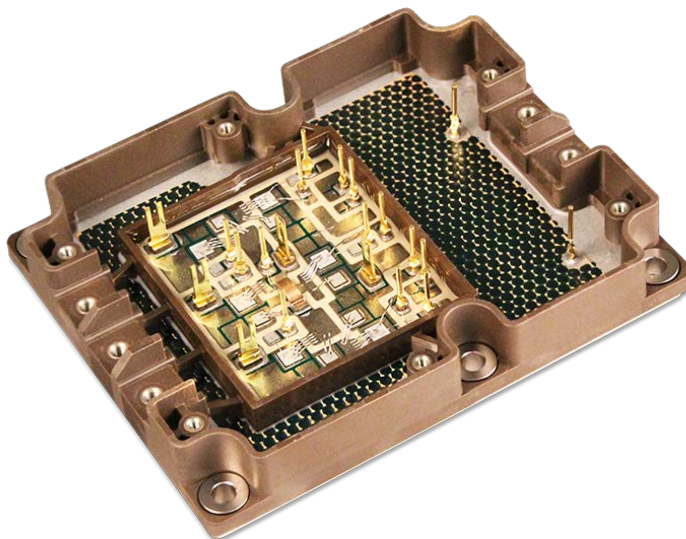
- The material that forms the PCM housing and cover has poor thermal conductivity, and so it does not have a significant impact on component junction temperatures. As a result, the housing and the cover were not included in the model.
- The ambient temperature is at 110 °C, and is applied as an infinite capacity 110 °C boundary condition at each interface location. This means that the model does not consider secondary thermal paths between the PCM and the ambient environment.

- There is full thermal contact between the PCM and the cold source without air gaps. The model incorporates a thermal resistance (1.13 °C cm^2/W) at the baseplate to simulate the presence of the thermal interface material between the baseplate and the cold source. For more information, see *MAICMMC40X120 Application Note: Power Core Module Mounting and Thermal Interface.* As the PCM ages, this thermal interface can deteriorate and result in higher thermal contact resistances. The degradation in the thermal performance of the thermal interface material depends on its operation temperature, expected lifespan, and material properties. Therefore, the selection and maintenance of the thermal interface material should take into account the thermal performance stability of the candidate thermal interface material.
- The analysis represents a continuous power situation with steady-state heat transfer.
- All internal heat transfer is by conduction only.
- For the controller PWA, heat transfer was assumed to occur by conduction and convection in free air.

The surface temperature profiles for each constituent part of the PCM for a 110 °C ambient and 12.5 A current are presented herein. The highest component junction temperatures for each constituent part of the PCM, based on ambient temperatures of –55 °C, –40 °C, 20 °C, and 110 °C, and currents of 12.5 A and 25 A are presented in Table 6.

Power dissipation occurs from the power substrate and the driver PWA in the HPD, and from the controller PWA in the PCM. In the HPD, cooling is carried out by means of conductive heat transfer from the substrate to the baseplate, and from the driver PWA to the baseplate through a network of vertical copper pins, as shown in the following illustration. Heat generated by the components is then transferred from the baseplate to a cold-source through a thermal grease interface. For more information on the steps for correct application of the thermal interface and mounting of the PCM to ensure effective heat transfer, see *MAICMMC40X120 Application Note: Power Core Module Mounting and Thermal Interface.*

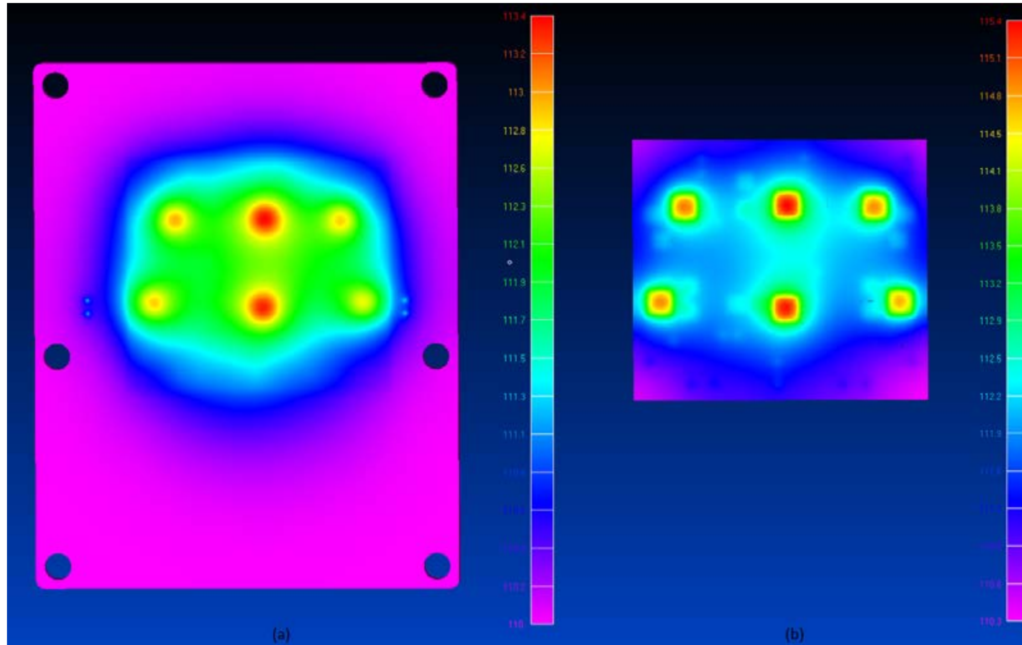
Figure 4 HPD Housing



As the highest power components are located on the substrate, it is therefore the source of the largest portion of the overall power dissipation. The temperature contour of the baseplate, as shown in the following illustration, shows that while most of the baseplate stays close to ambient

temperature, the region directly beneath the substrate is the only area involved in heat transfer to the cold source. This results in a temperature gradient across the baseplate of approximately 3 °C. The components with the highest power dissipations and the hottest components on the substrate are the six SiC MOSFETs (Ref Q1-6).

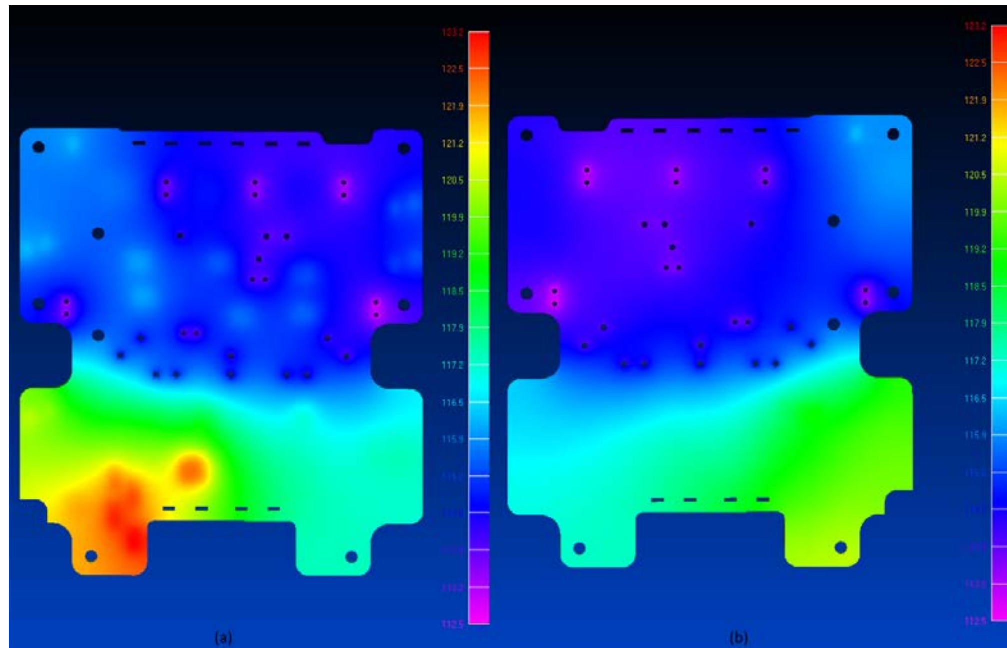
Figure 5 Temperature Contour Plots of the Baseplate and Substrate Surfaces



Note: Figure 5a demonstrates the temperature contour plot of the baseplate while Figure 5b demonstrates the temperature contour plot of the substrate.

As previously mentioned, heat transfer from the driver PWA to the baseplate occurs through the copper pins; this can be seen in the following illustration, which shows the temperature contours of the upper and lower surfaces of the driver PWA. For the worst-case power dissipation analysis, the component junction temperatures stay below manufacturer-specified temperatures. The components with the highest power dissipation are the single channel IGBT gate drivers (component references: U52, U53, U101, U102, U151, U152, U201, and U202). Two of the IGBT gate drivers (U201 and U202) have the highest junction temperatures on the driver board due to the physical location on the PWB mounted farthest from the thermal cooling path.

Figure 6 Temperature Contour Plots of Driver PWA



Note: Figure 6a demonstrates the temperature contour plot of the top surface, while Figure 6b demonstrates the temperature contour plot of the bottom surface of the driver PWA.

2.10 PWA Thermal Characteristics

The following discussion applies to the controller PWA only. A secondary conductive path from the controller PWA directly to the cold source may provide additional cooling. For more information on Microsemi's recommendations for controller PWA thermal management, see *MAICMMC40X120 Application Note: PCM Mounting and Thermal Interface*. Unlike the driver board and the substrate (when heat transfer occurs only due to conduction), heat transfer from the controller PWA occurs due to conduction and convection as it is mounted on the exterior of the module.

Figure 7 Temperature Contour Plots of Controller PWA for Convective and Conductive Cooling

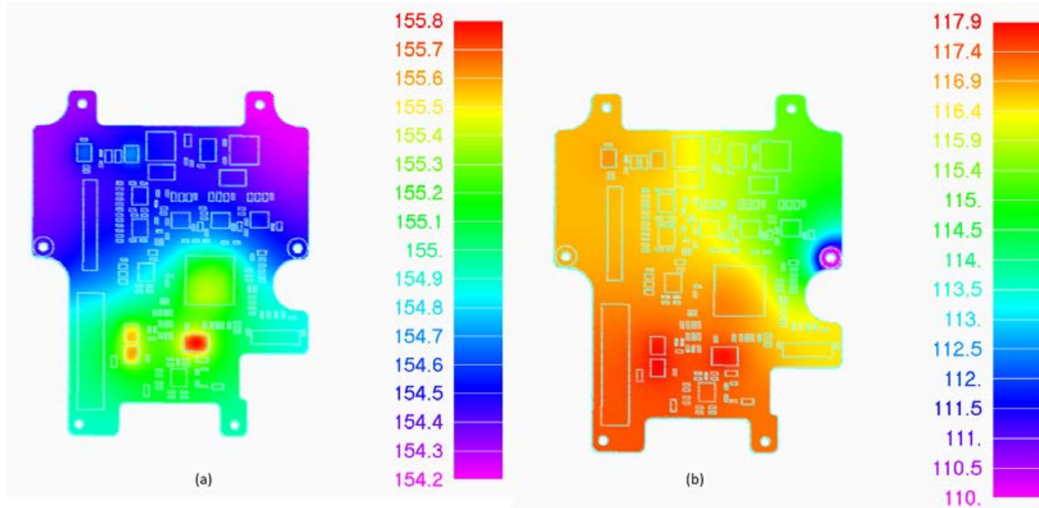


Figure 7a shows the temperature plot of the controller PWA surface with cooling by means of convection in free air only. Figure 7b shows the temperature plot when heat transfer occurs due to both convection in free air and through the additional conductive path (such as a thermal strap) to the cold source. For the worst-case power dissipation analysis, the component junction temperatures stay below manufacturer-specified temperatures only when the additional conduction path is used (up to a maximum ambient temperature of 110 °C). This additional conductive path must be used in applications where the ambient temperature exceeds 70 °C to maintain junction temperatures below their specified temperature limits. The components with the highest power dissipation on the controller PWA are the FPGA (U4) and the LVDS drivers (U3 and U13). The hottest components on the controller PWA are the 40 MHz oscillator (U12) and the LVDS drivers (U3 and U13).

Based on the surface temperatures generated by the thermal model shown in the previous three temperature contour plots, the temperatures in each component are calculated using the PWA-to-case and case-to-junction thermal resistances. The following table shows the highest resulting junction temperatures for each constituent of the PCM for different ambient temperatures and operating currents.

The following table of the highest resulting junction temperature based on the thermal model PWA surface temperatures shows that the additional conductive path is required above 70 °C, and that, at an ambient temperature of 110 °C, the components will exceed the manufacturer limit of 125 °C. Provided this additional conductive path is used above ambient temperatures of 70 °C, then none of the components in the PCM will significantly exceed the maximum operating temperature specified by the manufacturer (up to an ambient temperature of 110 °C).

Table 6 Highest Resulting Junction Temperature

Operating Conditions		Highest Resulting Junction Temperature (°C)				
Ambient Temperature (°C)	Operating Current (A)	Baseplate	Substrate	Driver PWA	Controller PWA	Controller PWA with Strap
–55	12.5	–47.29	–33.41	–24.74	–10.59	–40.26
	25	–36.79	–4.70	–19.99		

Operating Conditions		Highest Resulting Junction Temperature (°C)				
Ambient Temperature (°C)	**Operating Current (A)**	**Baseplate**	**Substrate**	**Driver PWA**	**Controller PWA**	**Controller PWA with Strap**
–40	12.5	–35.84	–28.59	–11.48	0.12	–25.26
	25	–32.01	–19.05	–8.18		
20	12.5	23.01	28.08	48.79	65.12	38.84
	25	24.89	31.80	51.88		
110	12.5	113.4	119.17	139.70	164.05	123.92

2.11 Summary

This document describes the performance evaluation of PCM based on the power dissipation and thermal characteristics for 5 kVA three phase inverter applications. The characterization of the module and its sub-assemblies are performed based on internal requirements.

The PLA is performed at 5 kVA output power for the entire temperature range of –55°C to 110 °C ambient temperature for 12.5 A and 25 A load currents. The thermal analysis is performed for the 12.5 A peak output current at 110 °C ambient temperature to demonstrate the thermal performance of the PCM under worst-case conditions. The resultant component junction temperatures all remain below 125 °C. The highest temperature components on the controller PWA are the 40 MHz oscillator (U12) and the LVDS drivers (U3 and U13). The highest temperature components on the substrate are the SiC MOSFETs (Q1-6). Two of the single channel IGBT gate drivers (U201 and U202) have the highest junction temperature on the driver PWA. If an additional conductive path from the controller PWA to the cold source is used above ambient temperatures of 70 °C none of the PCM components will exceed their maximum rated temperatures up to a maximum ambient temperature of 110°C.