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Synplify Pro® for Microsemi Edition Release Notes

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Publication Version 01

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About the Release

This J-2015.03M-SP1-1 release includes software features and enhancements for the Synplify Pro® Microsemi Edition product. For the complete summary of features and enhancements contained in the base release, see Feature and Enhancement Summary below.

Feature and Enhancement Summary

The following table highlights the J-2015.03M-SP1-1 features:

Feature	Description
Support for URAM inference for sequential shift registers	Synplify Pro is enhanced to support URAM inference for sequential shift registers. By default, seqshift is implemented using registers.The syn_srlstyle attribute is used to override the default behavior of seqshift implementation using URAM. This support is available for SmartFusion2, IGLOO2, and RTG4 technologies. *Reference Manual->Designing with Microsemi->Microsemi Components->Microsemi RAM Implementations* *Attribute Reference->Attributes and Directives*

The following table highlights the J-2015.03M-SP1 features:

Feature	Description
Support for Error Correction Codes (ECC) and Single Event Transient (SET) features for RTG4 RAMs	RAM inference is enhanced for RTG4, both RAM1K18_RT and RAM64x18_RT, using ECC pin and SET pin with error monitoring. Both features are enabled using the syn_ramstyle attribute. *Reference Manual->Designing with Microsemi->Microsemi Components->Microsemi RAM Implementations* *Attribute Reference->Attributes and Directives*
New operating conditions support for SmartFusion2, IGLOO2 and RTG4.	The tool is enhanced to support new operating conditions: • COMTC • COM1p0TC

The following table highlights the J-2015.03M features:

Feature	Description
Cross-Module Referencing for RAM Initialization	RAM can be accessed hierarchically and initialized with the $readmemb/$readmemh statement from the top-level design. *Reference Manual->RAM and ROM Inference->Initial Values for RAMs*
Compiler Enhancements (Verilog/SystemVerilog)	Compiler support includes the following: • Multiple configuration blocks • Configurations with generate statements • The $typeof operator • Enumerated type methods • Aggregate assignments on ports • Structure assignment patterns using member names *Reference Manual->Verilog Language Support* and *SystemVerilog Language Support*

Platforms

This section includes platform support for the Synopsys FPGA synthesis products. The software is supported on the platforms and operating systems listed below:

Windows	• Windows 8.1 Professional or Enterprise (64-bit) • Windows 7 Professional or Enterprise (32/64-bit) • Windows Server 2008 R2 (64-bit) • Windows Server 2012 R2 (64-bit)
Linux	All Linux platforms require 32-bit compatible libraries. • Red Hat Enterprise Linux 5 (32/64-bit)/6 (64-bit) • SUSE Linux Enterprise 10/11 (32/64-bit)

Documentation

The following documents are included with the Synopsys FPGA synthesis products. All documents can be accessed through the online help (HTML), and as PDF documents. See *Accessing Online Help* on page 4, and *Accessing PDF Documents* on page 4 for information on how to access the documents.

Document	Access
User Guide	Online help, context-sensitive help, PDF
Reference Manual	Online help, context-sensitive help, PDF

Document	Access
Attribute Reference Manual	Online help, context-sensitive help, PDF
Command Reference Manual	Online help, context-sensitive help, PDF

Accessing PDF Documents

PDF documents display in Adobe Acrobat Reader. You can download the latest Acrobat Reader at no cost from Adobe's website (www.adobe.com). The PDF files provided are optimized for output to a laser printer, not for viewing online.

You can access the PDF documents in multiple ways, while running the tool or separately:

- From within the tool, with the Help-Online Documents command.
- From outside the tool, as described below:

Linux	From outside the software, select Open Acrobat Reader: `acroread` Open *installDirectory*`/documents/`*`docFile`*
Windows	Start->Programs->Synopsys->FPGA Synthesis J-2015.03M-SP1-1->Documents Then, select the desired document.

If the PDF for the online documentation does not open in the synthesis tool, make sure you are using a recent version of the Acrobat Reader that can be downloaded from Adobe's website. Do not use the View->Full Screen option when viewing documents in Acrobat Reader unless you are sure you want this full magnification. On some applications, this selection takes over the monitor and there is no apparent way to access other running tasks or windows. If you do happen to use the Full Screen option, you can use Ctrl-l to undo it.

Accessing Online Help

This section describes how to access online help and context-sensitive help in the Synplify Pro tool. If your online help graphics do not display correctly, this is usually because your Display setting is 256-Color. Reset it to 16-bit Color, then reopen the online help.

Accessing Help from inside the tool	
All platforms	Select Help->Help for the online help system. For context-sensitive help, click F1 in a dialog box or window. For context-sensitive help for an error message, click the link in the log file or the Message viewer.
Accessing Help from outside the tool	
Windows	Select Start->Programs->Synopsys->FPGA Synthesis J-2015.03M-SP1-1 ->Help
Linux	Run fpga_help.

Known Problems and Solutions

The following problems apply to supported features in the Synplify Pro tool.

GUI Processing can Fail on Windows 7 for the Synthesis Tool

The synthesis tool GUI might intermittently stop responding on Windows 7.

Solution: To resolve this issue, apply the hotfix from Microsoft by going to http://suppport.microsoft.com/kb/2718841/.

EncryptP1735 Script Sensitivity

The encryptP1735.pl script does not run correctly when used with the default Windows command shell due to the shell's limited Perl support (the script works correctly on a Linux 64-bit platform).

Solution: To run the script from a Windows platform, use a freeware windows shell such as Cygwin 32-bit version 2011 or later with OpenSSL and Perl

Crossprobing Source Code Files Created with Third-Party Editors

When using source code files created with third-party editors, you sometimes cannot crossprobe to the correct line number in the source file.

Solution: Open the file in the FPGA synthesis tool text editor.

Editing Externally Created Project (prj) Files

If Tcl commands or script files were used to build your project, you might not be able to save this Project file from the synthesis UI in downstream tools, because they contain hard-coded file paths.

Solution: Generally, use the same method to save a project as you did to create the project. In this case, save the project file to an external text editor and not in the project UI.

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