# IGLOO2 FPGA Adaptive FIR Filter - Libero SoC v11.6

## DG0514 Demo Guide



October 2015

Microsemi

# Revision History

| Date | Revision | Change |
|---|---|---|
| 16 October 2015 | 5 | Fifth release |
| 23 January 2015 | 4 | Fourth release |
| 11 August 2014 | 3 | Third release |
| 11 June 2014 | 2 | Second release |
| 7 January 2014 | 1 | First release |

## Confidentiality Status

This is a non-confidential document.

# Table of Contents

# Preface

## About this document

This demo is for IGLOO®2 field programmable gate array (FPGA) devices. It provides instructions on how to use the corresponding reference design.

## Intended Audience

IGLOO2 devices are used by:

- FPGA designers
- System-level designers

## References

### Microsemi Publications

- *UG0451: IGLOO2 FPGA and SmartFusion2 SoC FPGA Programming User Guide*
- *UG0450: SmartFusion2 SoC FPGA and IGLOO2 FPGA System Controller User Guide*
- *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide*
- *Configuring Serial Terminal Emulation Programs Tutorial*

See the following web page for a complete and up-to-date listing of IGLOO2 device documentation: *http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga*

# IGLOO2 FPGA Adaptive FIR Filter Demo

## Introduction

The IGLOO2 FPGA devices integrate a fourth generation flash-based FPGA fabric architecture, which includes embedded mathblocks optimized specifically for digital signal processing (DSP) applications such as, finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast Fourier transform (FFT) functions.

An adaptive filter is a filter that automatically adjusts the filter coefficients according to the underlying adaptive algorithm and the input signal characteristics. Due to its self adjustment of transfer function of an unknown system and computational requirements, adaptive filters are widely used in different areas of DSP application such as communication, biomedical instrumentation, audio processing, and video processing.

The least mean square (LMS) is the basic adaptive algorithm used in adaptive filters to update the filter coefficients. The LMS algorithm has advantages over other algorithms because of its simplicity, less computations and best performance in terms of the number of iterations required for convergence.

In this demo, the suppression of a narrow band signal interference on a wide band signal is implemented using an IGLOO2 device. Refer to Figure 1.

The LMS algorithm is implemented in the FPGA fabric to adjust the filter coefficients based on the mean square error (MSE) approach. CoreFIR IP is used to perform the filtering operation and CoreFFT IP is used to generate the output spectrum to observe that the narrow band interfering signal component is suppressed. The host interface is implemented in FPGA fabric using CoreUART IP to communicate with the host PC. A user friendly `IGL2_Adaptive_FIR_Filter.exe` generates input signals (narrow band signal and wide band signal), and also plots the input or output waveforms and the required spectrum.


***Figure 1 •*** **Narrowband Interference Cancellation**

## Theory of Operation

Adaptive filters are mainly categorized into four basic architectures:

- System identification
- Noise cancellation
- Linear prediction
- Inverse modeling

In this demo, linear prediction architecture is used to implement adaptive filter. The LMS algorithm uses a gradient search technique to determine the filter coefficients that minimize the mean square prediction error. The estimate of the gradient is based on the sample values of the tap-input vector and the error signal. The algorithm iterates over each coefficient in the filter, moving it in the direction of the approximated gradient. After reaching the optimal filter coefficients, the error signal e(n) consists of the Wideband signal. Figure 2 shows the linear prediction based adaptive filter architecture.

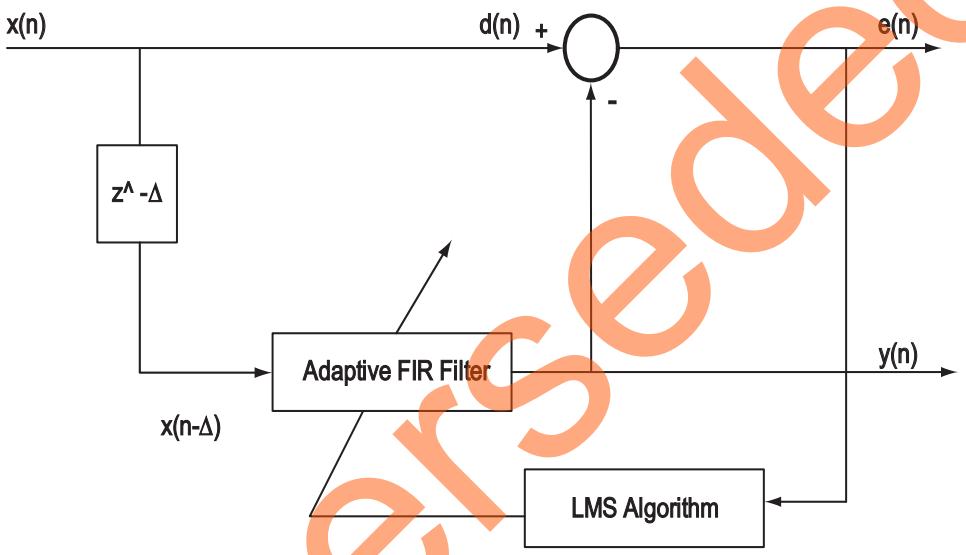


***Figure 2 •*** **Linear Prediction Adaptive Filter Architecture**

The input signal x(n) consists of wideband signals along with the narrow band signals that are not required, refer to Figure 3 on page 8. In a linear prediction architecture, the desired signal d(n) is same as the input signal x(n) and a delayed input x(n-Δ) is fed to the adaptive filter as shown in Figure 2. The delay factor Δ (delta) de-correlates the wide band component and correlates the narrow band component of the desired signal d(n) with the delayed input signal x(n-Δ).

The adaptive filter tries to estimate the narrow band component y(n), and forms an equivalent transfer function, which is similar to that of narrow band filters centered at the frequencies of the narrow band components of the input signal. At the summing junction, the filtered input signal subtracting with delayed input signal produces an error signal. The error signal is used by the LMS algorithm to adjust the filter coefficients. After some iterations, the Error signal converges to a wide band component.

The following equations describe computing the coefficients using the LMS algorithm.

$$y(n) = \sum_{k=0}^{k=l-1} h(n) \times x(n - \Delta - k)$$

EQ 1

where,
According to EQ 1, narrow band component y(n), is the adaptive filter output
h(n) is the filter coefficients
x(n-Δ) is the input signal to the adaptive filter
l is the length of the filter (number of taps)
k is the index variable
The error is computed using the following equation:

e(n)= d(n)- y(n)

EQ 2

where,
e(n) is the error signal
d(n) is desired signal

The filter coefficients are updated using the following equation:

h(n+1)=h(n)+μ*e(n)*x(n-Δ)

EQ 3

where,
h(n+1) is the estimated filter coefficients
h(n) is present filter coefficients
μ is the step size factor

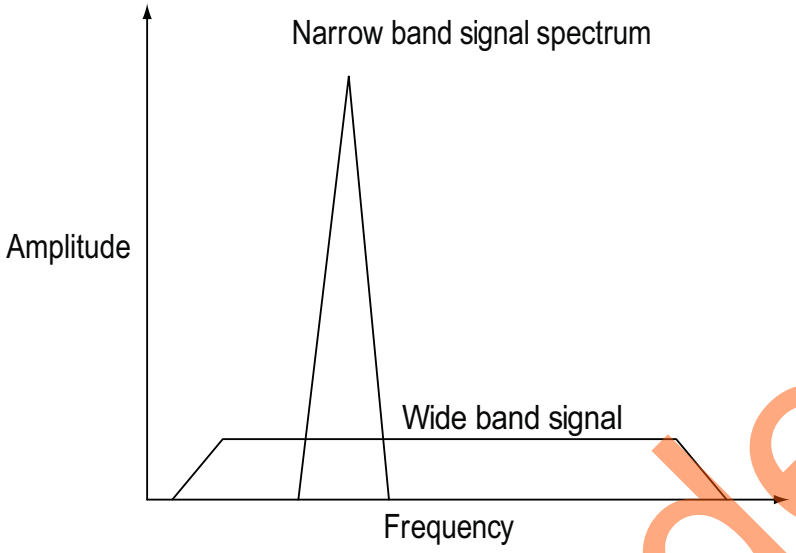


***Figure 3 •*** **Input Spectrum of Narrow Band Signal + Wide Band Signal**

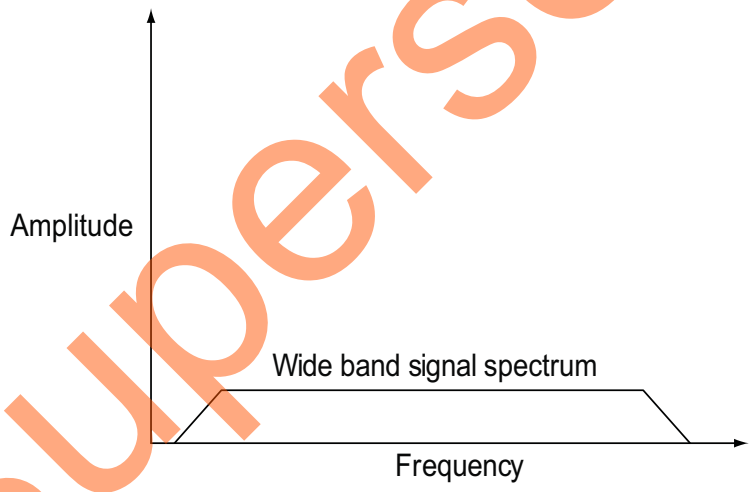


***Figure 4 •*** **Output Spectrum of Wide Band Signal**

# Design Requirements

***Table 1 •*** **Design Requirements**

| Design Requirements | Description |
|---|---|
| **Hardware Requirements** | |
| IGLOO2 Evaluation Kit:<br>• FlashPro4 programmer<br>• USB A to Mini-B cable | Rev C or later |
| Host PC or Laptop | Windows 7 64-bit Operating System |
| **Software Requirements** | |
| Libero® System-on-Chip (SoC) | v11.6 |
| FlashPro Programming Software | v11.6 |
| Host PC Drivers | USB to UART drivers |
| Framework | Microsoft .NET Framework 4 Client for launching demo GUI |

# Demo Design

## Introduction

The design files for this demo can be downloaded from the Microsemi® website:
*http://soc.microsemi.com/download/rsc/?f=m2gl_dg0514_adaptive_fir_filter_liberov11p6_df*

Design files include:

- Design files
- GUI
- Programming files
- Readme file

Figure 5 shows the top-level structure of the design files. For further details, refer to the `Readme.txt` file.

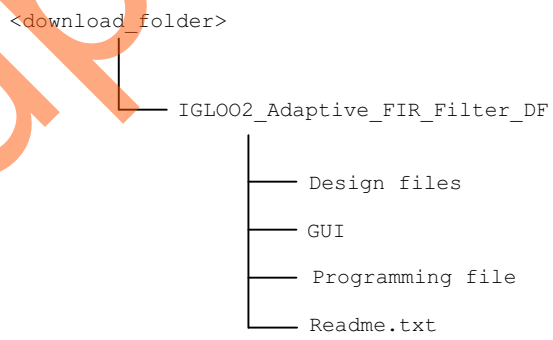


***Figure 5 •*** **Demo Design Files Top-Level Structure**

## Demo Design Description

This demo design uses the following blocks:

- Data Handle Block (SmartDesign)
- Filter Control (user RTL)
- LMS_FIR_TOP (Smart Design)
- TPSRAM IP (IPcore)
- CoreFFT (IPcore)
- SYSRESET(IPcore)
- OSC (IPcore)
- CCC (IPcore)
- CoreUART (IP Core)

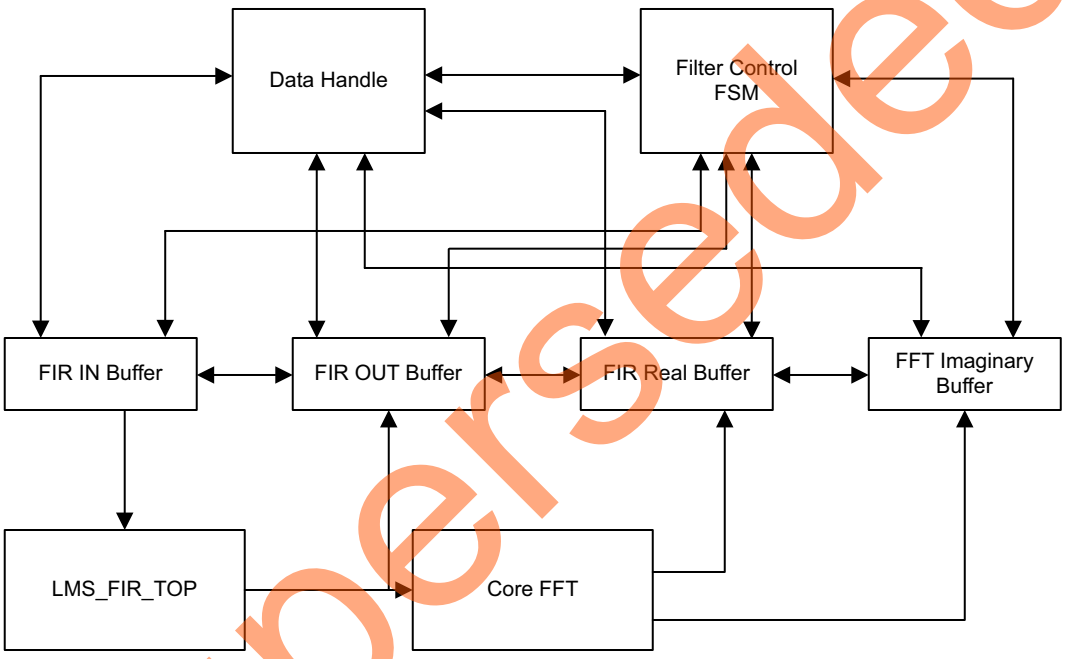


***Figure 6 •*** **Adaptive FIR Filter Demo Design Block Diagram**

### *Data Handle Block*

The Data handle block consists of a CoreUART IP and UART interface finite state machine to handle the controls and operations between the host PC (GUI interface) and fabric logic. It controls loading filter input data to the corresponding input data buffer and then send and receive data from the host PC.

### *Filter Control*

Controls the FIR filter and FFT operations. It loads the filtered data to the corresponding output buffer and moves the FFT output data to the corresponding output data buffer.

### *LMS_FIR_TOP*

This is a SmartDesign block implemented in the fabric. It consists of the following blocks:

- **LMS_CONTROL_FSM**: This finite-state machine (FSM) is implemented in the RTL to provide the control signals to the LMS_ALGO block.
- **LMS_ALGO**: This LMS algorithm is implemented in RTL to compute the error signal, correction factor, filter coefficients, and to send the filter coefficients to the Core FIR filter.

- **CoreFIR**: CoreFIR IP is used in the Reloadable Coefficient mode to configure its coefficients on the fly. CoreFIR IP configuration is as follows:
  - Version: 8.6.101
  - Filter Type: Single rate fully enumerated
  - No of taps: 8
  - Coefficients type: Reloadable
  - Coefficients bit width: 16 (signed)
  - Data bit width: 16 (signed)
  - Filter structure: Transposed with no symmetry

### TPSRAM IP

TPSRAM IP uses the following configurations:

- Input signal data buffer
- Output signal buffer
- Output signal FFT real data buffer
- Output signal FFT imaginary data buffer

***Table 2 •*** **TPSRAM Configuration for Data Buffers**

| Buffer | Write Port | | Read Port | |
|---|---|---|---|---|
| | Depth | Width | Depth | Width |
| FIR Input Signal | 2048 | 8 | 1024 | 16 |
| FIR Output Signal | 1024 | 16 | 1024 | 16 |
| FFT Output Real Signal | 1024 | 16 | 1024 | 16 |
| FFT Output Imaginary Signal | 1024 | 16 | 1024 | 16 |

### CoreFFT

CoreFFT IP is used to generate the frequency spectrum of the filtered data. CoreFFT IP configuration is as follows:

- Version: 6.4.105
- FFT Architecture: In place
- FFT type: Forward
- FFT Scaling: Conditional
- FFT Transform Size: 256
- Width: 16

### SYSRESET

SYSRESET IP provides the power-on reset signal.

### OSC

OSC IP is configured as an RC oscillator to provide the 50 MHz signal to the CCC (clock conditioning circuit), narrowband component y(n).

### CCC

CCC IP is configured to provide a 100 MHz clock signal

For detailed SmartDesign implementation and resource usage summary, refer to "Appendix 1: SmartDesign Implementation" on page 32.

### CoreUART

The CoreUART IP is used to transfer the data between the host PC (GUI) and the IGLOO2 device. The CoreUART Configuration is as follows:

- Version: 5.5.101
- TxFIFO: Disable
- RxFIFO: Disable
- RxLegacyMode: Disable
- Baud rate: 115200
- Number of bits: 8
- Stop bits: 1
- Parity: None

## Setting Up the Demo Design

The following steps describe how to setup the hardware demo:

1. Connect the jumpers on the IGLOO2 Evaluation Kit board as shown in Table 3.

***Table 3 •*** **IGLOO2 FPGA Evaluation Kit Jumper Settings**

| Jumper | Pin (From) | Pin (To) | Comments |
|---|---|---|---|
| J22 | 1 | 2 | Default |
| J23 | 1 | 2 | Default |
| J24 | 1 | 2 | Default |
| J8 | 1 | 2 | Default |
| J3 | 1 | 2 | Default |

**CAUTION:** While making the jumper connections, the power supply switch **SW7** must be switched OFF.

2. Connect the Power supply to the **J6** connector, switch on the power supply switch, **SW7**.
3. Connect the FlashPro4 programmer to the **J5** connector of the IGLOO2 Evaluation Kit board.
4. Connect the host PC USB port to the **J18** USB connector on the IGLOO2 Evaluation Kit board using the USB mini-B cable.

Figure 7 shows the board setup for running the Adaptive FIR Filter Demo on the IGLOO2 Evaluation Kit.

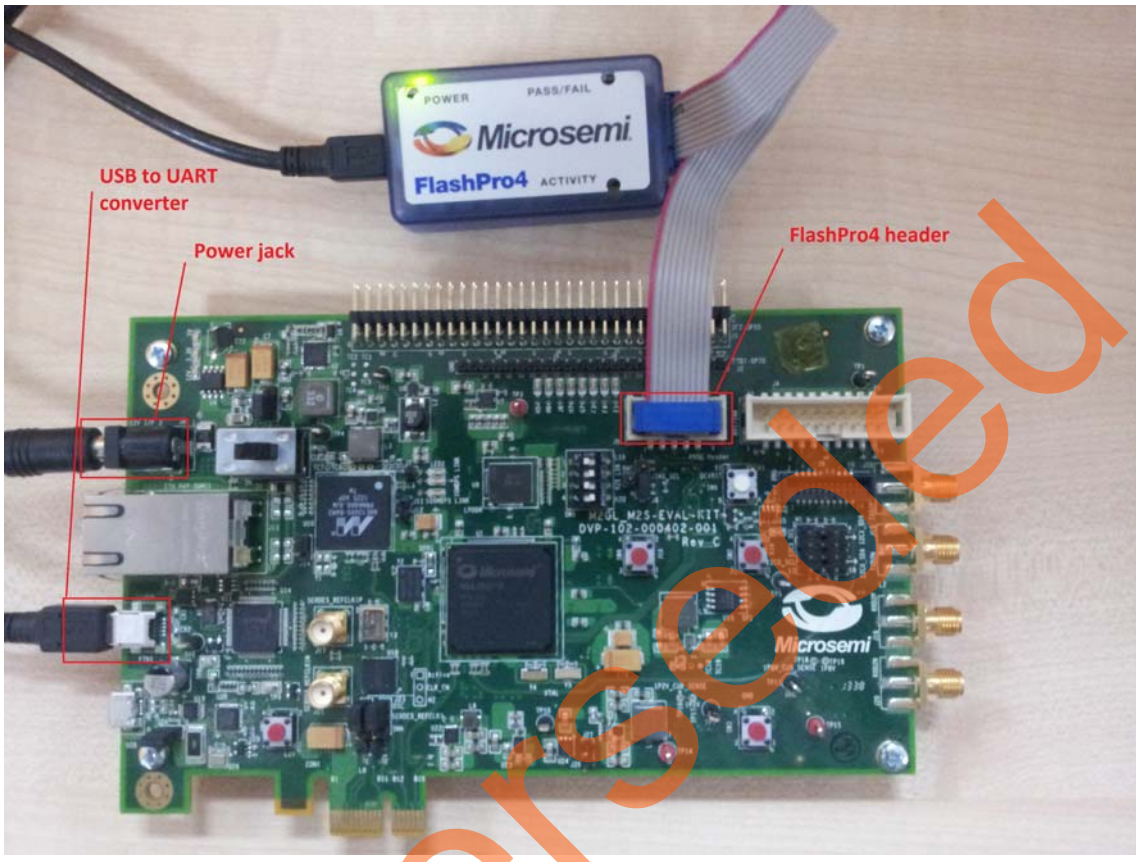


***Figure 7 •*** **IGLOO2 Evaluation Kit Adaptive FIR Filter Demo Setup**

5. Ensure that the USB to UART bridge drivers are automatically detected. This can be verified in the Device Manager of the host PC. The FTDI USB to UART converter enumerates four COM ports. For USB 2.0, note down the USB Serial Converter D COM port number to use it in the IGL2_Adaptive_FIR_Filter.exe.

Figure 8 shows the USB 2.0 Serial port properties and the connected COM10 and USB Serial Converter D.

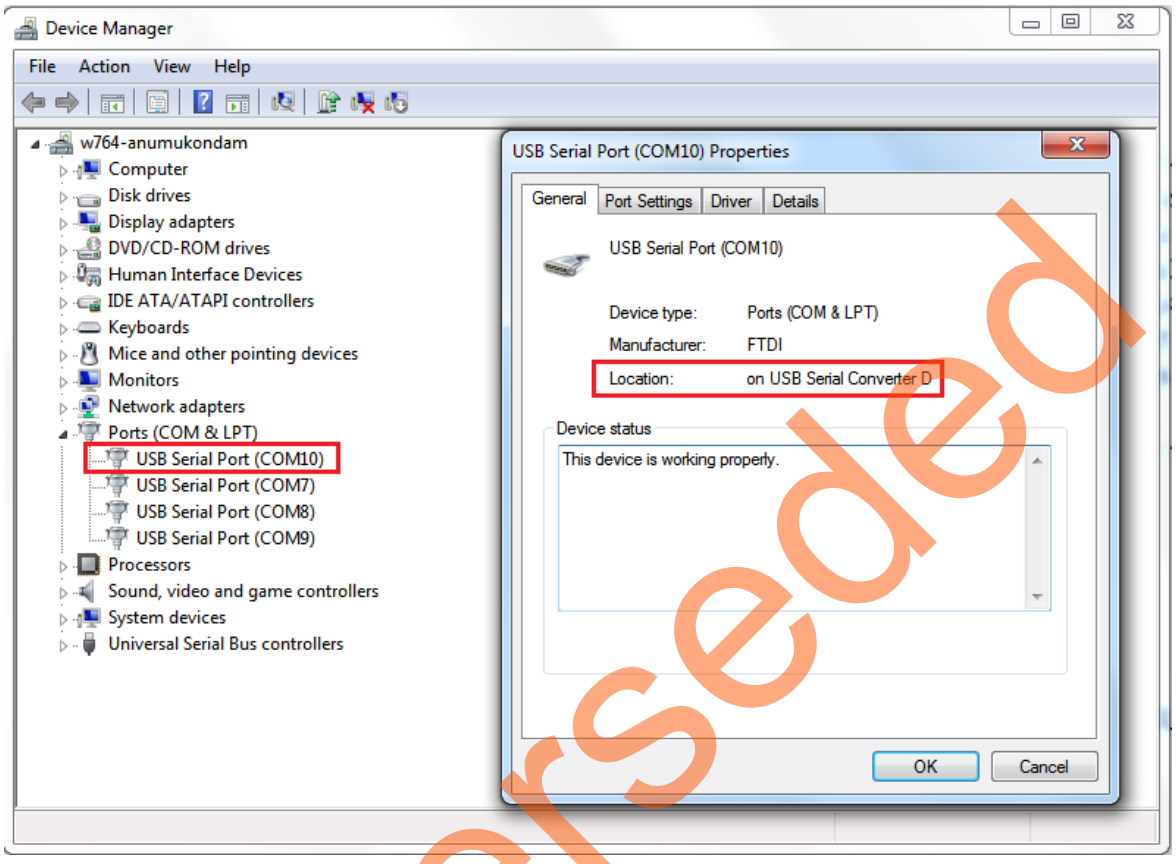


***Figure 8 •*** **USB to UART Bridge Drivers**

6. If the USB to UART bridge drivers are not installed, download and install the drivers from *www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip*.

# Programming the Demo Design

The following steps describe how to program the demo design:

1. Download the demo design from:
   *http://soc.microsemi.com/download/rsc/?f=m2gl_dg0514_adaptive_fir_filter_liberov11p6_df*
2. Launch the FlashPro software.
3. Click **New Project**.

4. In the **New Project** window, enter the project name as `IGL2_Adaptive_FIR_Filter`.

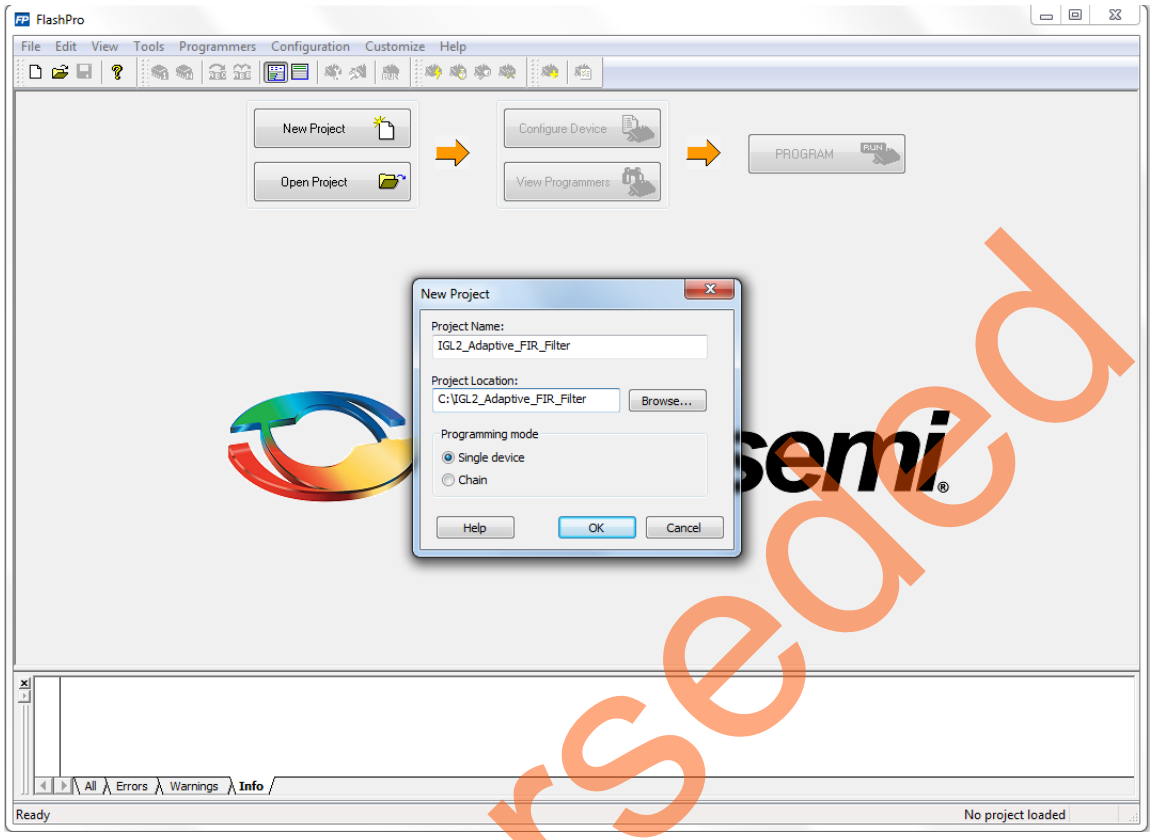


***Figure 9* • FlashPro - New Project**

5. Click **Browse** and navigate to the location where you want to save the project.
6. Select **Single device** as the **Programming mode**.
7. Click **OK** to save the project.

## Setting Up the Device

The following steps describe how to configure the device:

1. Click **Configure Device** on the FlashPro GUI.
2. Click **Browse** and navigate to the location where the `IGL2_Adaptive_FIR_Filter.stp` file is located and select the file. The default location of the programming file is: *<download_folder>/IGLOO2_Adaptive_FIR_Filter_DF\Programmingfile\IGL2_Adaptive_FIR_Filter.stp*.
3. Click **Open**. The required programming file is selected and is ready to be programmed in the device.
4. Select **Advanced** as Mode and **PROGRAM** as Action.

## Programming the Device

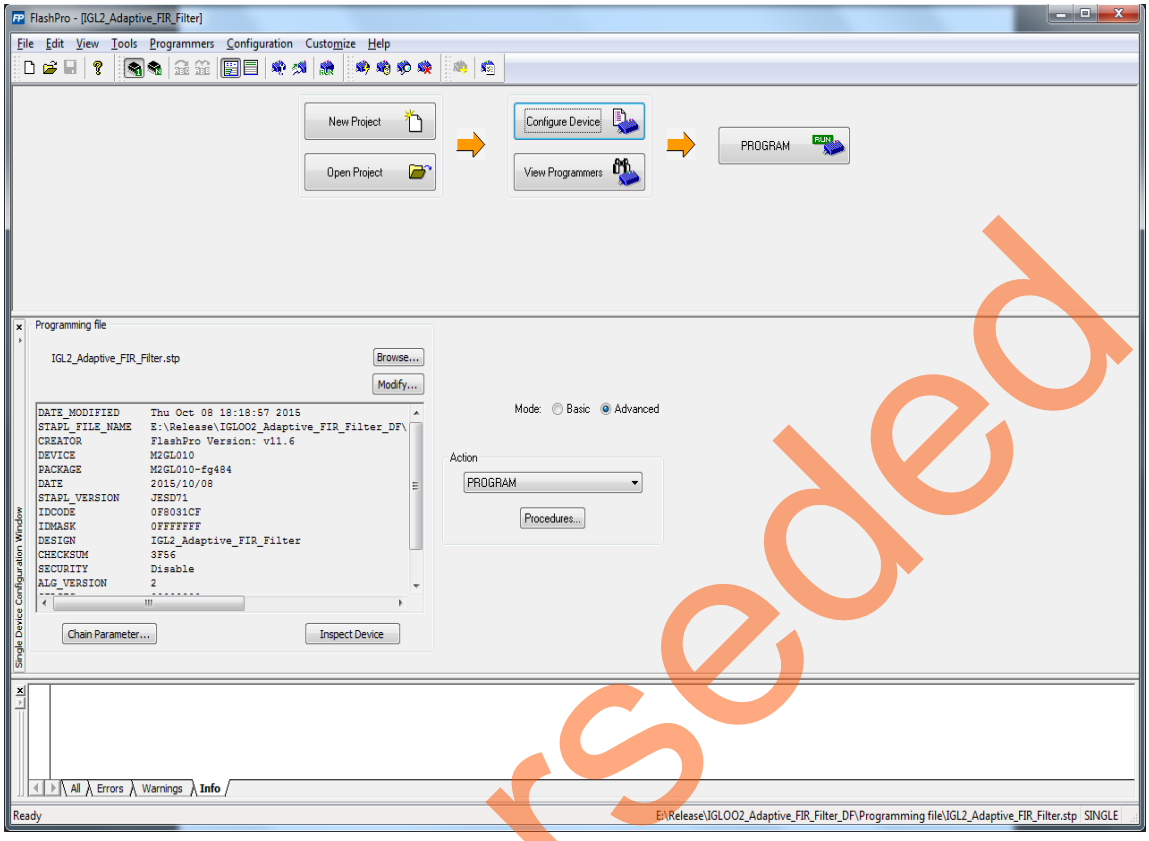


***Figure 10 •*** **FlashPro Project Configuration**

Click **PROGRAM** to start programming the device. Wait until Programmer Status is changed to **RUN PASSED**.

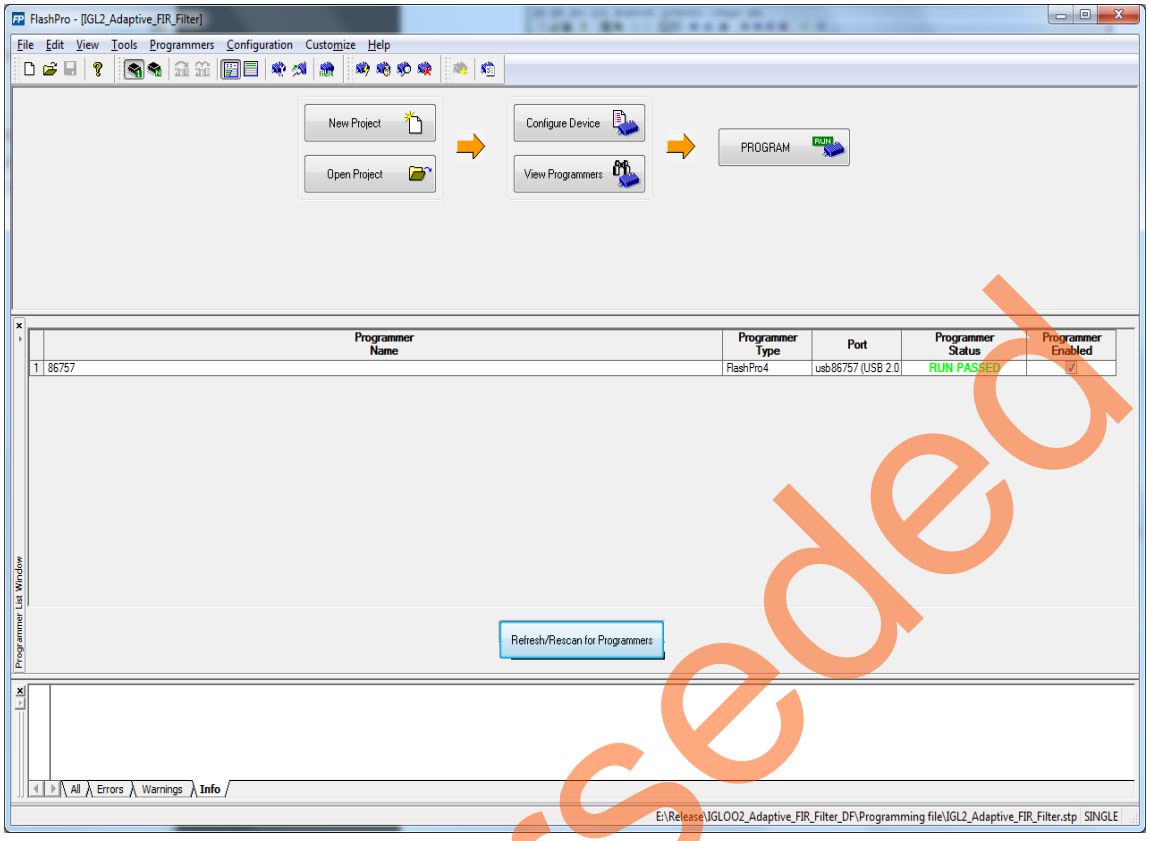


***Figure 11* • FlashPro Project RUN Passed**

## Adaptive FIR Filter Demo GUI

The adaptive FIR filter demo is provided with a user friendly GUI that runs on the host PC and communicates with IGLOO2 Evaluation Kit. UART is used as the communication protocol between the host PC and the IGLOO2 Evaluation Kit.

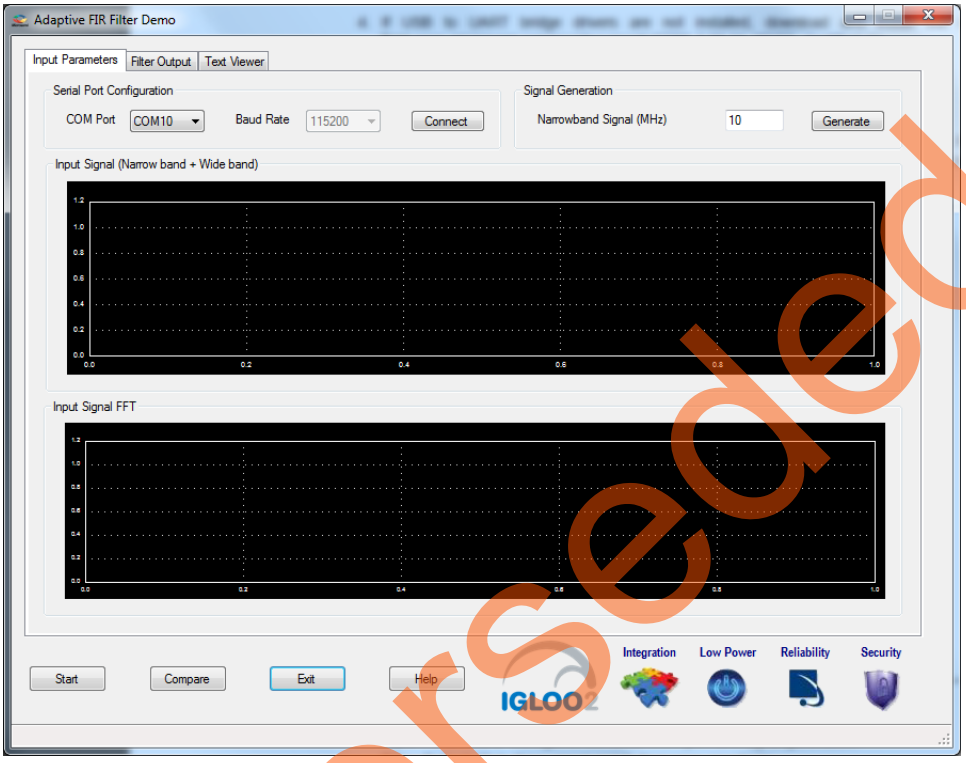


***Figure 12 •*** **Adaptive FIR Filter Demo Window**

The Adaptive FIR Filter Demo window consists of the following tabs:

- **Input Parameters**: Configures the serial COM port and signal generation.
- **Filter Output**: Plots Error signal and its frequency spectrum.
- **Text viewer**: Shows Input signal, Error signal data values.

Click **Help** for more information on the GUI.

# Running the Demo Design

1. Launch the adaptive FIR filter demo GUI, install and invoke the executable file provided with the design files. (*IGLOO2_Adaptive_FIR_Filter_DF\GUI\IGL2_Adaptive_FIR_Filter.exe*). The Adaptive FIR Filter Demo window is displayed, refer to Figure 13.

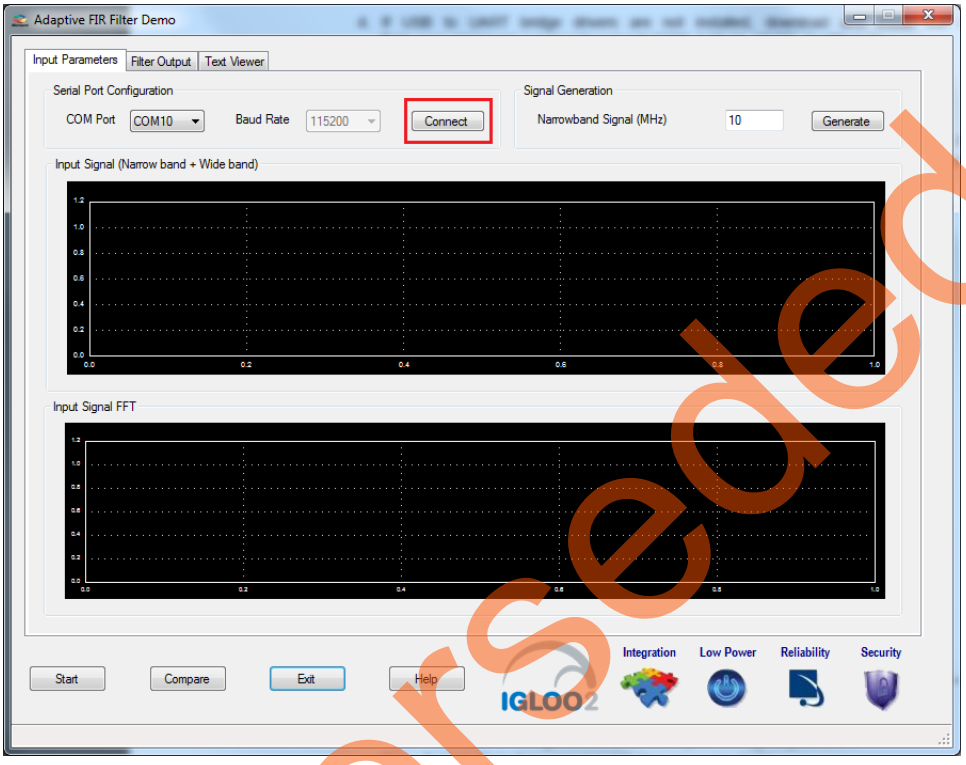


***Figure 13 •*** **Serial Port Configuration**

2. **Serial Port Configuration**: The COM port number is automatically detected and baud rate is fixed at 115200. Click **Connect**. Refer to Figure 13.

3. **Signal Generation**: Enter the narrow band signal frequency as 2 MHz (supported range is 1 MHz and 20 MHz) and click **Generate**. Refer to Figure 14.

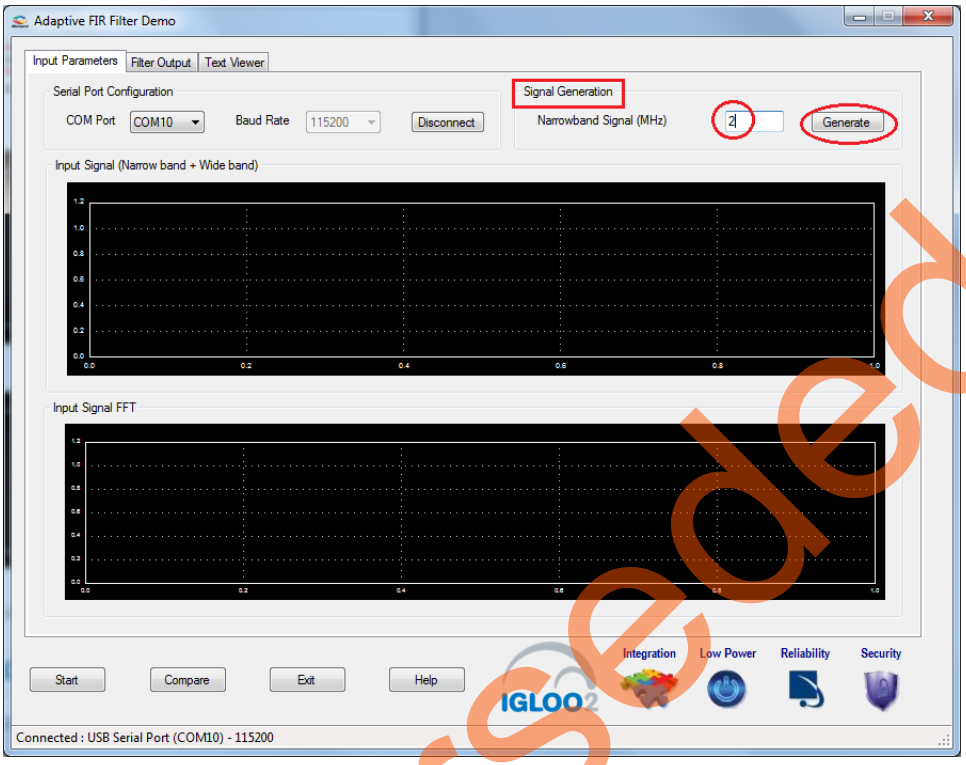


***Figure 14 •*** **Signal Generation**

Adaptive FIR Filter Demo adds the wide band signal (generated inside the Adaptive FIR Filter Demo window) to the narrow band signal component and plots the combined signal (Narrow band and Wide band), FFT spectrum. Refer to Figure 15.


***Figure 15 •*** **Signal Generation**

4. Click **Start** to load the input data (1k samples) to the IGLOO2 device for processing the filtering operation, refer to Figure 16.

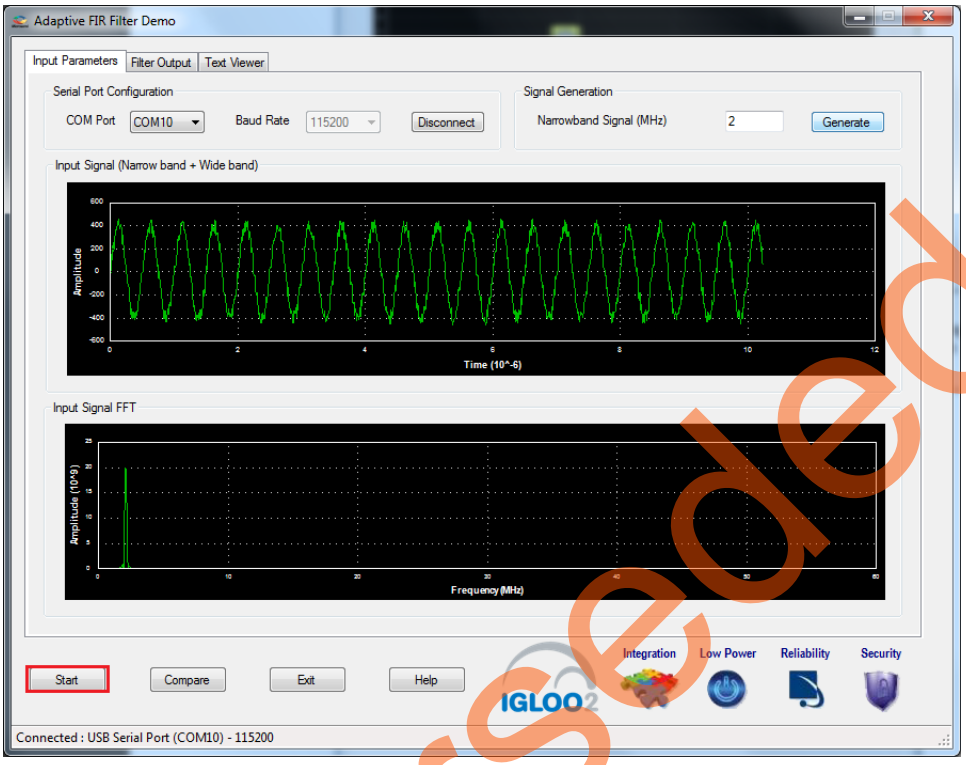


***Figure 16 •*** **Adaptive FIR Filter Demo - Start**

After completing the filter operation, the GUI displays the error data and its FFT data from the IGLOO2 device and plots as shown in Figure 17. The error signal plot shows the suppression of narrow band component from the signal and outputting wide band signals only after the required number of iterations.

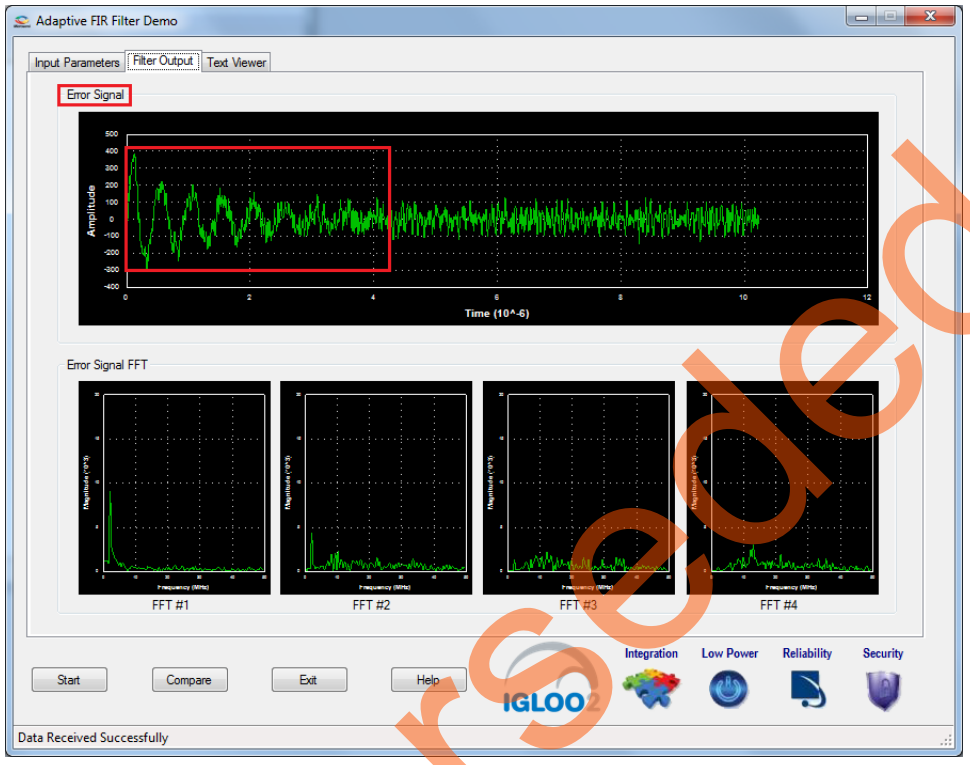


***Figure 17 •*** **Error Signal: Time and Frequency Plot**

The narrow band signal component is suppressed gradually in the Error signal frequency spectrum. This can be observed in the Error signal FFT plot as shown in Figure 18.

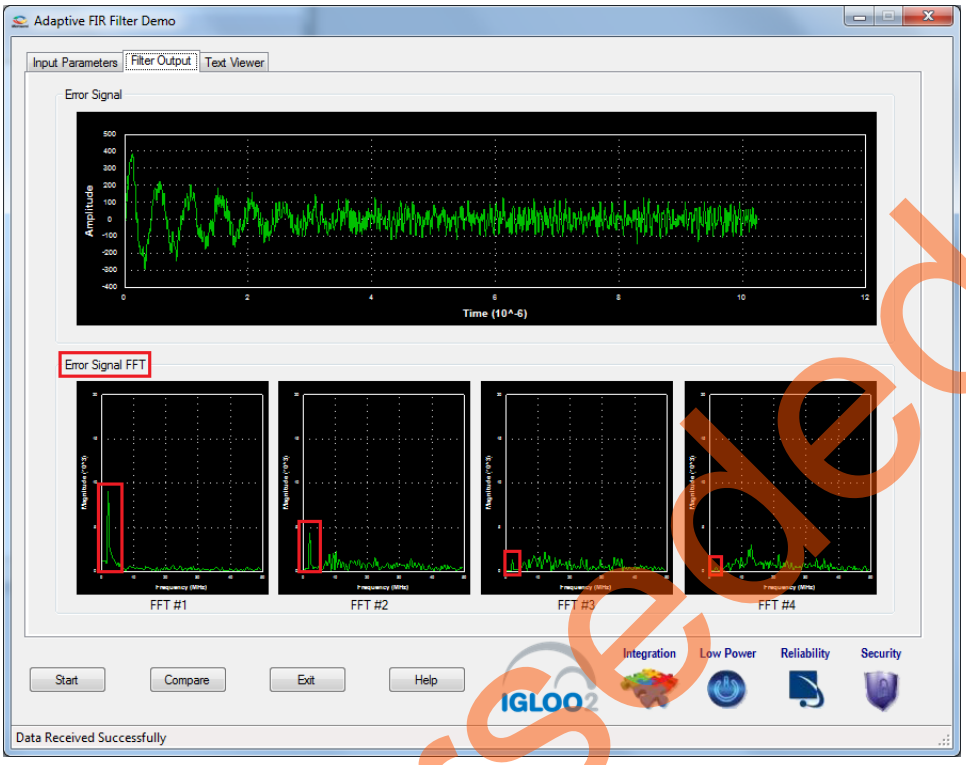


***Figure 18 •*** **Error Signal FFT: Time and Frequency Plot**

5. Click **Compare** to analyze the Input wide band data with the Output wide band data.

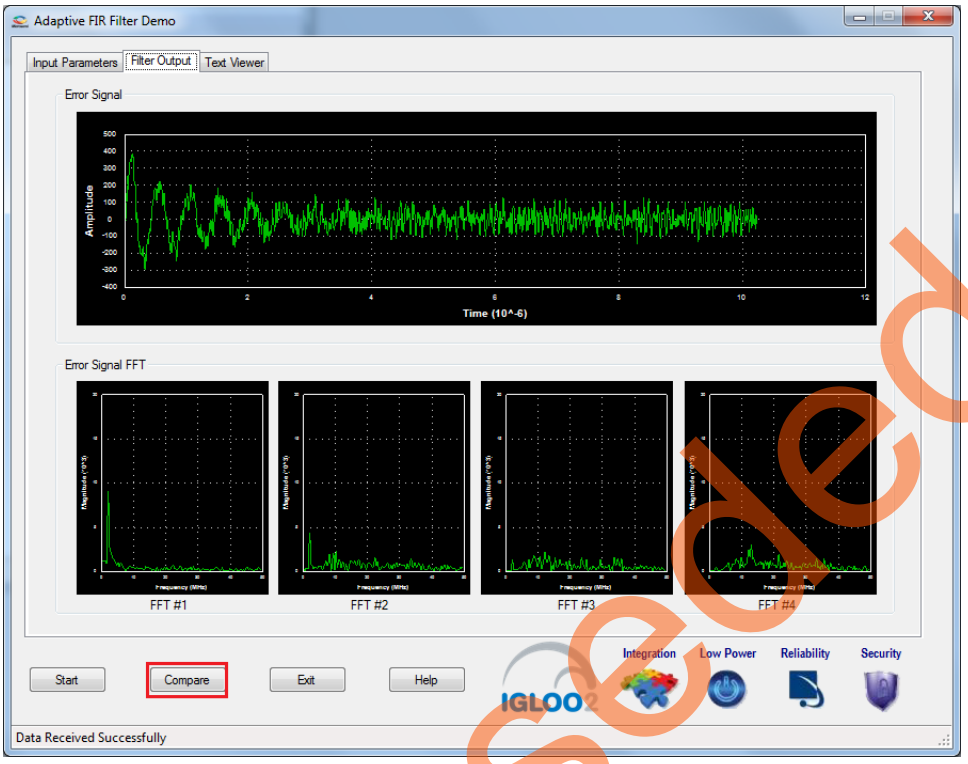


***Figure 19 •*** **Compare Error Signal: Time and Frequency Plot**

A window displaying the comparison between the Input Wide band and Output Wide band is displayed, refer to Figure 20.

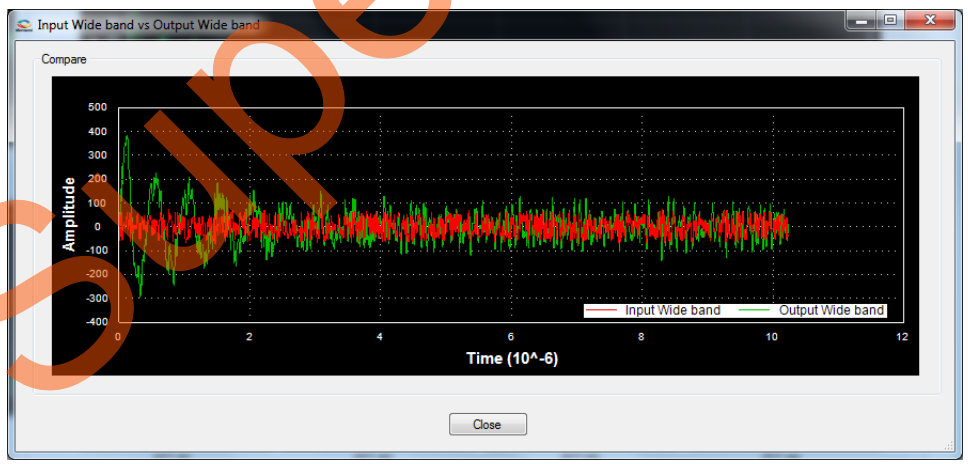


***Figure 20 •*** **Comparison of Input Wide Band and Output Wide Band**

The plot can be zoomed in for comparison, refer to Figure 21.


***Figure 21 •*** **Input Wide Band vs Output Wide Band - Zoomed In**

Compare the Error signal (Output Wide band signal) with the Input Wide band signal, refer to Figure 22. You can see that the narrow band interfering component is eliminated and the wide band signal is preserved in Error signal.


***Figure 22 •*** **Comparison of Input Wide Band and Output Wide Band**

6. Click **Close**, refer to Figure 23.


***Figure 23 •*** **Closing Input Wide Band vs Output Wide Band Window**

7. You can copy, save, export and customize page and configure print setup the Error Signal plot. Right click **Error Signal** plot.
8. From the context sensitive pop up select the required option.

   It shows the different options as shown in Figure 24. The data can be copied, saved, and exported to CSV plot for analysis purpose. Page setup, print, show point values, Zoom, and set scale are set to default.

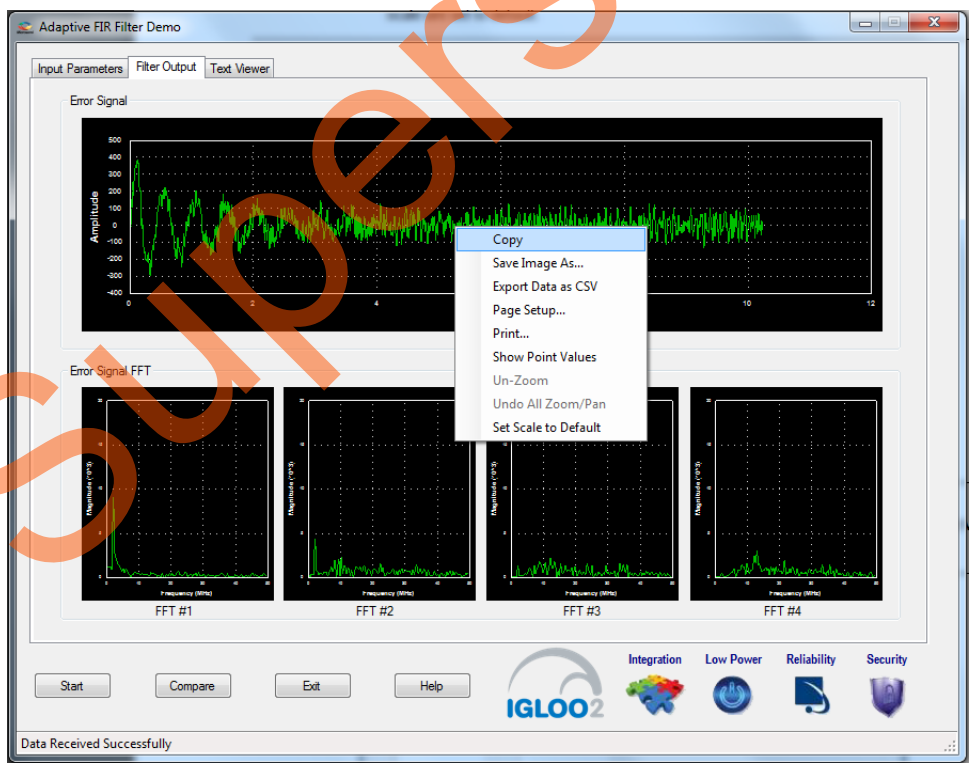


***Figure 24 •*** **Error Signal - GUI Options**

9. The input signal and error signal values can be viewed in the **Text Viewer** tab. Click the **Text Viewer** tab and then click the corresponding **View** shown in Figure 25.

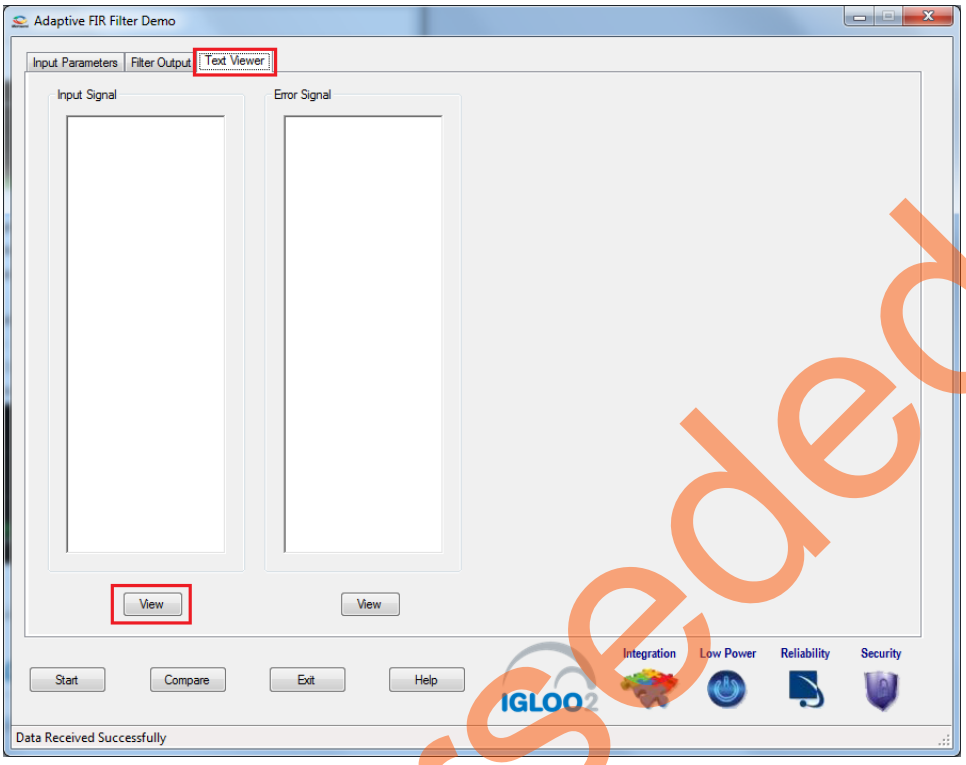


***Figure 25 •*** **Text Viewer**

Figure 26 shows the **Text Viewer** tab showing the **Input Signal** values.

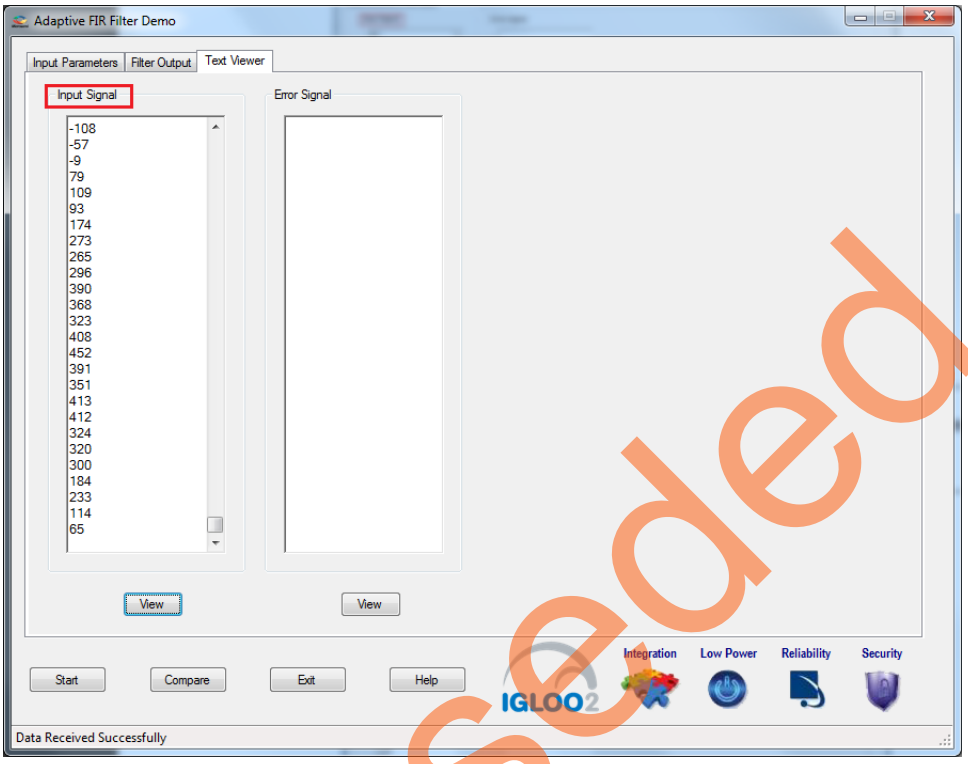


***Figure 26 •*** **Text Viewer: Input Signal Values**

10. To save the Input Signal as a text file, right-click the Input Signal window. The Input Signal window displays different options as shown in Figure 27.
11. Click **Save**. Select **OK** to save the text file.

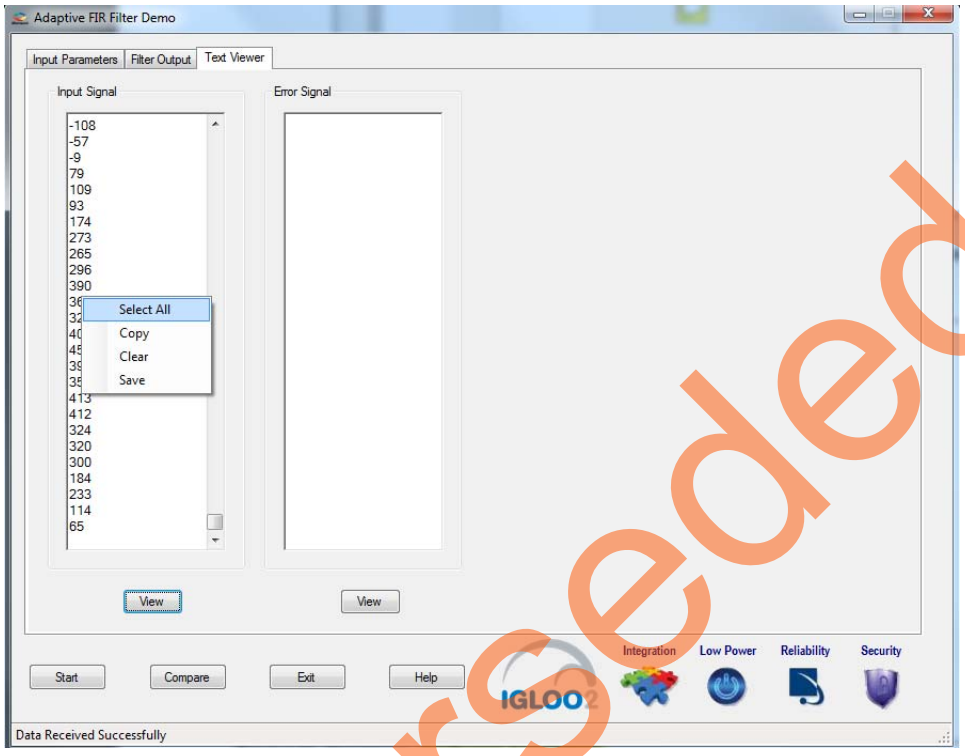


***Figure 27 •*** **Text Viewer - Input Signal Save Option**

12. Click **Exit** to stop the demo, refer to Figure 28.

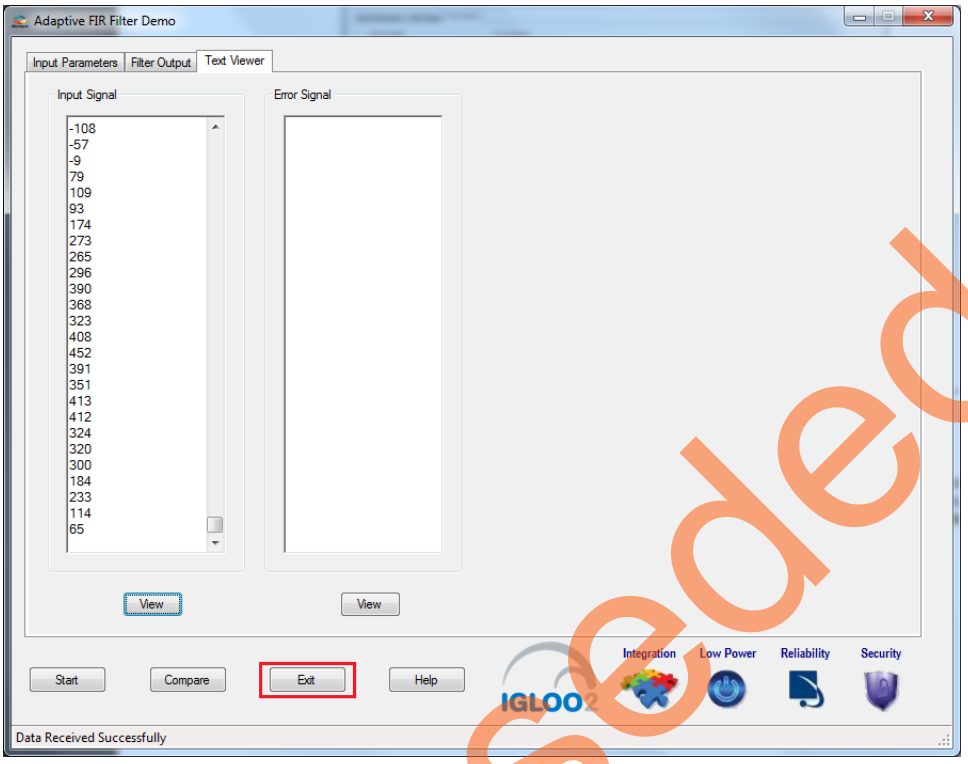


***Figure 28 •*** **Exit Demo**

# Conclusion

This demo provides information about the features of the IGLOO2 device including mathblocks and how to use Microsemi IPs (CoreFIR and CoreFFT) for narrow band interference cancellation application using Adaptive FIR filters. This Adaptive FIR Filter based demo is easy to use and provides several options to understand and implement DSP filters on the IGLOO2 device.

# Appendix 1: SmartDesign Implementation

Adaptive FIR filter SmartDesign is shown in Figure 1.

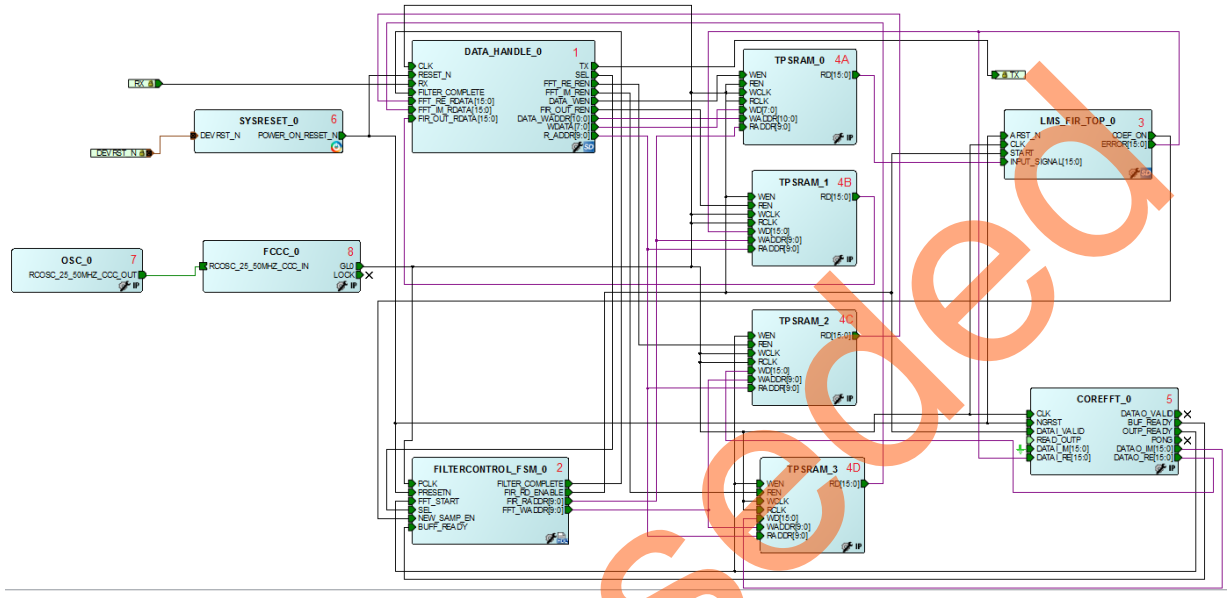


***Figure 1 •*** **Adaptive FIR Filter SmartDesign**

SmartDesign LMS_FIR_TOP is shown in Figure 2.

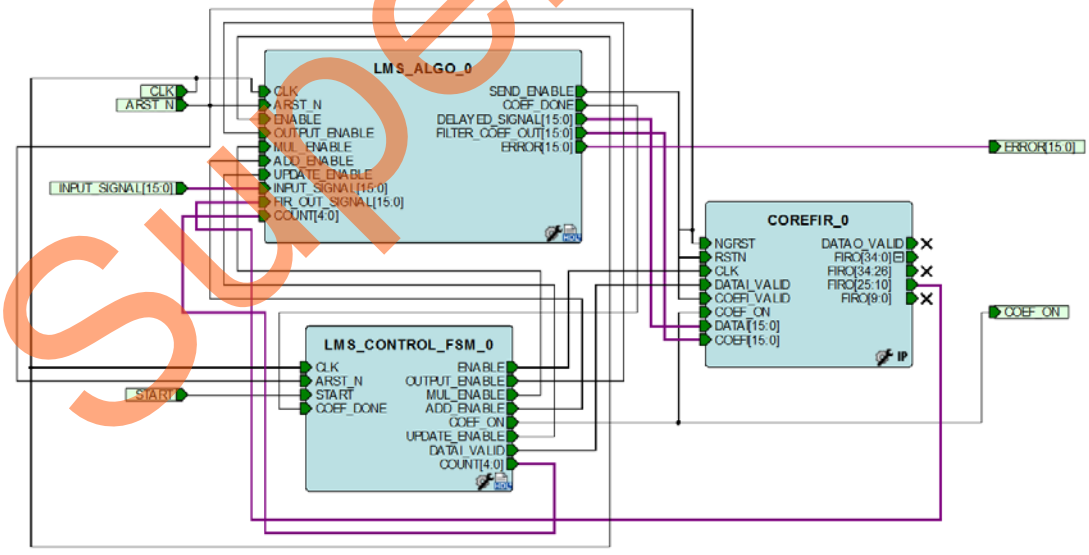


***Figure 2 •*** **SmartDesign LMS_FIR_TOP**

Table 1 shows SmartDesign blocks in Adaptive FIR Filter.

***Table 1 •*** **Adaptive FIR Filter Demo SmartDesign Blocks and Description**

| S.No | Block Name | Description |
|---|---|---|
| 1 | DATAHANDLE_0 | Handles communication between the host PC and IGLOO2 Evaluation Kit board. |
| 2 | FILTERCONTROL_FSM_0 | Control logic to generate the control signals for FIR and FFT operations. |
| 3 | LMS_FIR_TOP | SmartDesign. |
| 4 | INPUT_Buffer | FIR input signal data buffer. |
| | OUTPUT_Buffer | FIR output signal buffer. |
| | FFT_Im_Buffer | FFT output imaginary data buffer. |
| | FFT_Re_Buffer | FFT output real data buffer. |
| 5 | COREFFT_0 | COREFFT IP. |
| 6 | SYSRESET_0 | Reset IP. |
| 7 | OSC_0 | Oscillator IP. |
| 8 | FCCC_0 | Clock conditioning circuit IP. |

Table 2 shows SmartDesign blocks in LMS_FIR_TOP.

***Table 2 •*** **LMS_FIR_TOP SmartDesign Blocks and Description**

| S.No | Block Name | Description |
|---|---|---|
| 1 | LMS_ALGO | LMS algorithm implemented in the RTL to compute error, correction factor, and filter coefficients. |
| 2 | LMS_CONTROL_FSM | FSM implemented in the RTL to control LMS_ALGO block. |
| 3 | COREFIR | COREFIR IP. |

# Appendix 2: Resource Usage Summary

Table 1 shows adaptive FIR filter demo resource usage summary.

**Device**: IGLOO2 device

**Die**: M2GL010

**Package**: 484 FBGA

***Table 1 •*** **Adaptive FIR Filter Demo Resource Usage Summary**

| Type | Used | Total | Used vs Total in Percentage (%) |
|---|---|---|---|
| 4LUT | 2997 | 12084 | 24.80 |
| DFF | 2905 | 12084 | 24.04 |
| RAM1Kx18 | 11 | 21 | 52.38 |
| MACC | 13 | 22 | 59.09 |

Table 2 shows MACC blocks usage summary.

***Table 2 •*** **MACC Blocks Usage Summary**

| CoreFIR | CoreFFT | LMS_ALGO | Total |
|---|---|---|---|
| 8 | 04 | 1 | 13 |

Table 3 shows RAM1Kx18 blocks usage summary.

***Table 3 •*** **RAM1Kx18 Blocks Usage Summary**

| CoreFIR | CoreFFT | Fabric Buffers | Total |
|---|---|---|---|
| 0 | 7 | 4 | 11 |

# A – List of Changes

The following table shows important changes made in this document for each revision.

| Date | Changes | Page |
|---|---|---|
| Revision 5 (October 2015) | Updated the document for Libero v11.6 software release (SAR 72357). | NA |
| Revision 4 (January 2015) | Updated the document for Libero v11.5 software release (SAR 63925). | NA |
| Revision 3 (August 2014) | Updated the document for Libero v11.4 software release (SAR 59680). | NA |
| Revision 2 (June 2014) | Updated the document for Libero v11.3 software release (SAR 56264). | NA |
| | The "Theory of Operation" section updated (SAR 56264). | 6 |
| | Figure 6 updated (SAR 56264). | 10 |
| Revision 1 (January 2014) | Initial Release | NA |

# B – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

## Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

## Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

## Technical Support

For Microsemi SoC Products Support, visit

http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

## Website

You can browse a variety of technical and non-technical information on the SoC home page, at http://www.microsemi.com/products/fpga-soc/fpga-and-soc.

## Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

### Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

### My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

### Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

## ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech@microsemi.com. Alternatively, within My Cases, select Yes in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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