Error Detection and Correction on SmartFusion2 Devices using DDR Memory - Libero SoC v11.6

DG0618 Demo Guide

Superseded

November 2015

Microsemi

Revision History

Date	Revision	Change
4 November 2015	2	Second release
27 May 2015	1	First release

Confidentiality Status

This is a non-confidential document.

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Preface

About this document

This demo is for Microsemi® SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) error detection and correction (EDAC) capabilities. It provides instructions about how to use the corresponding reference design.

Intended Audience

SmartFusion2 EDAC using double data rate (DDR) memory capabilities are used by:

- FPGA designers
- Embedded designers
- System-level designers

References

Microsemi Publications

- *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*
- *UG0446: SmartFusion2 SoC FPGA and IGLOO2 FPGA High Speed DDR Interfaces User Guide*

Refer to the following web page for a complete and up-to date list of SmartFusion2 device documentation: *http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#documents*.

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Error Detection and Correction on SmartFusion2 Devices using DDR Memory

Introduction

In a single event upset (SEU) susceptible environment, random access memory (RAM) is prone to transient errors caused by heavy ions.

This document describes the EDAC capabilities of the SoC FPGA, which are used in applications with memories connected through the microcontroller subsystem (MSS) DDR subsystem (MDDR).

The EDAC controllers implemented in the SmartFusion2 SoC FPGA devices support single error correction and double error detection (SECDED). All memories eSRAM, DDR, LPDDR – within the MSS of the SmartFusion2 SoC FPGA devices are protected by SECDED. The DDR synchronous dynamic random access memory (SDRAM) memory can be DDR2, DDR3, or low power DDR (LPDDR1), depending on the MDDR configuration and hardware ECC capabilities.

The MDDR subsystem in the SmartFusion2 devices supports memory densities up to 4 GB. In this demo, you have a provision to select any memory location of 1 GB in the DDR address space (0xA0000000 to 0xDFFFFFFF).

When SECDED is enabled:

- A write operation computes and adds 8 bits of SECDED code (to every 64 bits of data)
- A read operation reads and checks the data against the stored SECDED code to support 1-bit error correction and 2-bit error detection.

Figure 1 shows the block diagram of SmartFusion2 EDAC on DDR SDRAM.

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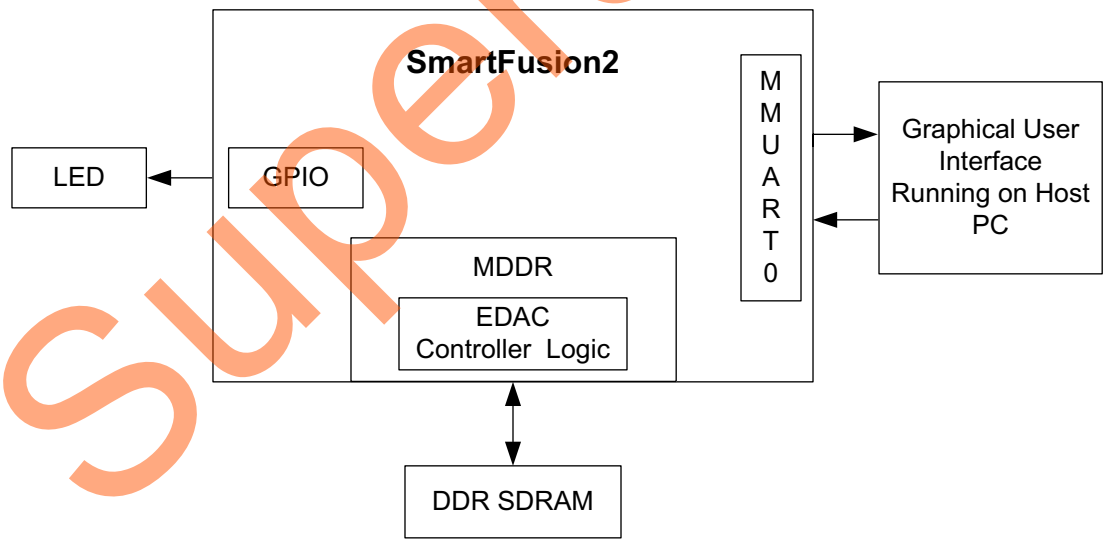

Figure 1 • **Top-Level Block Diagram**

The EDAC feature of DDR supports the following:

1. SECDED mechanism.
2. Provides interrupts to the ARM® Cortex®-M3 processor and FPGA fabric upon the detection of a 1-bit error or 2-bit error.
3. Stores the number of 1-bit and 2-bit errors in error counter registers.
4. Stores the address of the last 1-bit or 2-bit error affected memory location.
5. Stores the 1-bit or 2-bit error data in SECDED registers.
6. Provides error bus signals to the FPGA fabric.

Refer to the EDAC chapter of the *UG0443: SmartFusion2 and IGLOO2 FPGA Security and Reliability User Guide* and *UG0446: SmartFusion2 and IGLOO2 FPGA High Speed DDR Interfaces User Guide*.

Design Requirements

Table 1 shows the design requirements.

Table 1 • **Design Requirements**

Design Requirements	**Description**
Hardware Requirements	
SmartFusion2 SoC FPGA Advanced Development Kit board	Rev D or later
FlashPro4 programmer or later	–
USB A to mini-B USB cable	–
Power adapter	12 V
DDR3 Daughter board	–
Operating System	Any 64-bit or 32-bit Windows XP SP2 Any 64-bit or 32-bit Windows 7
Software Requirements	
Libero® System-on-Chip (SoC)	v11.6
FlashPro programming software	v11.6
Host PC Drivers	USB to UART drivers
Framework to run demonstration	Microsoft .NET Framework 4 client

Demo Design

The demo design files are available for downloading from the following path in the Microsemi website: *http://soc.microsemi.com/download/rsc/?f=m2s_dg0618_liberov11p6_df*

The demo design files include:

- DDR Configuration File
- DDR_EDAC
- Programming files
- GUI executable
- Readme file

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Figure 2 shows the top-level structure of the design files. For further details, see the `readme.txt` file.

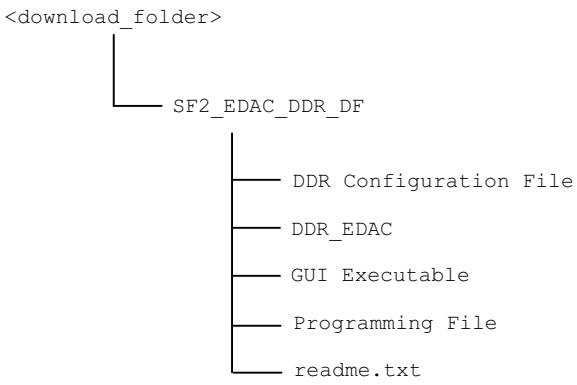

Figure 2 • **Demo Design Top-level Structure**

Demo Design Implementation

The MDDR subsystem has a dedicated EDAC controller. EDAC detects a 1-bit error or 2-bit error when data is read from the memory. If EDAC detects the 1-bit error, the EDAC controller corrects the error bit. If EDAC is enabled for all the 1-bit and 2-bit errors, corresponding error counters in the system registers are incremented and corresponding interrupts and error bus signals to the FPGA fabric are generated.

This happens in real-time. To demonstrate this SECDED feature, an error is introduced manually and detection and correction is observed.

This demo design involves implementation of following tasks:

1. Enable EDAC.
2. Write data to DDR.
3. Read data from DDR.
4. Disable EDAC.
5. Corrupt one or two bits.
6. Write data to DDR.
7. Enable EDAC.
8. Read the data.
9. In the case of a 1-bit error, the EDAC controller corrects the error, updates the corresponding status registers, and gives the data written in Step 2 at the read operation done at Step 8.
10. In the case of a 2-bit error, a corresponding interrupt is generated and the application must correct the data or take the appropriate action in the interrupt handler. These two methods are demonstrated in this demo.

Two tests are implemented in this demo: loop test and manual test and they are applicable to both 1-bit and 2-bit errors.

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Loop Test

Loop test is executed when the SmartFusion2 SoC FPGA devices receive a loop test command from the GUI. Initially, all the error counters and EDAC related registers are placed in the RESET state.

The following steps are executed for each iteration.

1. Enable the EDAC controller.
2. Write the data to the specific DDR memory location.
3. Disable the EDAC controller.
4. Write the 1-bit or 2-bit error induced data to the same DDR memory location.
5. Enable the EDAC controller.
6. Read the data from the same DDR memory location.
7. Send the 1-bit or2-bit error detection and 1-bit error correction data in case of 1-bit error to the GUI.

Manual Test

This method allows manual testing of 1-bit error detection and correction and 2-bit error detection for DDR memory address (0xA0000000 to 0xDFFFFFFF) with initialization. A 1-bit/2-bit error is introduced manually to a selected DDR memory address. The given data is written to the selected DDR memory location with EDAC enabled. The corrupted 1-bit or 2-bit error data is then written to the same memory location with EDAC disabled. The information on the detected 1-bit or 2-bit error is logged when the data is read from the same memory location with EDAC enabled. The high-performance DMA controller (HPDMA) is used to read the data from the DDR memory. The dual-bit error detection interrupt handler is implemented to take the appropriate action when a 2-bit error is detected.

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Figure 3 shows the EDAC demo operations.

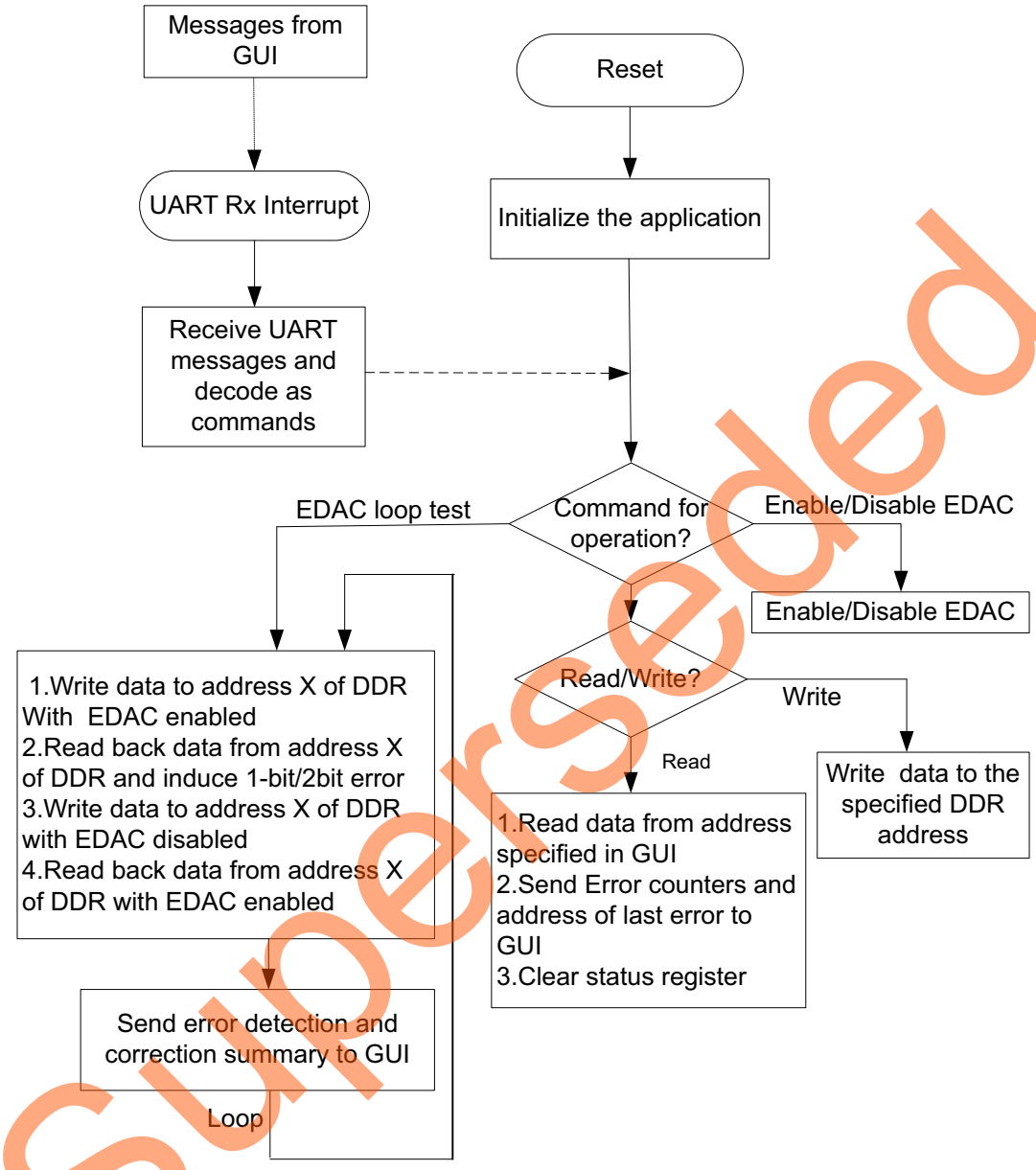

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Figure 3 • **Design Flow**

Note: For a 2-bit error, when the Cortex-M3 processor reads the data, the code execution goes in to the hard fault handler, as the interrupt received is late for the processor to respond. By the time it responds to the interrupt, it may have already passed the data and accidentally launched a command. As a result, the HRESP stops processing the incorrect data. 2-bit error detection uses HPDMA to read the data from the DDR address location, which instructs the processor that read data has a 2-bit error and the system should take appropriate action to recover (ECC interrupt Handler).

Setting Up the Demo Design

This section describes the SmartFusion2 Advanced Development Kit board setup, the GUI options, and how to execute the demo design.

The following steps describe how to setup the demo:

1. Connect one end of the USB mini-B cable to the **J33** connector provided in the SmartFusion2 Advanced Development Kit board. Connect the other end of the USB cable to the host PC. Light emitting diode (LED) DS27 should light up, indicating the UART link has been established. Ensure that the USB to UART bridge drivers are automatically detected (can be verified in the **Device Manager**), as shown in Figure 4.
2. Copy the COM port number for serial port configuration.

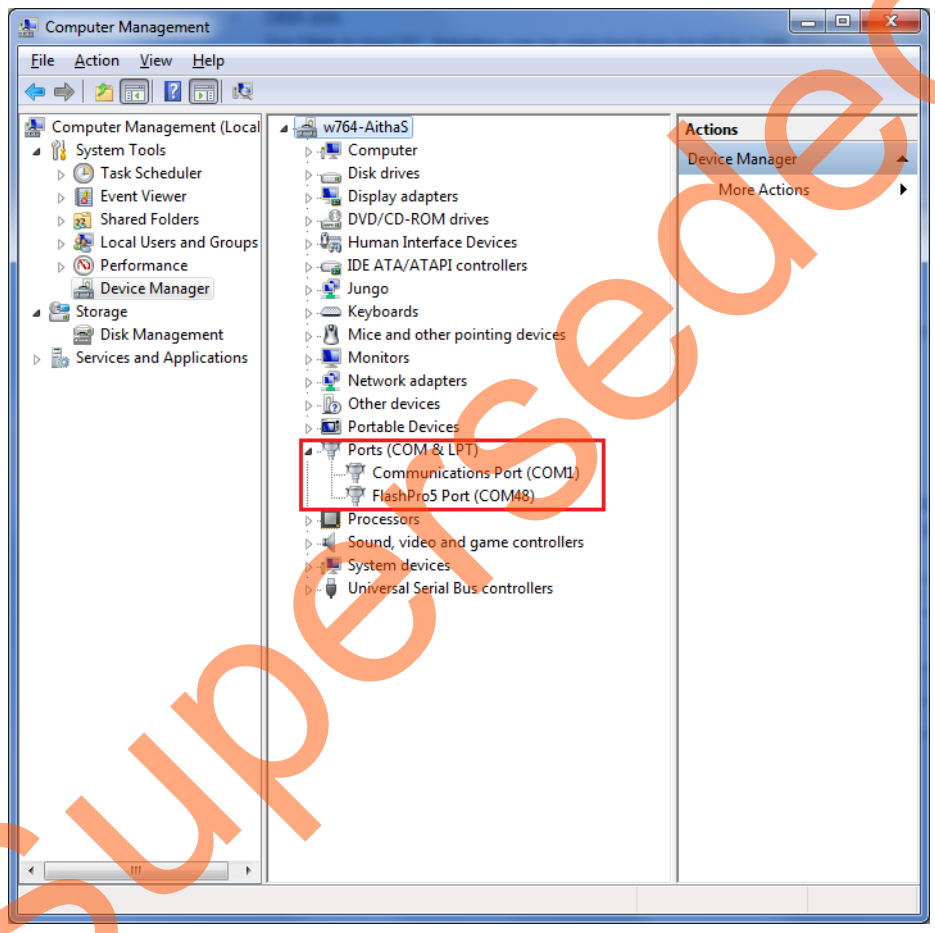

Figure 4 • **USB to UART Bridge Drivers**

3. If USB to UART bridge drivers are not installed, download and install the drivers from www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip.

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4. Connect the jumpers on the SmartFusion2 Advanced Development Kit board, as shown in Table 4 on page 16. The power supply switch **SW7** must be switched **OFF**, while making the jumper connections.

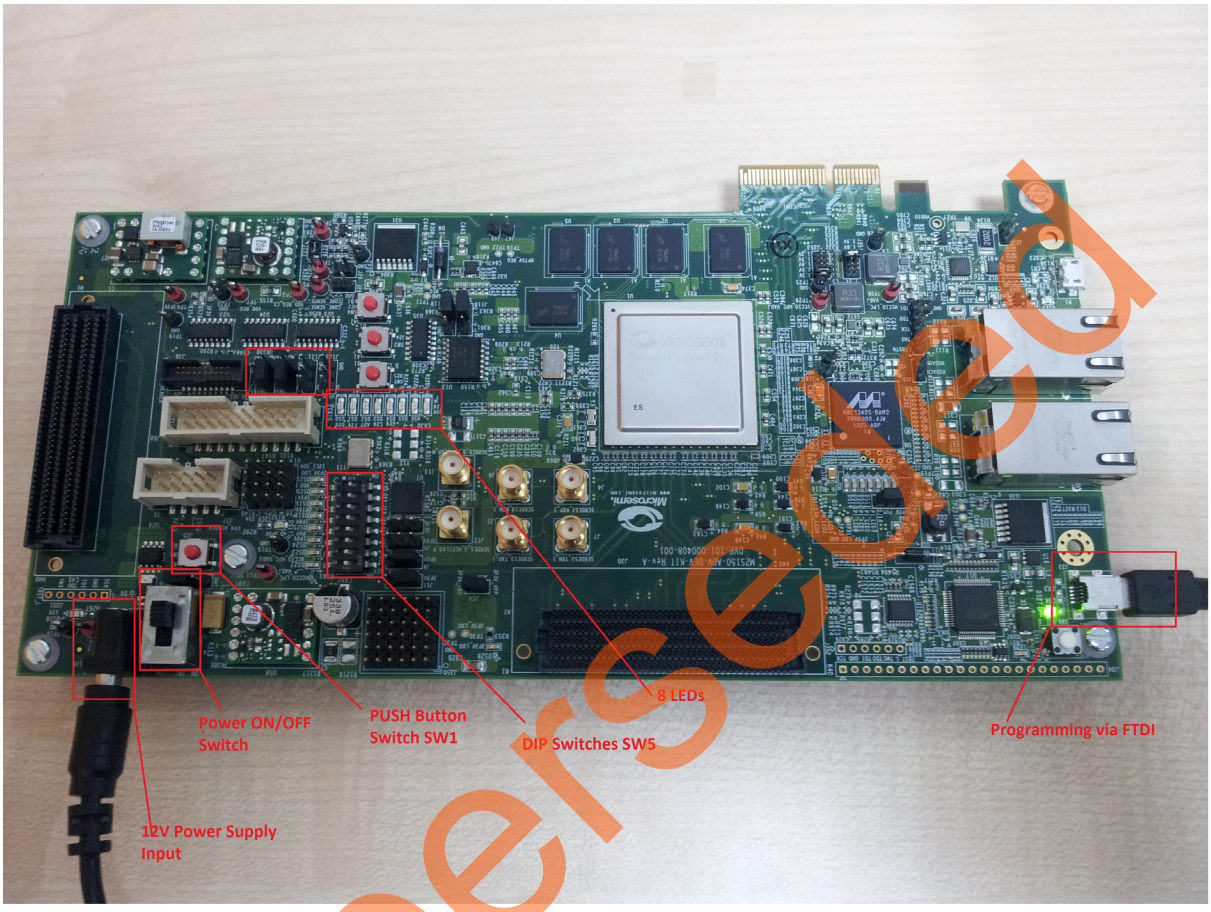

Figure 5 • **SmartFusion2 Advanced Development Kit Board Setup**

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Graphical User Interface

The following section describes the DDR – EDAC Demo GUI.

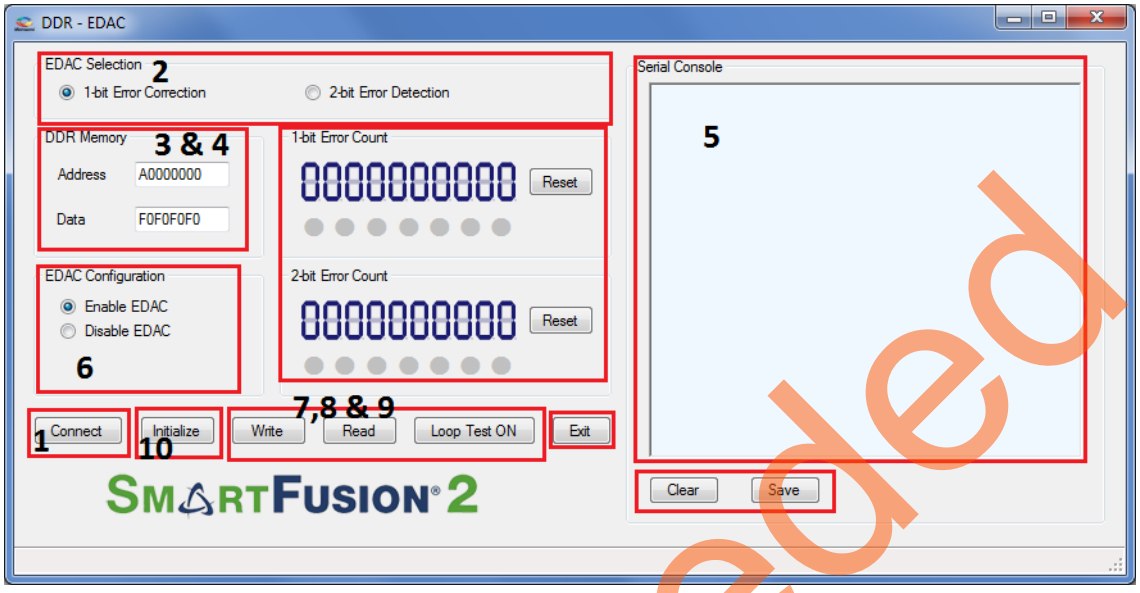

Figure 6 • **DDR – EDAC Demo GUI**

The GUI supports the following features:

1. Selection of COM port and Baud Rate.
2. Selection of 1-bit error correction tab or 2-bit error detection.
3. Address field to write or read data to or from specified DDR address.
4. Data field to write or read data to or from specified DDR address.
5. Serial Console section to print the status information received from the application.
6. **Enable EDAC/Disable EDAC**: Enables or disables the EDAC.
7. **Write:** Allows writing data to the specified address.
8. **Read:** Allows reading data from the specified address.
9. **LOOP test ON/OFF:** Allows testing the EDAC mechanism in a loop method.
10. **Initialize:** Allows to initialize the predefined memory location (in this demo A0000000-A000CFFF).

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Running the Demo Design

The following steps describe how to run the design:

1. Switch **ON** the supply switch, **SW7**.
2. Program the SmarFusion2 device with the programming file provided in the design files (`\ProgrammingFile\EDAC_DDR3.stp`) using FlashPro design software, as shown in Figure 7.

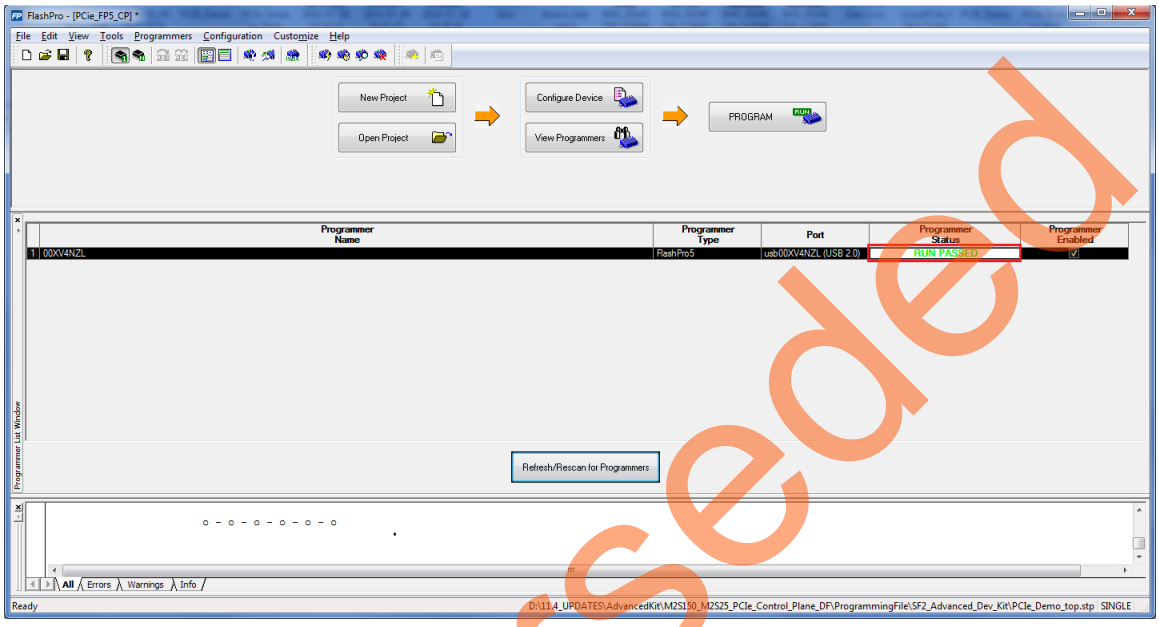

Figure 7 • **FlashPro Programming Window**

3. Press **SW6** switch to reset the board after successful programming.
4. Launch the **EDAC_DDR Demo** GUI executable file available in the design files (`\GUI Executable\ EDAC_DDR.exe`). The GUI window is displayed, as shown in Figure 8 on page 14.
5. Click **Connect**, it will automatically select the COM port and establishes the connection, **Connect** changes to **Disconnect**.
6. Select the **1-bit Error Correction** tab or **2-bit Error Detection**.
7. Two types of tests can be performed: Manual and Loop.

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8. Click **Initialize** to initialize the DDR memory to perform the Manual and Loop tests, an **initialization completion** message is displayed on Serial Console, as shown in Figure 8.

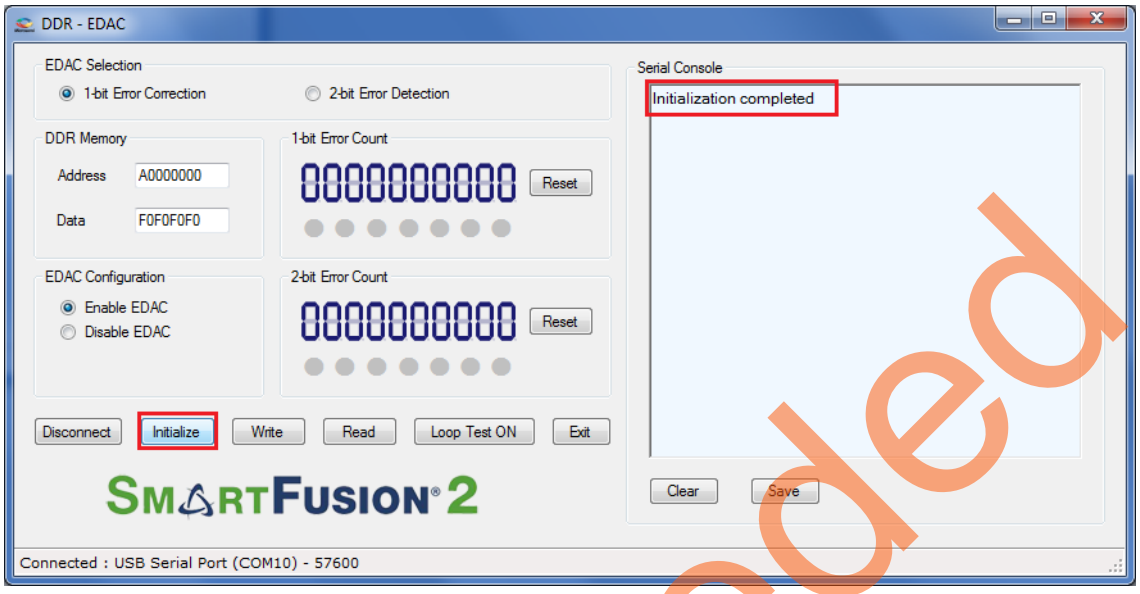

Figure 8 • **Initialization Completed Window**

Performing Loop Test

Click **Loop Test ON**. It runs in loop mode where continuous correction and detection of errors is done. All actions performed in the SmartFusion2 SoC FPGA are logged in the **Serial Console** section of the GUI.

Table 2 • **DDR3 Memory Addresses used in Loop Test**

Memory	DDR3
1-bit error correction	0xA0008000
2-bit error detection	0xA000C000

Performing Manual Test

In this method, errors are introduced manually using GUI. Use the following steps to execute 1-bit error correction or 2-bit error detection.

Table 3 • **DDR3 Memory Addresses used in Manual Test**

Memory	DDR3
1-bit error correction	0xA0000000-0xA0004000
2-bit error detection	0xA0004000-0xA0008000

Input Address and Data fields (use 32-bit Hexadecimal values).

1. Click **Enable EDAC** and click **Select**.
2. Click **Write**.
3. Click **Disable EDAC** and click **Select**.
4. Just change one bit (in case of 1-bit error correction) or two bits (in case of 2-bit error detection) in **Data** field (introducing error).

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The 1-bit error loop correction window is shown in Figure 9.

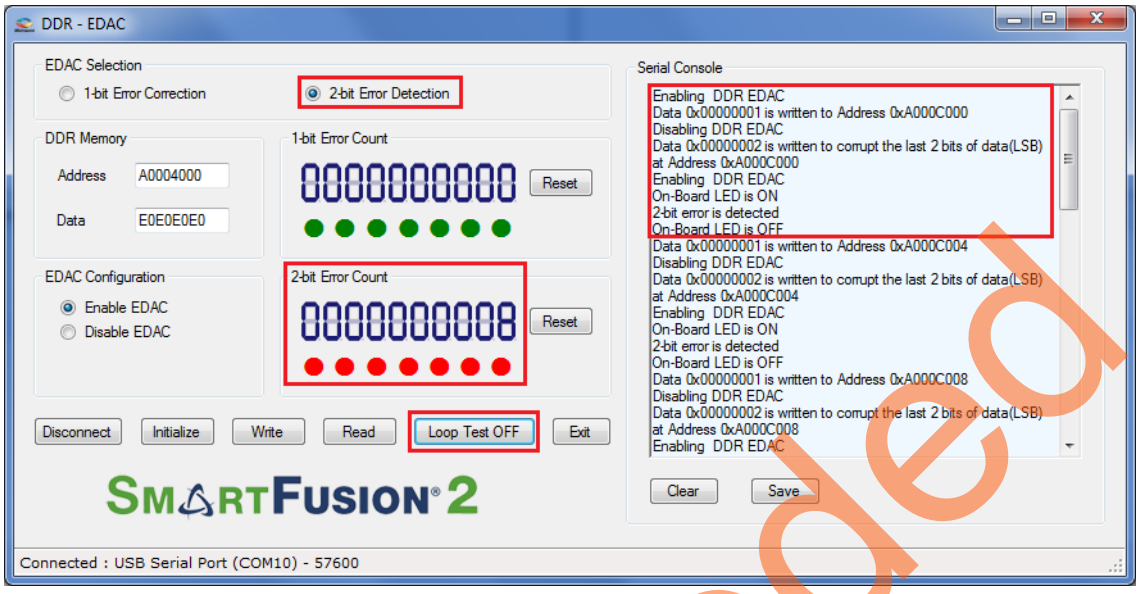

Figure 9 • **2-bit Error Loop Detection Window**

The 1-bit error loop correction window is shown in Figure 10.

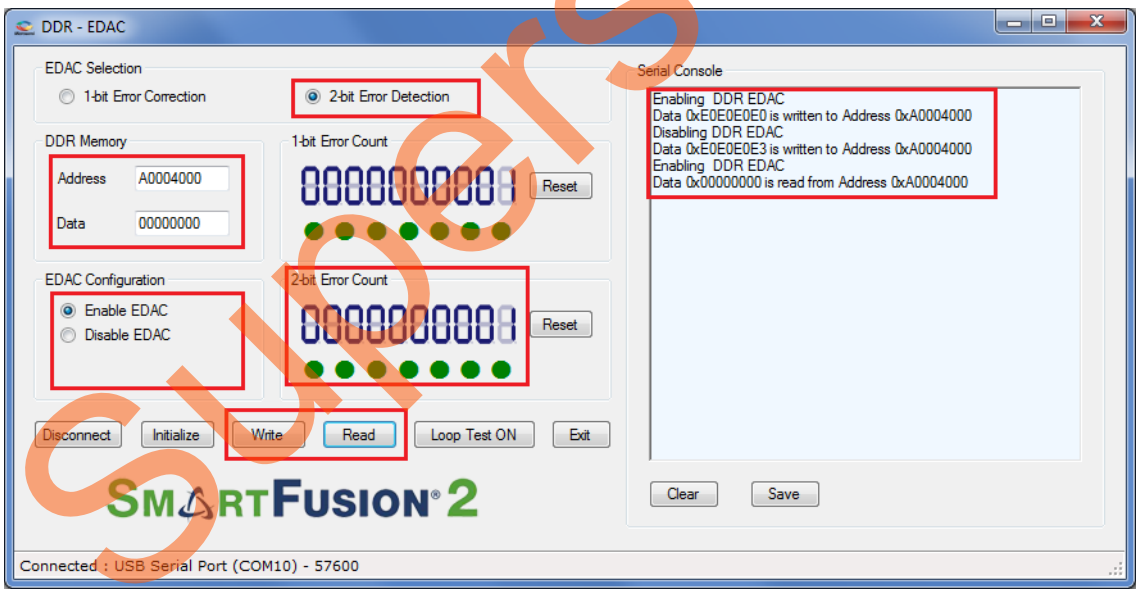

Figure 10 • **2-bit Error Detection Manual Window**

Conclusion

This demo shows SmartFusion2 SECDED capabilities for the MDDR subsystem.

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Appendix: Jumper Settings

Table 4 shows all the jumpers that are required to set on the SmartFusion2 Advanced Development Kit.

Table 4 • **SmartFusion2 Advanced Kit Jumper Settings**

Jumper	Pin (from)	Pin (to)	Comments
J116, J353, J354, J54	1	2	These are the default jumper settings of the Advanced Development Kit board. Ensure these jumpers are set accordingly.
J123	2	3	
J124, J121, J32	1	2	JTAG programming via FTDI

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List of Changes

The following table shows important changes made in this document for each revision.

Date	Changes	Page
Revision 2 (November 2015)	Updated the document for Libero v11.6 software release (SAR 72436).	NA
Revision 1 (May 2015)	Initial release for Libero SoC v11.5 software release.	NA
Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*		

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