SmartFusion2 and IGLOO2 PCIe Data Plane Demo using 2 Channel Fabric DMA - Libero SoC v11.6

DG0517 Demo Guide

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Microsemi

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Confidentiality Status

This is a non-confidential document.

Table of Contents

Preface . . . 4
About this document . . . 4
Intended Audience . . . 4
References . . . 4
Microsemi Publications . . . 4

SmartFusion2 and IGLOO2 PCIe Data Plane Demo using 2 Channel Fabric DMA . . . 5
Introduction . . . 5
Demo Design . . . 6
Introduction . . . 6
Demo Design Features . . . 8
Demo Design Description . . . 9
Throughput Calculation . . . 11
Setting Up the Demo Design . . . 11
Jumper Settings for SmartFusion2 Advanced Development Kit . . . 11
Jumper Settings for IGLOO2 Evaluation Kit . . . 12
Programming the Device . . . 13
Connecting the Kit to the Host PC PCIe Slot . . . 15
Drivers Installation . . . 20
PCIe_Demo Application . . . 22
Running the Design . . . 25
Summary . . . 42

Appendix 1: IGLOO2 Evaluation Kit Board Setup for Laptop . . . 43

Appendix 2: Register Details . . . 46

A List of Changes . . . 47

B Product Support . . . 48
Customer Service . . . 48
Customer Technical Support Center . . . 48
Technical Support . . . 48
Website . . . 48
Contacting the Customer Technical Support Center . . . 48
Email . . . 48
My Cases . . . 49
Outside the U.S. . . . 49
ITAR Technical Support . . . 49

Preface

About this document

This demo is for SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO®2 FPGA devices. It provides instructions on how to use the corresponding reference design.

Intended Audience

SmartFusion2 and IGLOO2 devices are used by:

- FPGA designers
- Embedded designers
- System-level designers

References

Microsemi Publications

UG0331: SmartFusion2 Microcontroller Subsystem User Guide

UG0447: SmartFusion2 and IGLOO2 FPGA High Speed Serial Interfaces User Guide

UG0456: SmartFusion2 SoC FPGA PCIe Control Plane Demo User Guide

TU0509: IGOO2 FPGA PCIe Control Plane Design Libero SoC Flow Tutorial

Refer to the following web page for a complete and up-to-date listing of SmartFusion2 device documentation: *http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2*

Refer to the following web page for a complete and up-to-date listing of IGLOO2 device documentation: *http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga*

SmartFusion2 and IGLOO2 PCIe Data Plane Demo using 2 Channel Fabric DMA

Introduction

This demo highlights the high-speed data transfer, the capability of SmartFusion2 and IGLOO2 devices through the PCIe interface. To achieve the high-speed data transfers, an advanced extensible interface (AXI) based direct memory access (DMA) controller is implemented in the FPGA Fabric. An application, **PCIe_Demo** that runs in the Host PC is provided for setting up and initiating DMA transactions from the SmartFusion2 or IGLOO2 PCIe endpoint to the Host PC device. Drivers for connecting the Host PC to the SmartFusion2 or IGLOO2 PCIe endpoint are provided as part of the demo deliverables.

Microsemi® provides three different PCIe data plane demos for SmartFusion2 devices:

- *DG0501: SmartFusion2 PCIe MSS HPDMA Demo Guide*: This demo shows the low throughput data transfers between PCIe and double data rate (DDR).
- *DG0535: SmartFusion2 PCIe Data Plane Demo using MSS HPDMA and SMC_FIC Demo Guide*: This demo shows the medium throughput data transfers between PCIe and embedded static random access memory (eSRAM).
- DG0517: SmartFusion2 and IGLOO2 PCIe Data Plane Demo using 2 Channel Fabric DMA Demo Guide (current demo): This demo shows the high throughput data transfers between PCIe and large SRAM (LSRAM).

The high-speed serial interface (SERDESIF) available in the SmartFusion2 or IGLOO2 devices provides a fully hardened PCIe endpoint implementation and is compliant to the PCIe Base Specification Revision 2.0 and 1.1. For more information, refer to the *UG0447: SmartFusion2 and IGLOO2 FPGA High Speed Serial Interfaces User Guide*.

This demo demonstrates the performance of the PCIe and DDR controller of the SmartFusion2 and IGLOO2 device families. For a tutorial design on how to develop and use the PCIe endpoint including the tools flow and simulation, see the *UG0456: SmartFusion2 SoC FPGA PCIe Control Plane Demo User Guide*.

Table 1 • Design Requirements

Design Requirements	Description
Hardware Requirements	
SmartFusion2 Advanced Development Kit: • 12 V adapter • PCI Edge Card Ribbon Cable	Rev B or later
IGLOO2 Evaluation Kit: • FlashPro4 programmer • 12 V adapter • USB A to Mini-B cable	Rev C or later
Host PC (or Laptop) with 8GB RAM and PCIe 2.0 Gen1 or Gen2 compliant slot.	Any 64-bit Windows Operating System
Software Requirements	
Libero® System-on-Chip (SoC)	v11.6
FlashPro programming software	v11.6
PCIe_Demo Application	–

Notes: 1. For SmartFusion2 Kit, PCIe with x4 or higher is required. For IGLOO2 Kit, PCIe with x1 or higher is required.
2. PCI Express card slot and PCIe Express card adapter (for Laptop only).
3. PCIe Express card adapter is not supplied with the IGLOO2 Evaluation Kit.

Demo Design

Introduction

The demo design files are available for download from the following path in the Microsemi website: *http://soc.microsemi.com/download/rsc/?f=m2s_m2gl_dg0517_pcie_fabric_dma_liberov11p6_df*

The demo design files include:

- Drivers_64bitOS
- GUI
- Libero Project
- Programming files
- Readme.txt file

Figure 1 shows the top-level structure of the design files. For further details, see the `readme.txt` file.

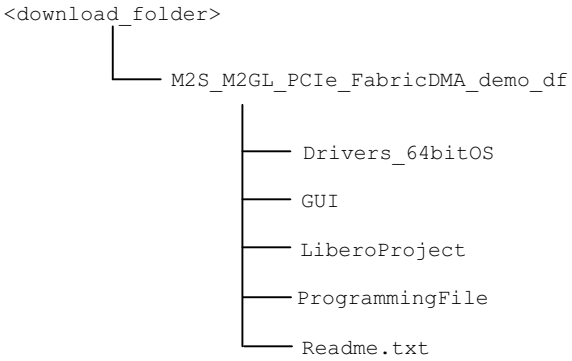

Figure 1 • **Demo Design Files Top Level Structure**

Figure 2 on page 8 describes the demo design. The PCIe core in the SmartFusion2 or IGLOO2 devices supports both AXI and AMBA high-performance bus (AHB) Master and Slave interfaces. This demo design uses the AXI Master and Slave interfaces to achieve maximum bandwidth. The PCIe_Demo application on the Host PC initiates the DMA transfers and the embedded PCIe core in the SmartFusion2 or IGLOO2 device initiates the AXI transactions through the AXI master interface to the DMA controller in the FPGA Fabric. The DMA controller has two independent channels that share the AXI read/write channels of the PCIe AXI slave interface and the MDDR AXI slave interface. The DMA controller in the FPGA Fabric initiates the DMA channels depending on the type of the DMA transfer. Each channel has a timer for calculating the throughput and has 4 KB of LSRAM buffer.

DMA channel 0 handles the following DMA transfers:

- Host PC memory to LSRAM
- Host PC memory to DDR memory
- LSRAM to DDR memory

DMA channel 1 handles the following DMA transfers:

- LSRAM to Host PC memory
- DDR memory to Host PC memory
- DDR memory to LSRAM

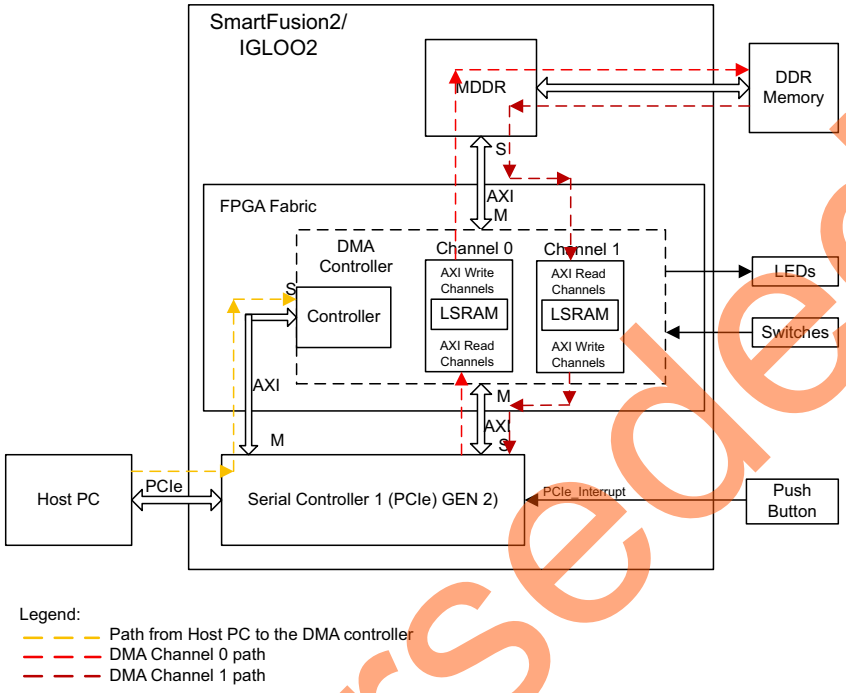

Figure 2 • **PCIe Data Plane Demo Block Diagram**

For SmartFusion2 Advanced Development Kit, MDDR is configured for accessing DDR3 memory in x32 mode. The MDDR clock is configured to 332 MHz (664 Mbps DDR) with a 166 MHz DDR_FIC clock for an aggregate memory bandwidth of nearly 2656 MBps. The PCIe AXI interface clock, ARM® Cortex®-M3 clock, PCIe AXI interface clock, and Fabric DMA controller clocks are configured to 166 MHz.

For IGLOO2 Evaluation Kit, MDDR is configured for accessing LPDDR memory in x16 mode. The MDDR clock is configured to 166 MHz (332 Mbps DDR) with a 166 MHz DDR_FIC clock for an aggregate memory bandwidth of nearly 664 MBps. The PCIe AXI interface clock and Fabric DMA controller clocks are configured to 166 MHz.

Demo Design Features

- DMA data transfers between the Host PC memory and the LSRAM
- DMA data transfers between the Host PC memory and the DDR memory
- DMA data transfers between the DDR memory and the LSRAM
- Throughput for every DMA data transfer
- Enables continuous DMA transfers for observing throughput variations.
- Displays the PCIe link enable/disable, negotiated link width, and the link speed on the PCIe_Demo application.
- Displays the position of DIP Switches on the SmartFusion2 Advanced Development Kit or IGLOO2 Evaluation Kit on the PCIe_Demo application.
- Displays the PCIe Configuration Space on the PCIe_Demo application.

- Controls LEDs on the board according to the command from the PCIe_Demo application.
- Enables read and write operations to scratchpad register in the FPGA Fabric.
- Interrupts the Host PC, when the Push button is pressed. The PCIe_Demo application displays the count value of the number of interrupts sent from the board.

Demo Design Description

There are six different types of data transfers supported by this demo design. The following sections describe the process of each data transfer:

- Host PC Memory to LSRAM (Read)
- LSRAM to Host PC Memory (Write)
- Host PC Memory to DDR Memory (Read)
- DDR Memory to Host PC Memory (Write)
- LSRAM to DDR Memory (Write)
- DDR Memory to LSRAM (Read)

Host PC Memory to LSRAM (Read)

Data transfer from PC memory to the LSRAM occurs in the following sequence:

1. PCIe_Demo application sets up the Fabric DMA controller through the PCIe link. This includes DMA direction, address, and size (4 KB).
2. Fabric DMA controller initiates a 16 beat AXI burst (that is, 128 bytes) read transaction to the PCIe AXI slave interface.
3. The PCIe core sends the memory read (MRd) transaction layer packets (TLP) to the Host PC.
4. The Host PC returns a completion (CplD) TLP to the PCIe link.
5. This returned data completes the AXI read initiated by the Fabric DMA controller.
6. This data is stored in the LSRAM.
7. The Fabric DMA controller repeats this process until the 4 KB of data transfer is completed.
8. The Fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application.

LSRAM to Host PC Memory (Write)

Data transfer from the LSRAM to PC memory occurs in the following sequence:

1. PCIe_Demo application sets up the Fabric DMA controller through the PCIe link. This includes DMA direction, address and size (4 KB).
2. Fabric DMA controller reads the LSRAM data and initiates an AXI 16 beat burst write transaction to PCIe AXI slave interface.
3. The PCIe core sends a memory write (MWr) TLP to the Host PC.
4. The Fabric DMA controller repeats this process until the 4 KB size of data transfer is completed.
5. The Fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application.

Host PC Memory to DDR Memory (Read)

Data transfer from the PC memory to the DDR memory occurs in the following sequence:

1. PCIe_Demo application sets up the Fabric DMA controller through the PCIe link. This includes DMA direction, address and size (4 KB).
2. Fabric DMA controller initiates 16 beat AXI burst (that is, 128 bytes) read transaction to the PCIe AXI interface.
3. The PCIe core sends a memory read (MRd) transaction layer packets (TLP) to the Host PC.
4. The Host PC returns a completion data (CplD) TLP to the PCIe link.
5. This returned data completes the AXI read initiated by the Fabric DMA controller.
6. This data is stored in the dual port LSRAM.

7. The LSRAM data is written to the DDR controller through the AXI interface as an AXI 16 beat burst write transaction. The reads from the Host PC memory and the writes to the DDR memory occur independent of each other for achieving high throughput. Empty flags are generated in the Fabric DMA controller to avoid reading unknown data from the LSRAM.
8. The Fabric DMA controller repeats this process until 4 KB of data transfer is completed.
9. The Fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application.

DDR Memory to Host PC Memory (Write)

Data transfer from the DDR memory to the PC memory occurs in the following sequence:

1. PCIe_Demo application sets up the Fabric DMA controller through the PCIe link. This includes DMA direction, address and size (4 KB).
2. The Fabric DMA controller initiates a 16 beat burst (that is, 128 bytes) AXI read transaction from the DDR through the MDDR controller.
3. The data is stored in the dual port LSRAM.
4. The LSRAM data is written to the PCIe core as an AXI 16 beat burst write transaction. The reads from the DDR memory and writes to Host PC memory occur independent of each other for achieving high throughput. Empty flags are generated in the Fabric DMA controller to avoid reading unknown data from the LSRAM.
5. The PCIe core sends a memory write (MWr) TLP to the Host PC.
6. The Fabric DMA controller repeats this process until 4 KB of data transfer is completed.
7. The Fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application.

LSRAM to DDR Memory (Write)

Data transfer from the LSRAM to the DDR memory occurs in the following sequence:

1. PCIe_Demo application sets up the Fabric DMA controller through the PCIe link. This includes DMA direction, address and size (4 KB).
2. The LSRAM data is written to the DDR controller through AXI interface as an AXI 16 beat burst write transaction.
3. The Fabric DMA controller repeats this process until 4 KB of data transfer is completed.
4. The Fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application for display.

DDR Memory to LSRAM (Read)

Data transfer from the DDR memory to the LSRAM occurs in the following sequence:

1. PCIe_Demo application sets up the Fabric DMA controller through the PCIe link. This includes DMA direction, address and size (4 KB).
2. The Fabric DMA controller initiates a 16 beat burst AXI read transaction of the DDR through the MDDR controller.
3. The data is stored in the dual port LSRAM.
4. The Fabric DMA controller repeats this process until 4 KB of data transfer is completed.
5. The Fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application for display.

Throughput Calculation

This demo implements a timer to measure the throughput of DMA transfers. The throughput measured includes all of the overhead of the AXI, PCIe, and DMA controller transactions. The procedure for measuring throughput is:

1. Setup the DMA controller for the complete transfer.
2. Start a timer and the DMA controller.
3. Initiate data transfer for the requested number of bytes.
4. Wait till DMA transfer is completed.
5. Record the number of clock cycles consumed for steps 2-4.

To arrive at a realistic system performance, the throughput calculation takes into account all the overheads during a transfer. The Throughput formula is as shown below:

Throughput = Transfer Size (Bytes) / (Number of clock cycles taken for a transfer * Clock Period)

EQ 1

Setting Up the Demo Design

Jumper Settings for SmartFusion2 Advanced Development Kit

1. Connect the jumpers on the SmartFusion2 Advanced Development Kit, as shown in Table 2.

   CAUTION: While making the jumper connections, the power supply switch **SW7** must be switched off.

Table 2 • **SmartFusion2 FPGA Advanced Kit Jumper Settings**

Jumper	Pin (from)	Pin (to)	Comments
J116, J353, J354, J54	1	2	These are the default jumper settings of the Advanced Development Kit board. Make sure these jumpers are set accordingly.
J123	2	3	
J124, J121, J32	1	2	JTAG programming via FTDI

2. Connect the Host PC to the J33 Connector using the USB A to mini-B cable. The USB to UART bridge drivers are automatically detected. Verify, if the detection is made in the device manager as shown in Figure 3 on page 12.

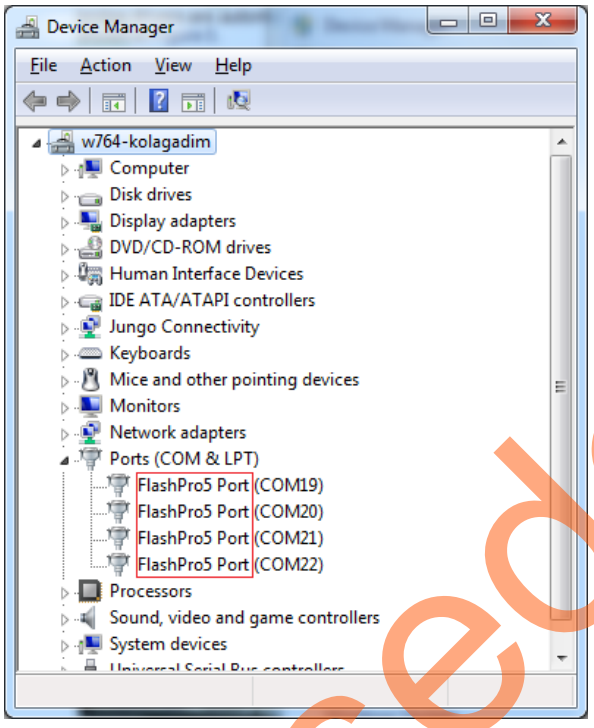

Figure 3 • **Device Manager**

3. Connect the power supply to the J18 connector. Switch on the power supply switch, **SW7**.

Jumper Settings for IGLOO2 Evaluation Kit

1. Connect the jumpers on the IGLOO2 Evaluation Kit as shown in Table 3.

   CAUTION: While making the jumper connections, the power supply switch **SW7** must be switched off.

Table 3 • **IGLOO2 FPGA Evaluation Kit Jumper Settings**

Jumper	Pin (from)	Pin (to)	Comments
J22	1	2	Default
J23	1	2	Default
J24	1	2	Default
J8	1	2	Default
J3	1	2	Default

2. Connect the FlashPro4 programmer to the J5 connector of the IGLOO2 Evaluation Kit.
3. Connect the power supply to the J6 connector. Switch on the power supply switch, **SW7**.

Programming the Device

Download the demo design from:
http://soc.microsemi.com/download/rsc/?f=m2s_m2gl_dg0517_pcie_fabric_dma_liberov11p6_df

1. Launch the FlashPro software.
2. Click **New Project**.
3. In the **New Project** window, type the project name.

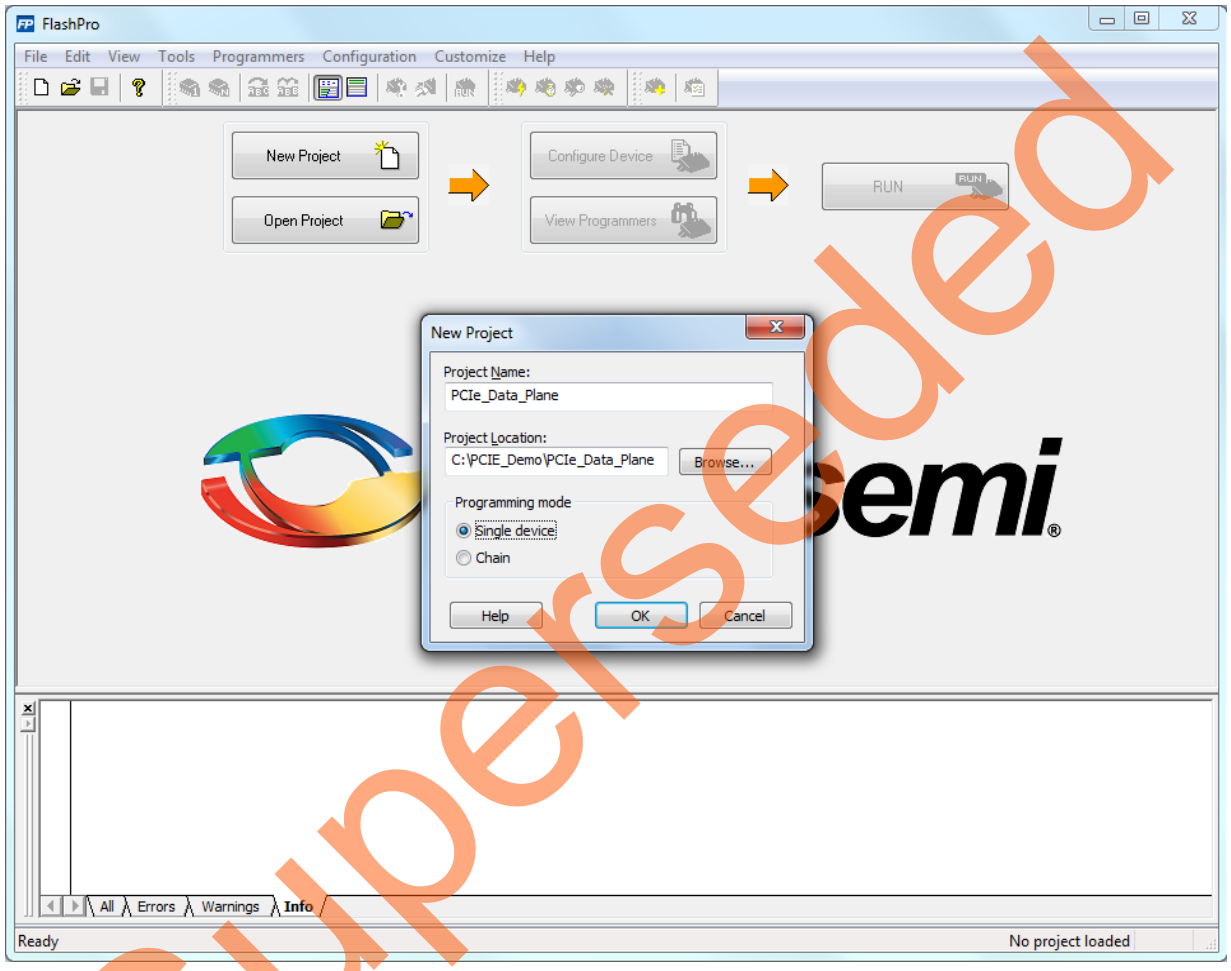

Figure 4 • **FlashPro New Project**

4. Click **Browse** and navigate to the location where you want to save the project.
5. Select **Single device** as the **Programming mode**.
6. Click **OK** to save the project.
7. Click **Configure Device**.
8. Click **Browse** and navigate to the location where the `PCIe_SB_top.stp` file is located and select the file. The default location is:

   SmartFusion2:
   <download_folder>\M2S_M2GL_PCIe_FabricDMA_demo_DF\ProgrammingFile\SF2

   IGLOO2: *<download_folder>\M2S_M2GL_PCIe_FabricDMA_demo_DF\ProgrammingFile\IGL2*

9. Click **Open**. The required programming file is selected and is ready to be programmed in the device.

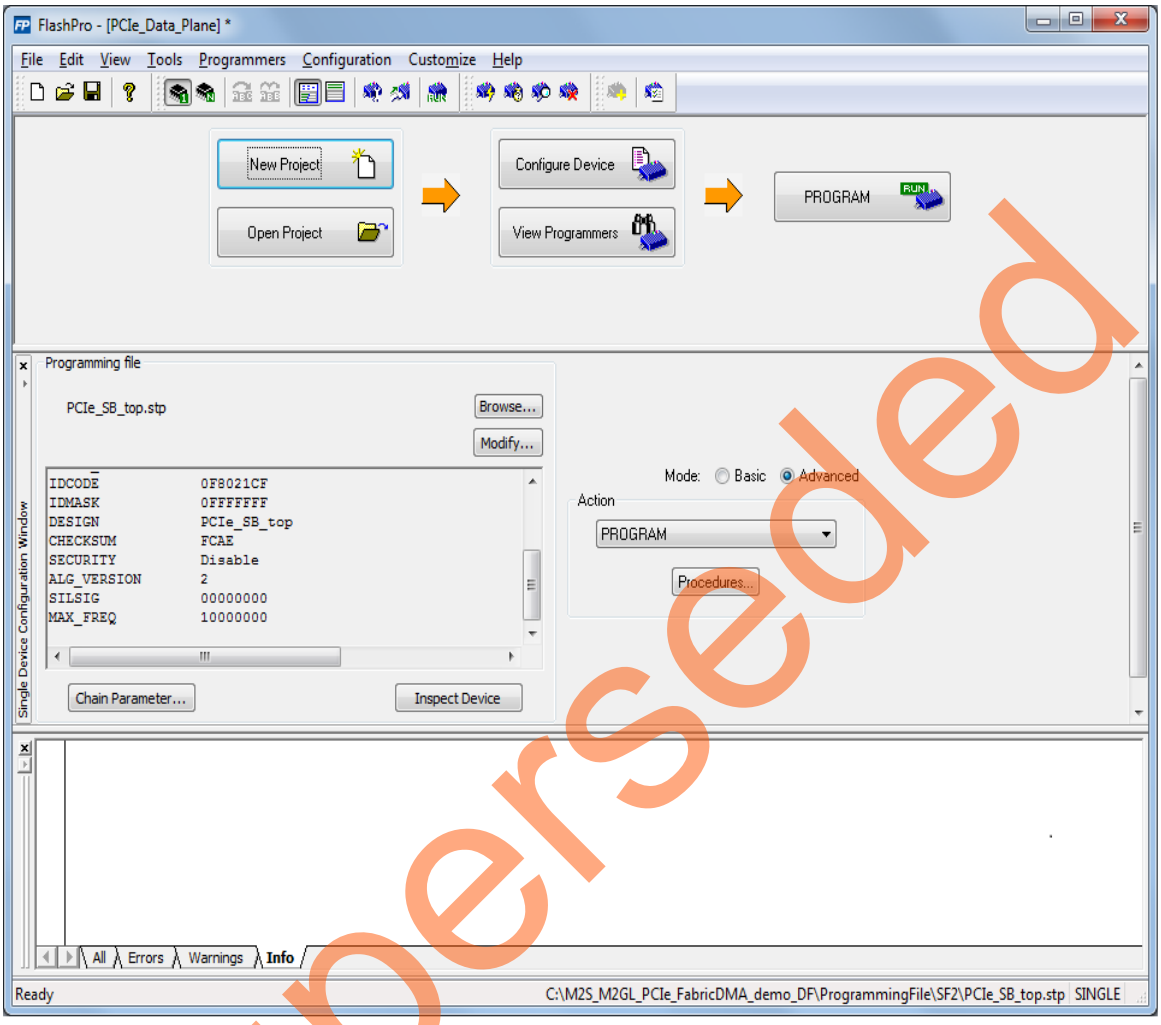

Figure 5 • **FlashPro Project Configured**

10. Click **PROGRAM** to start programming the device. Wait until you get a message indicating that the program passed.

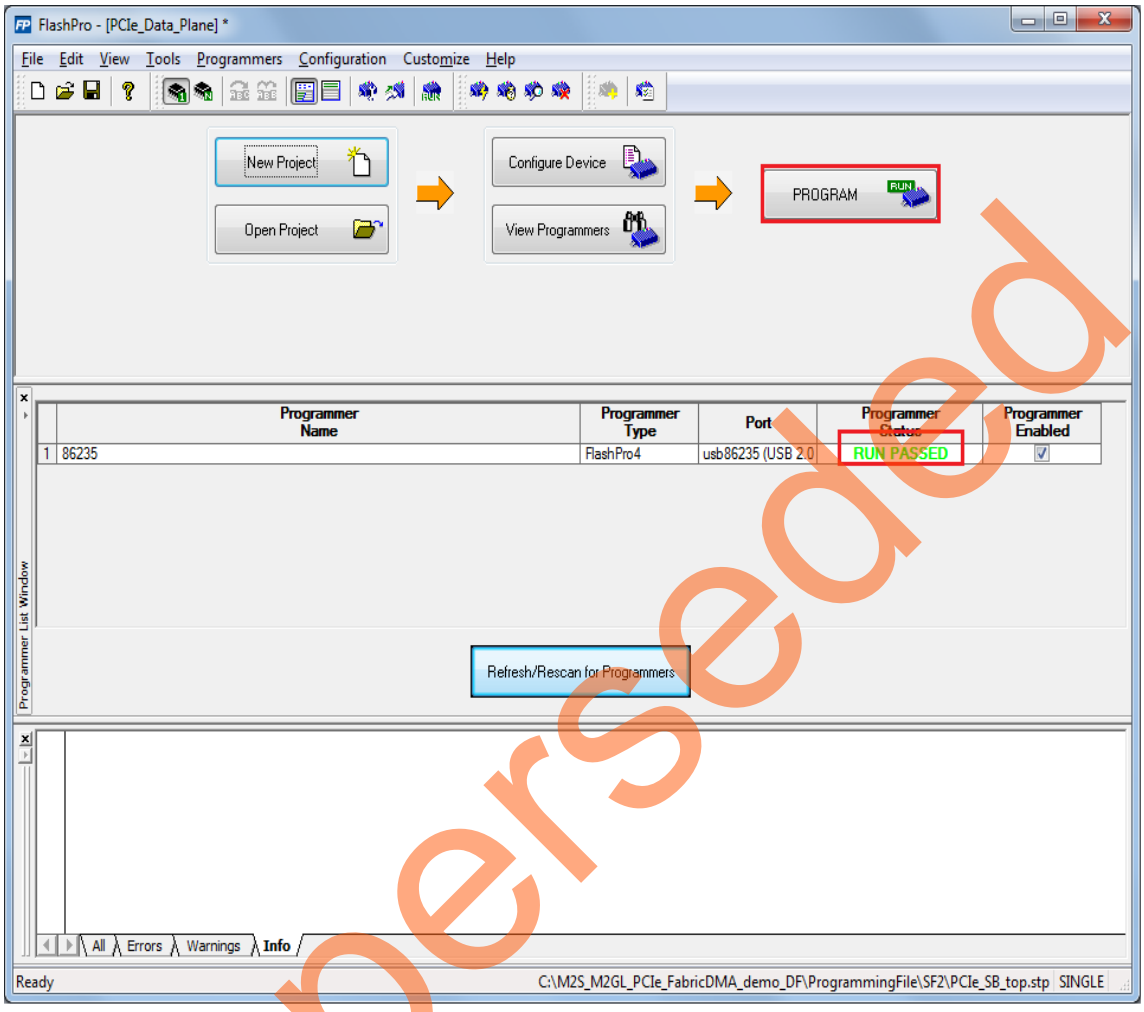

Figure 6 • **FlashPro Programming Passed**

Connecting the Kit to the Host PC PCIe Slot

1. After successful programming, **power off** the SmartFusion2 Advanced Development Kit or IGLOO2 Evaluation Kit and **shut down** the Host PC.
2. This Demo is designed to run in any PCIe Gen 2 compliant slot. If the host PC does not support Gen 2 compliant slot the demo will switch to Gen 1 mode. Connect the CON1 - PCIe Edge connector of SmartFusion2 Advanced Development Kit to Host PC's PCIe slot through the PCI Edge Card Ribbon Cable.

   OR,

   Connect the CON1 - PCIe Edge connector of IGLOO2 Evaluation Kit to the PCIe slot of the Host PC or connect the CON1-PCIe Edge connector to the Laptop PCIe slot using the Express card adapter. If using a laptop, Express card adapters typically support only Gen 1 and the demo will work in Gen 1 mode.

CAUTION: Host PC (or laptop) is required to be powered OFF while inserting the PCIe Edge Connector. If this step is not followed then please note that PCIe device detection and selection of Gen1 or Gen2 mode may not occur properly. This is very dependent on Host PC (or laptop) PCIe configuration. It is recommended that Host PC (or laptop) is powered off during PCIe card insertion.

3. Figure 7 shows the board setup for the Host PC in which SmartFusion2 Advanced Development Kit is connected to the Host PC PCIe slot.

Figure 7 • **SmartFusion2 Advanced Development Kit Setup for Host PC**

Figure 8 shows the board setup for the Host PC in which the IGLOO2 Evaluation Kit is connected to the Host PC PCIe slot. To connect the IGLOO2 Evaluation Kit to the Laptop using Express card adapter, refer to "Appendix 1: IGLOO2 Evaluation Kit Board Setup for Laptop" on page 43.

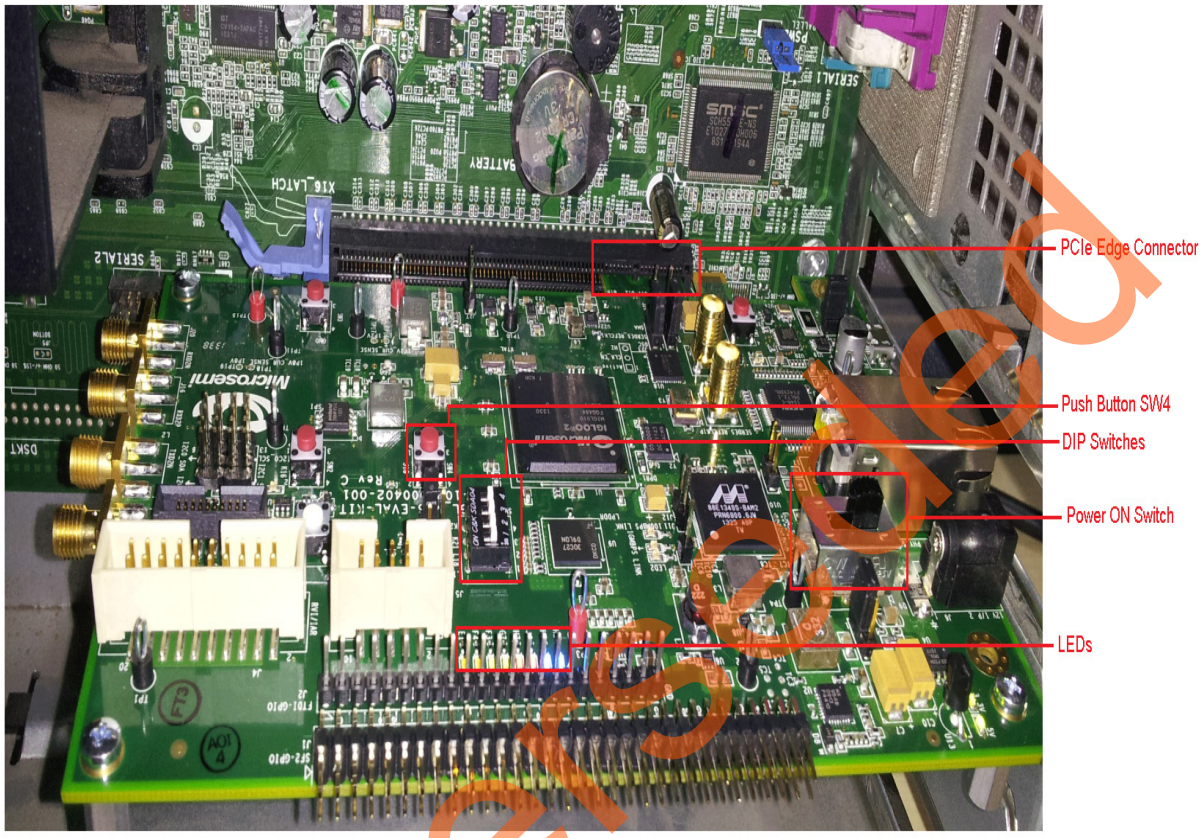

Figure 8 • **IGLOO2 Evaluation Kit Setup**

4. Switch ON the power supply switch, SW7.

5. Power on the Host PC and check the **Device Manager of the Host PC** for **PCIe Device**. Figure 9 shows the example **Device Manager** window. If the device is not detected, power cycle the SmartFusion2 Advanced Development Kit or IGLOO2 Evaluation Kit and click **scan for hardware changes** option in the **Device Manager**.

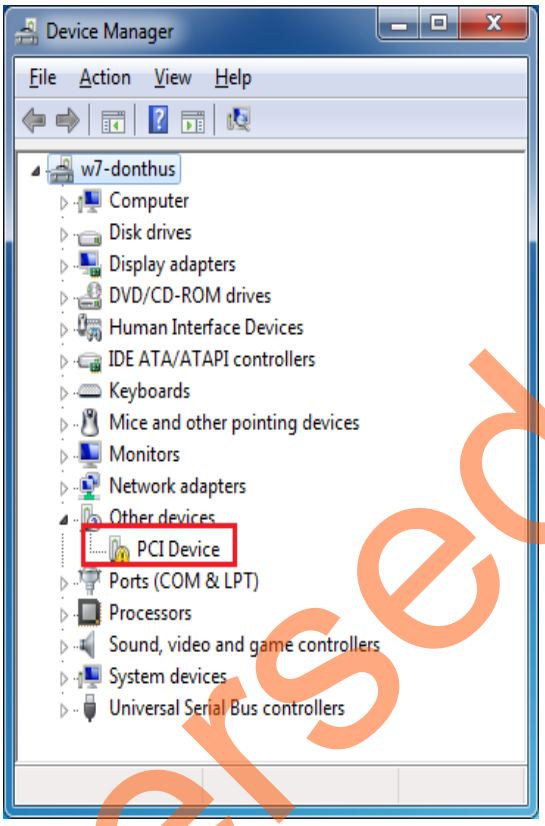

Figure 9 • **Device Manager - PCIe Device Detection**

Note: If the device is still not detected, check whether or not the BIOS version in the Host PC is latest, and if PCI is enabled in the Host PC BIOS.

6. If the Host PC has any other installed drivers (previous versions of Jungo drivers) for the PCIe device, uninstall them. To uninstall previous versions of Jungo drivers, follow steps a and b.

   a. To uninstall previous Jungo drivers, go to device manager and right-click on **DEVICE**. See, Figure 10.

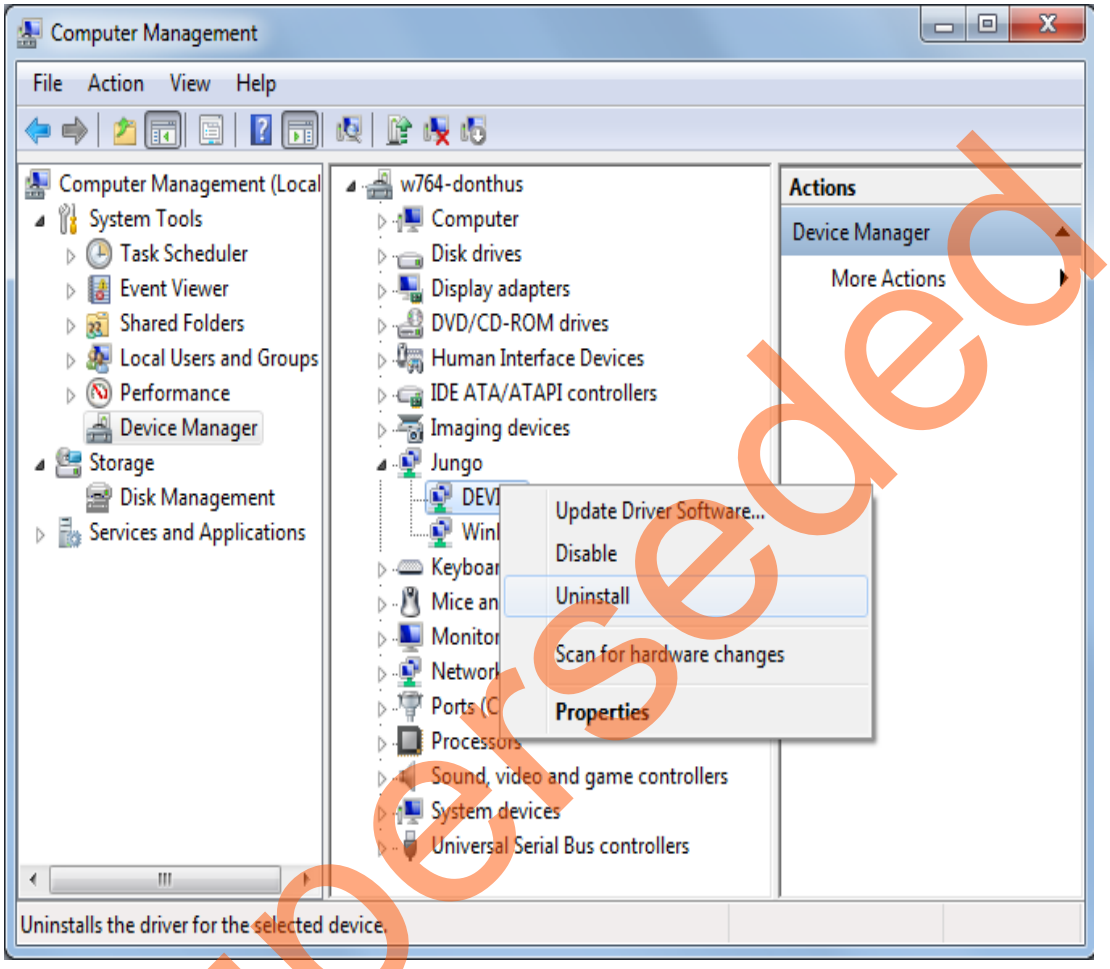

Figure 10 • **Uninstalling Jungo Driver**

b. From the **Confirm Device Uninstall** dialog, select **Delete the driver software for this device** and click **OK**. After uninstalling previous Jungo drivers, make sure that the PCI Device is detected in the **Device Manager** window. See Figure 11.

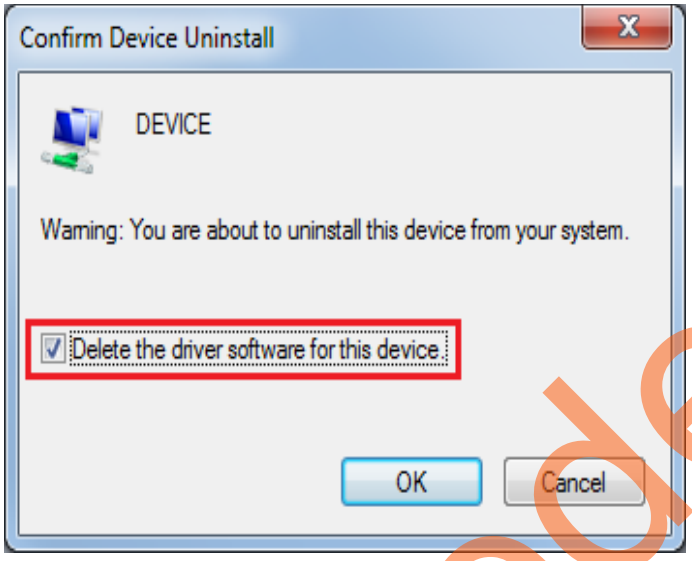

Figure 11 • **Confirm Device Uninstall Dialog**

Drivers Installation

The PCIe Demo uses a driver framework provided by Jungo WinDriverPro. The following steps describe how to install the PCIe drivers on Host PC:

1. Extract the `PCIe_Demo.rar` to C:\ drive. The `PCIe_Demo.rar` is located at:
   <Download Folder>\M2S_M2GL_PCIe_FabricDMA_demo_DF\Drivers_64bitOS\ PCIe_Demo.rar
2. Run the batch file `Jungo_KP_install.bat` located at *C:\ PCIe_Demo\DriverInstall*
   Note: Installing these drivers require administration rights.
3. If the **Windows Security** dialog appears asking to install or not, click **Install**.

Figure 12 • **Installing Jungo Driver**

Note: If the installation fails, invoke the **Command Prompt** in administrator mode and run the batch file `Jungo_KP_install.bat` located at *C:\PCIe_Demo\DriverInstall*

4. If the **Windows Security** dialog appears asking whether to install or not, click **Install this driver software anyway**.

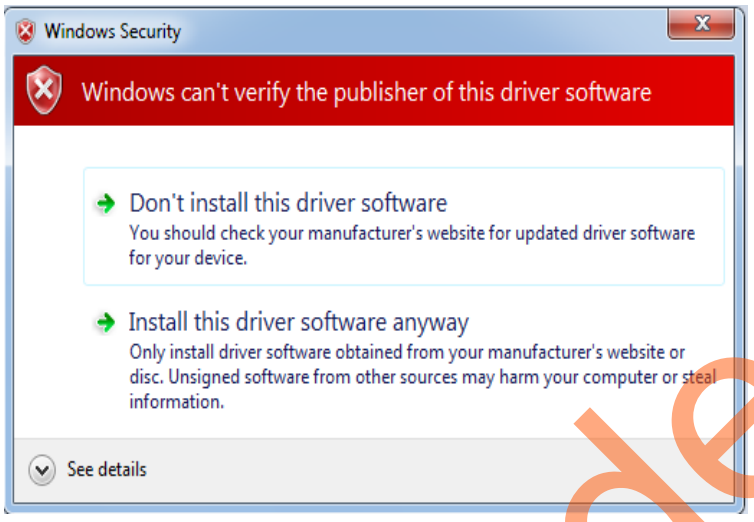

Figure 13 • **Windows Security Dialog**

PCIe_Demo Application

The PCIe_Demo application is a simple graphic user interface that runs on the Host PC to communicate with the SmartFusion2 or IGLOO2 PCIe endpoint device. It provides PCIe link status, driver information and demo controls. The PCIe_Demo application invokes the PCIe driver installed on the Host PC and provides commands to the driver according to the selection made. To install the PCIe_Demo application:

1. Download the PCIe demo GUI installer from *http://soc.microsemi.com/download/rsc/?f=PCIe_Demo_GUI_Installer*
2. Extract the **PCIe_Demo_GUI_Installer.rar**.
3. Double-click the **setup.exe** in the provided GUI installation (PCIe_Demo_GUI_Installer\setup.exe). Apply default options as shown in Figure 14.

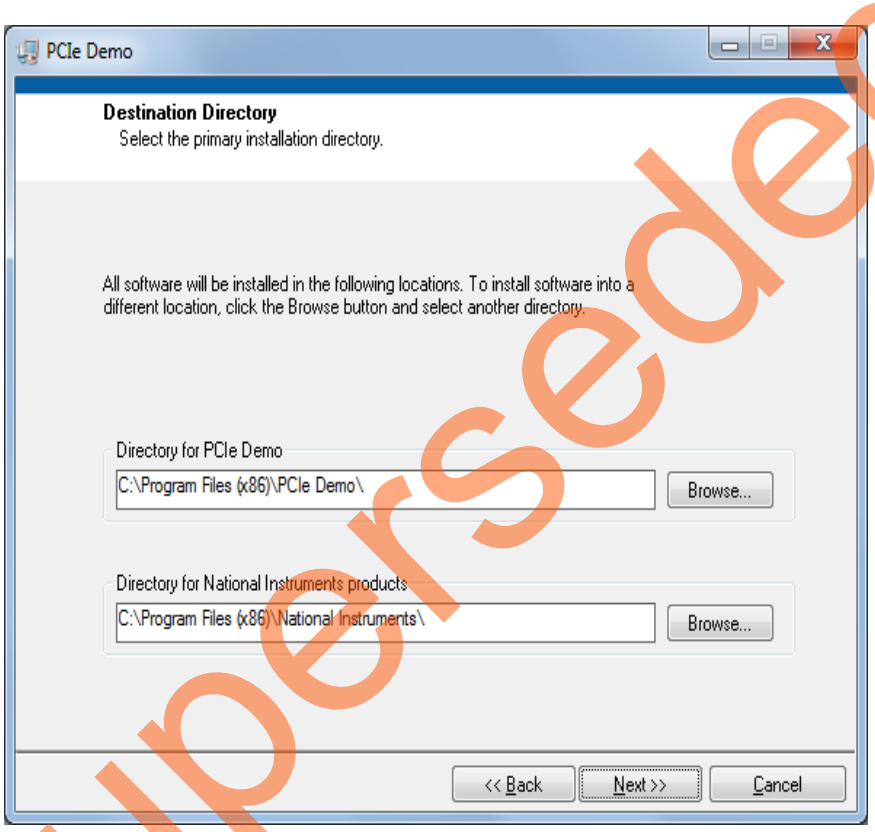

Figure 14 • **Installing PCIe_Demo Application**

4. To start the installation, click **Next**.

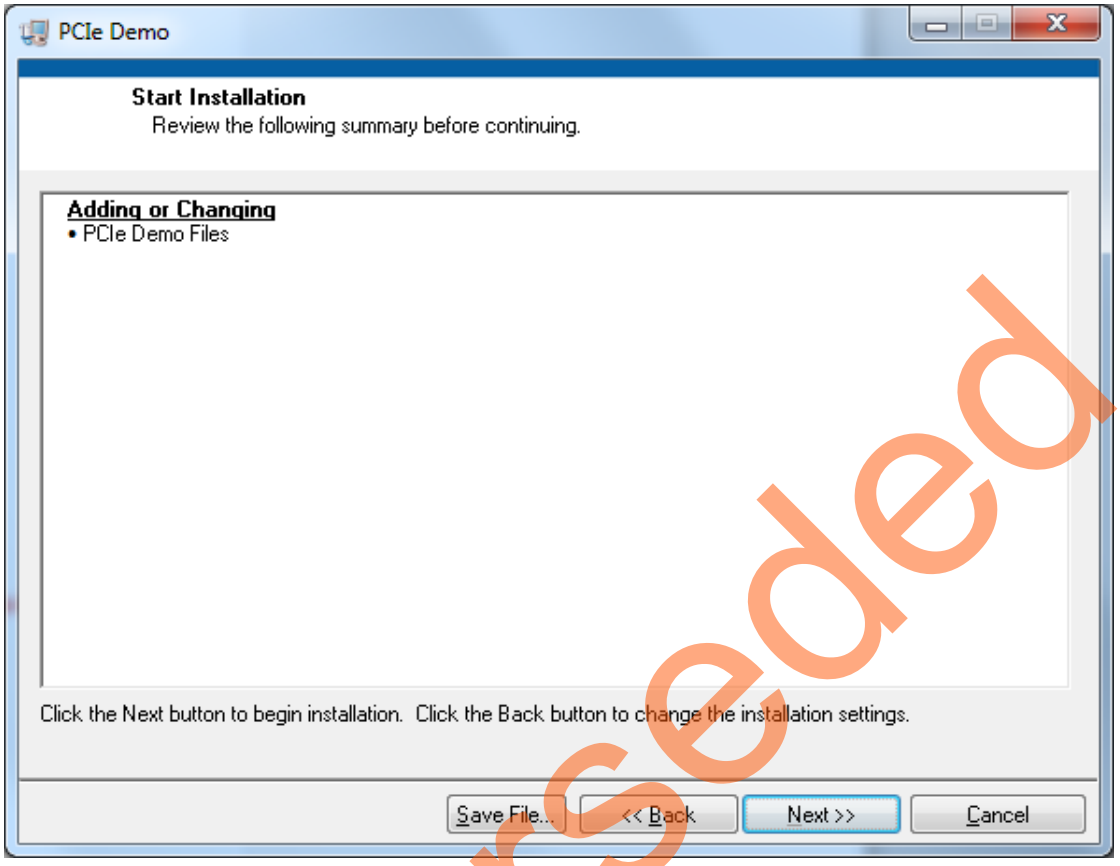

Figure 15 • **PCIe_Demo Application Installation Steps**

5. Click **Finish** to complete the installation.

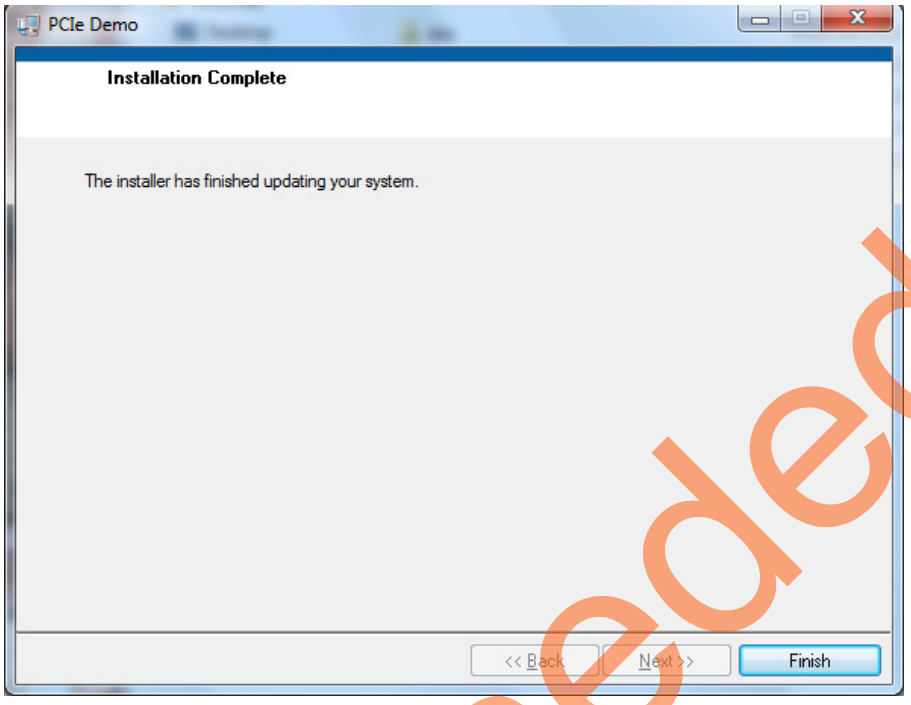

Figure 16 • **Successful Installation of PCIe_Demo Application**

6. Shut down the Host PC
7. Power Cycle the SmartFusion2 Advanced Development Kit.
8. Restart the Host PC.

Running the Design

1. Check the Host PC **Device Manager** for the drivers. Figure 17 shows an example Device Manager window highlighting the Jungo drivers installed. If the device is not detected, power cycle the SmartFusion2 Advanced Development Kit or IGLOO2 Evaluation Kit and click **scan for hardware changes** in **Device Manager**.

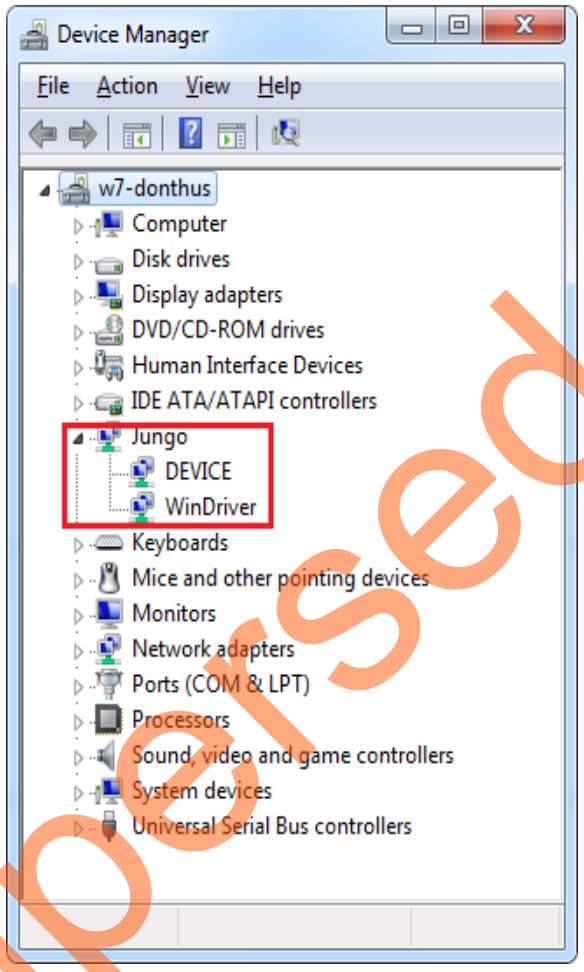

Figure 17 • **Device Manager - PCIe Device Detection**

Note: If a warning appears on the DEVICE or WinDriver in the Device Manager, uninstall them and start from step1 of driver installation.

2. Invoke the PCIe_Demo application from **ALL Programs > PCIe Demo > PCIe Demo GUI**. Figure 18 shows the PCIe_Demo launch window.

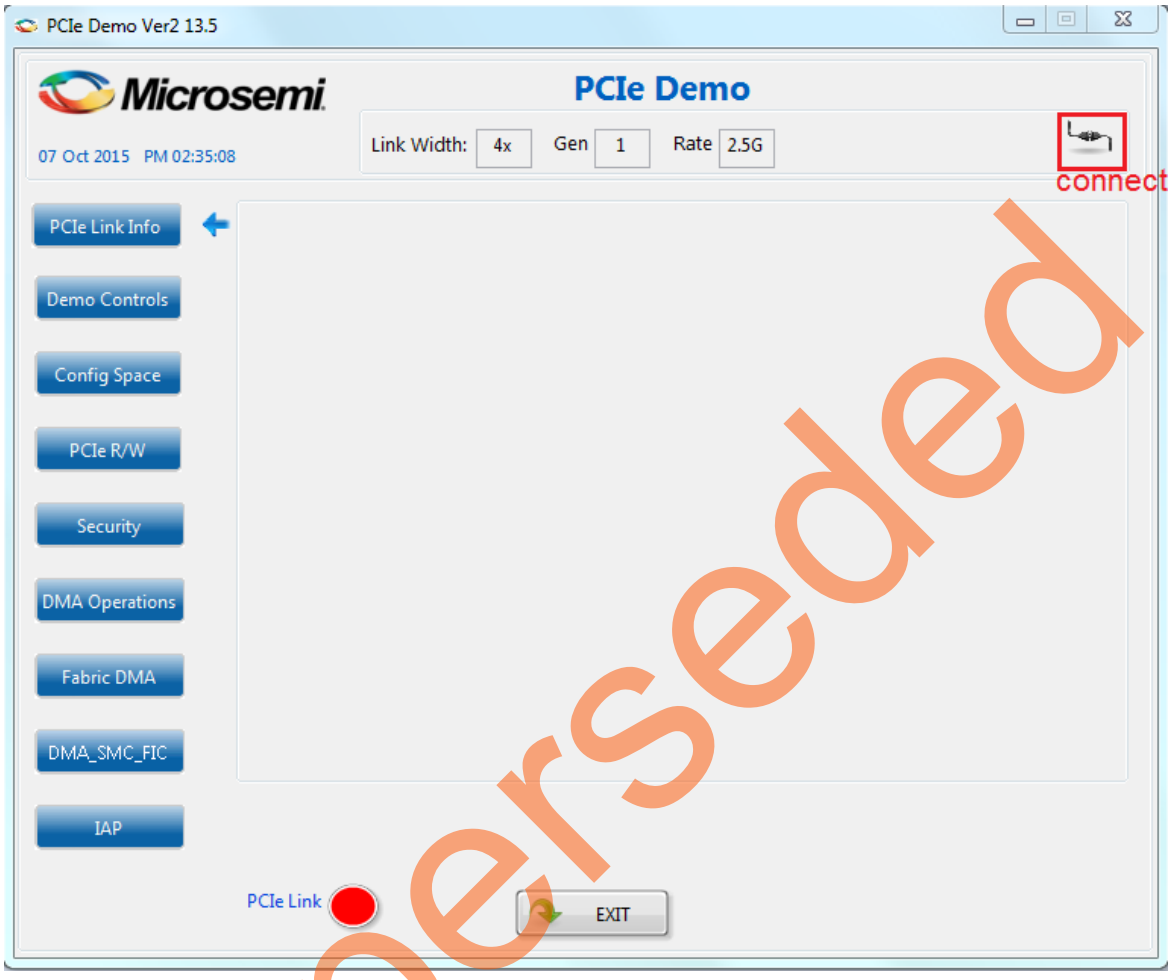

Figure 18 • **PCIe_Demo Application**

3. Click the **Connect** icon at top right corner of the PCIe_Demo application. The application detects and displays the connected Kit, demo design, and PCIe link. Figure 19 shows the example messages after the connection is established.

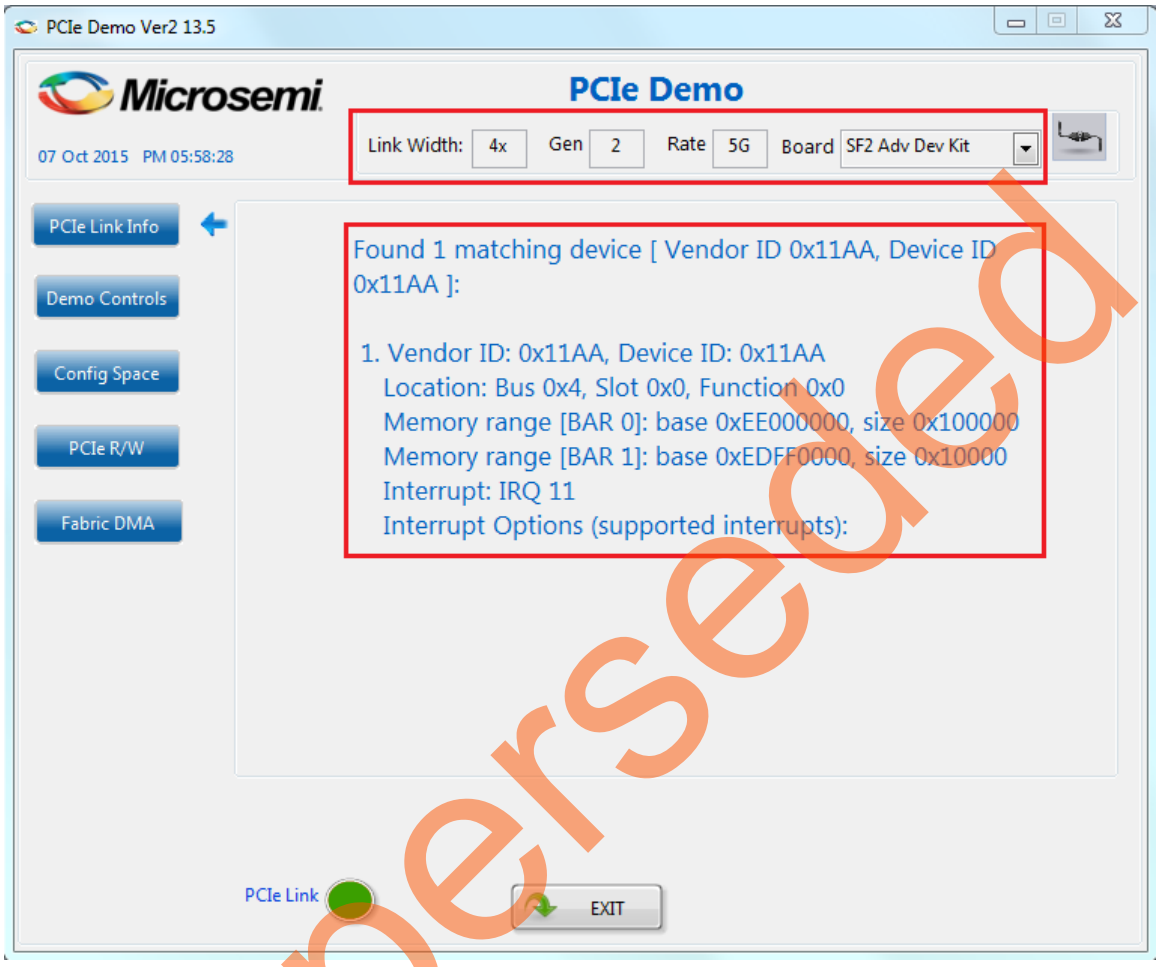

Figure 19 • **PCIe Device Information**

4. Click **Demo Controls** to display the LEDs options and DIP switch positions as shown in Figure 20.

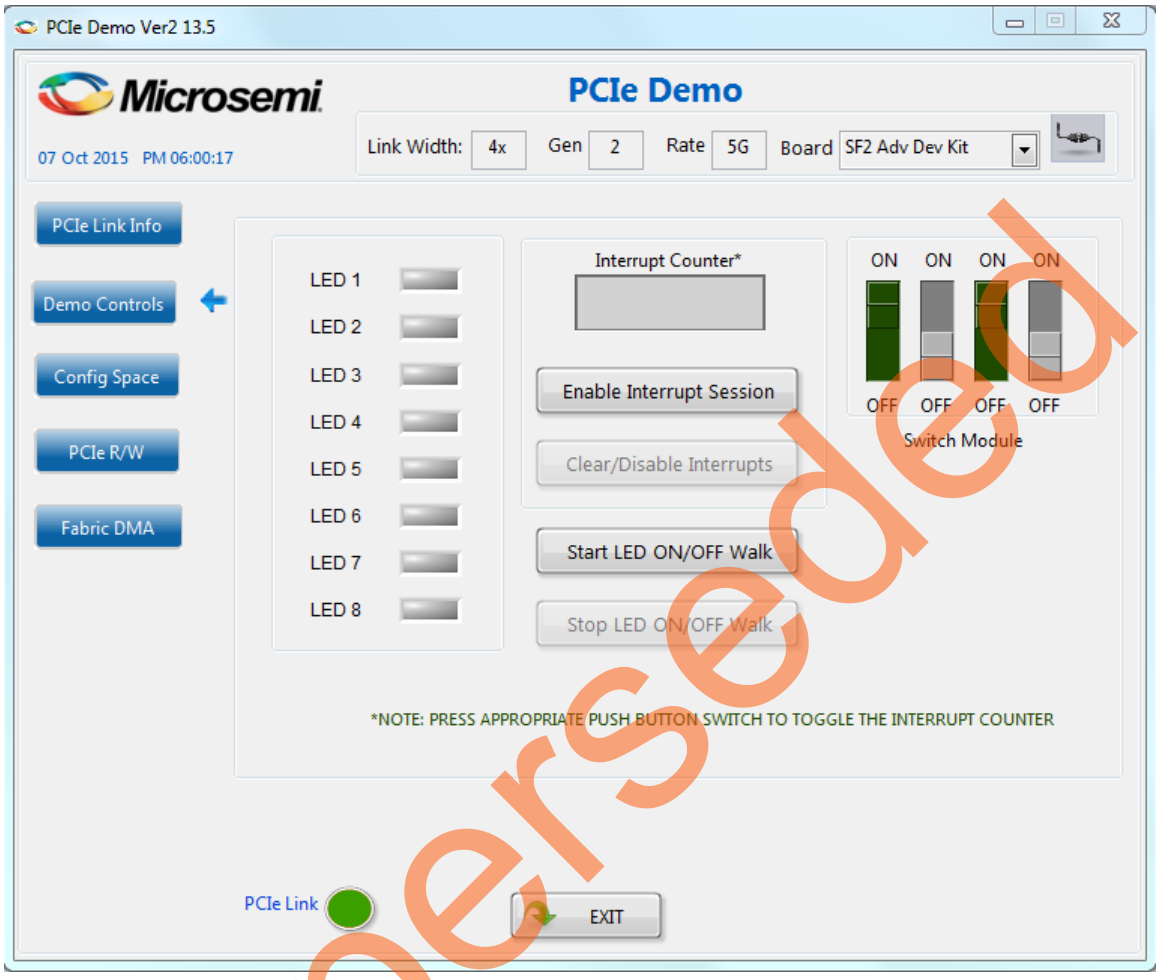

Figure 20 • **Demo Controls**

5. Click LED buttons to switch ON or OFF the LEDs on the board.
6. Click **Start LED ON/OFF Walk** to blink the LEDs on the board.
7. Click **Stop LED ON/OFF Walk** to stop the LEDs blinking.
8. Change the DIP switch positions on the board and observe the same reflected in the switches of the **Switch Module** of the PCIe_Demo application.
9. Click **Enable Interrupt Session** to enable the PCIe interrupt.

10. Press the push button, SW3 on the SmartFusion2 Advanced Development Kit board or SW4 on the IGLOO2 Evaluation Kit board. Observe the interrupt count on the **Interrupt Counter** field in PCIe_Demo application as shown in Figure 21.

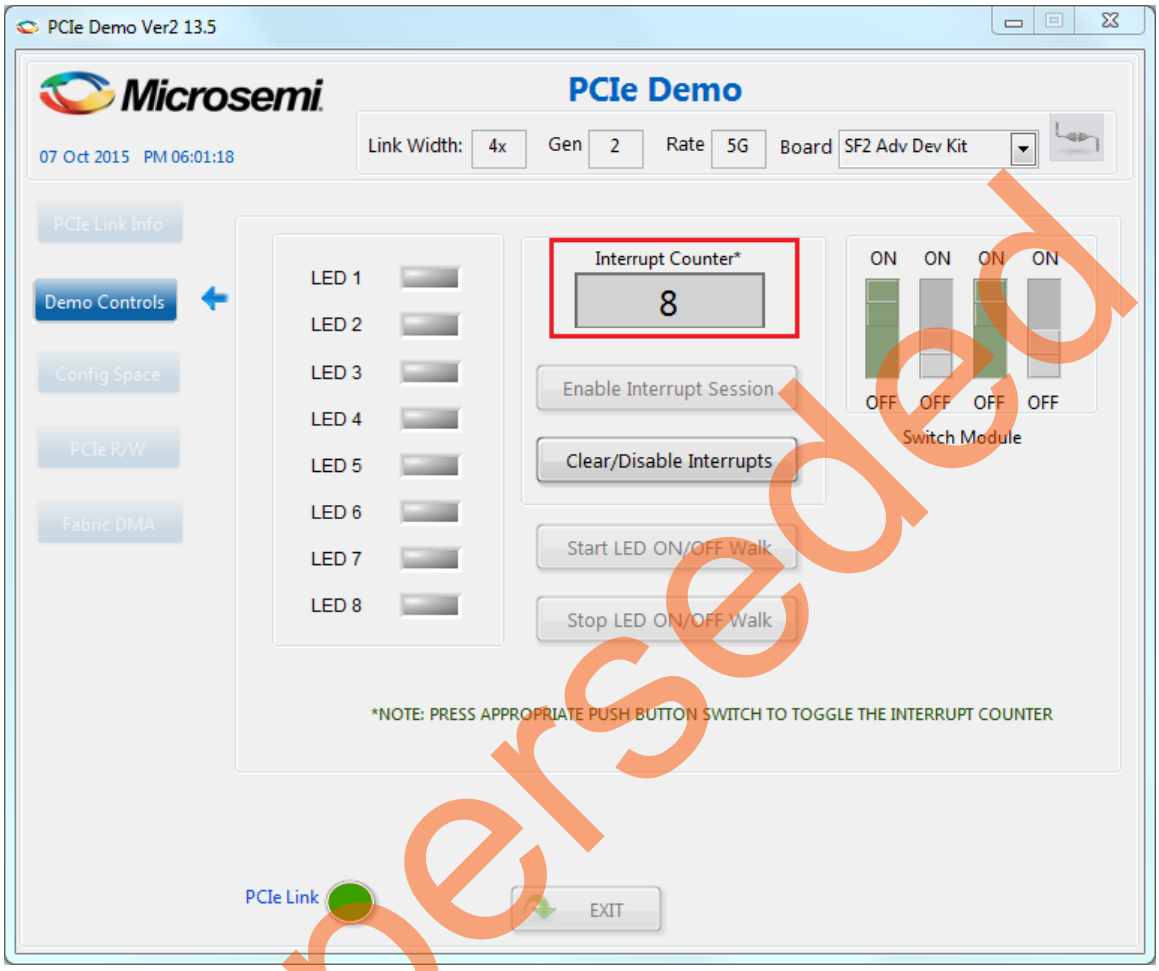

Figure 21 • **PCIe Interrupt**

11. Click **Clear/Disable Interrupts** to clear and disable the PCIe interrupts.

12. Click **Config Space** to see details about the PCIe configuration space. Figure 22 shows the PCIe configuration space.

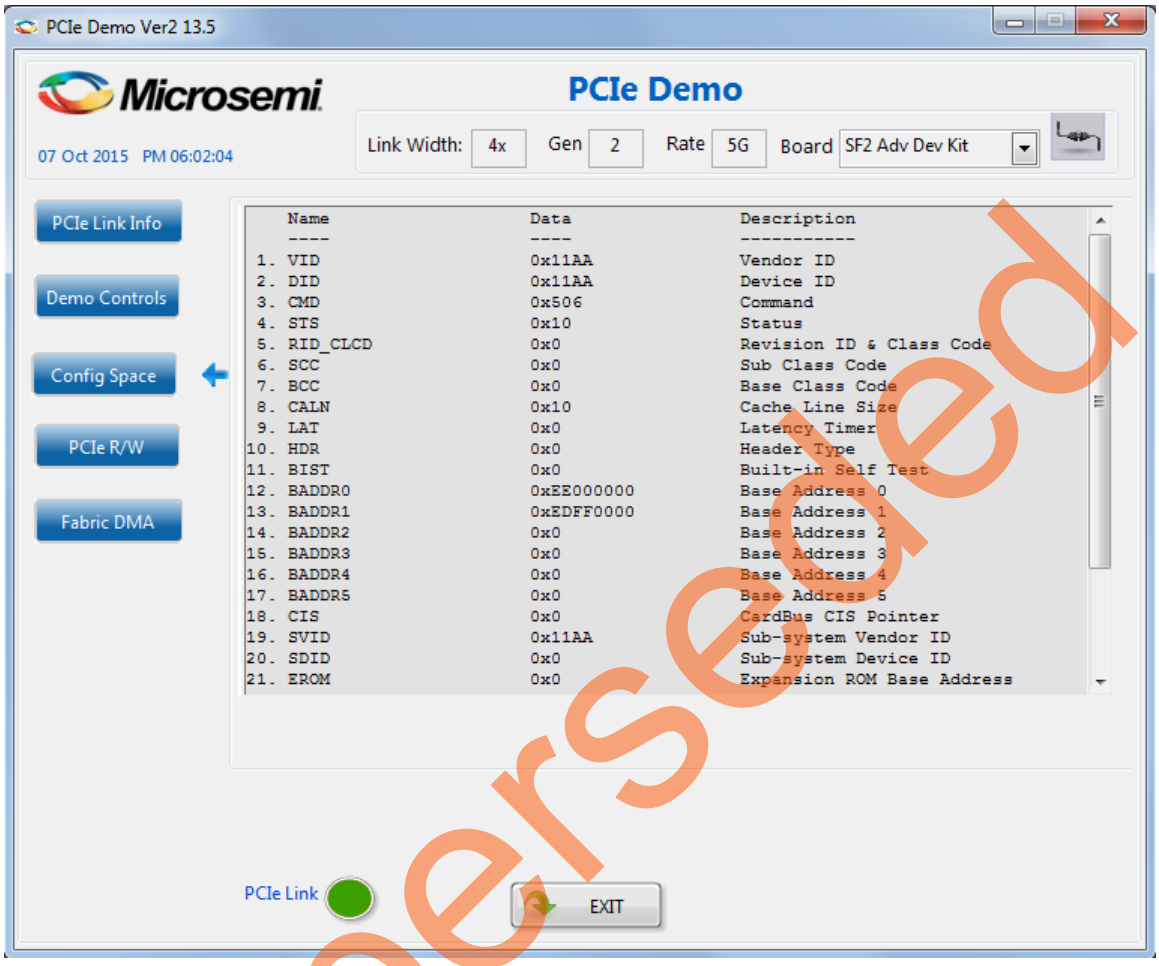

Figure 22 • **PCIe Configuration Space**

13. Click **PCIe R/W** to execute read and writes to a 32-bit scratchpad register through BAR1 space. Figure 23 shows the PCIe R/W panel.

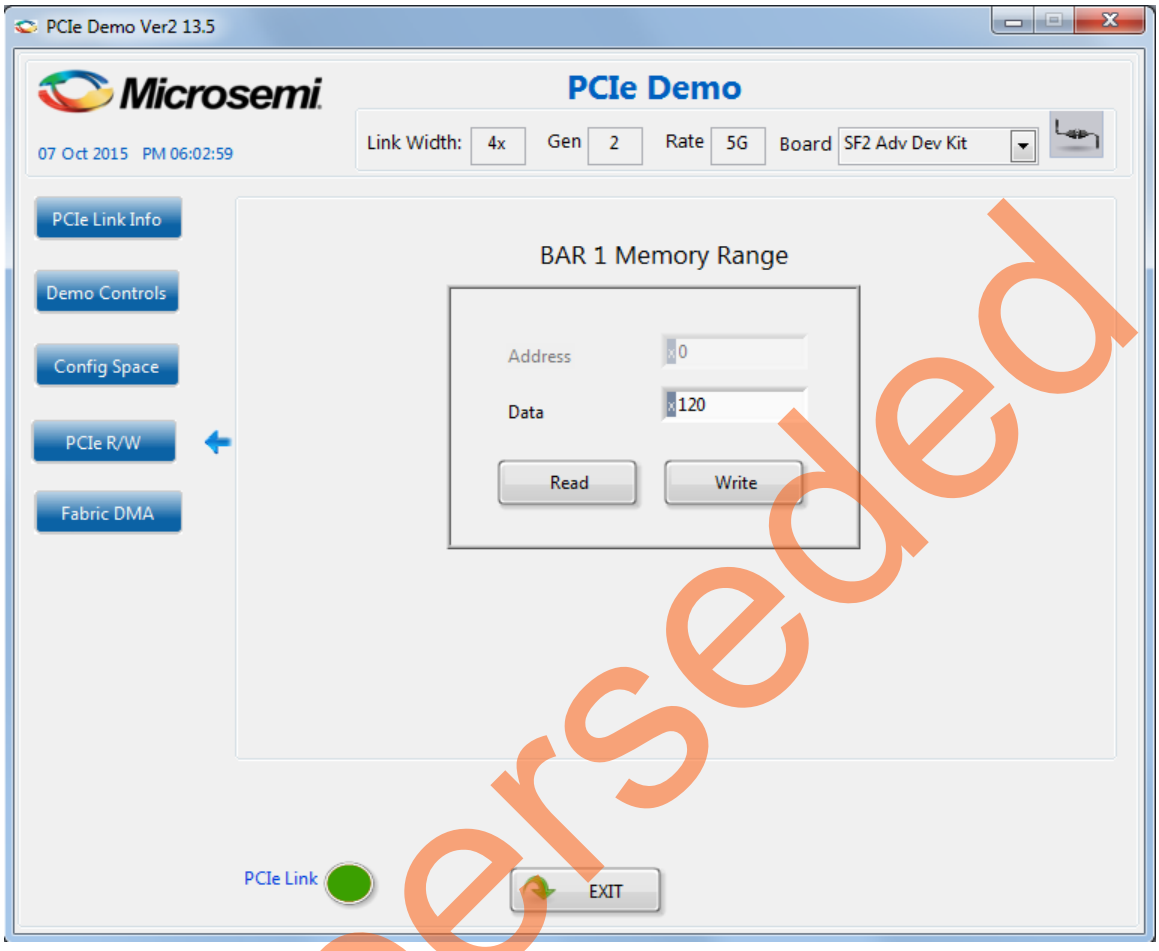

Figure 23 • **Read and Writes to Scratchpad Register**

14. Click **Fabric DMA** to execute the DMA operations. Three types of DMA transactions are possible:
    - Between Host PC memory and LSRAM
    - Between Host PC memory and DDR3 memory
    - Between LSRAM and DDR3 memory

    For each operation, **Transfer Type** can be selected as **Read**, **Write**, or **Read/Write** as shown in Figure 24. It also has a **Loop Count** field to execute the DAM operation in loop.

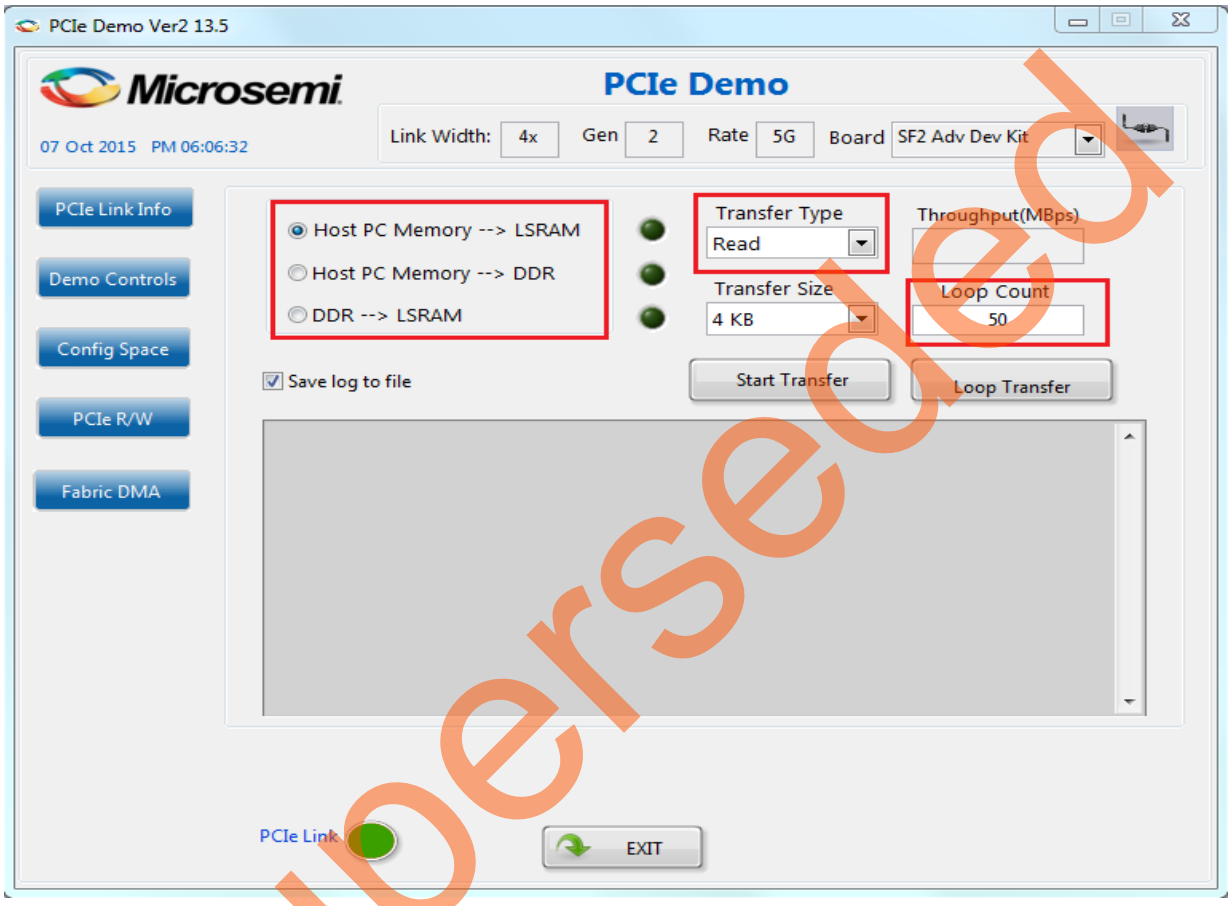

Figure 24 • **Fabric DMA Controls**

15. Select **Transfer Type** as **Read** and then select **Host PC Memory - - > LSRAM** to execute DMA transactions from Host PC to LSRAM. Click **Start Transfer**. Figure 25 shows the Fabric DMA panel.

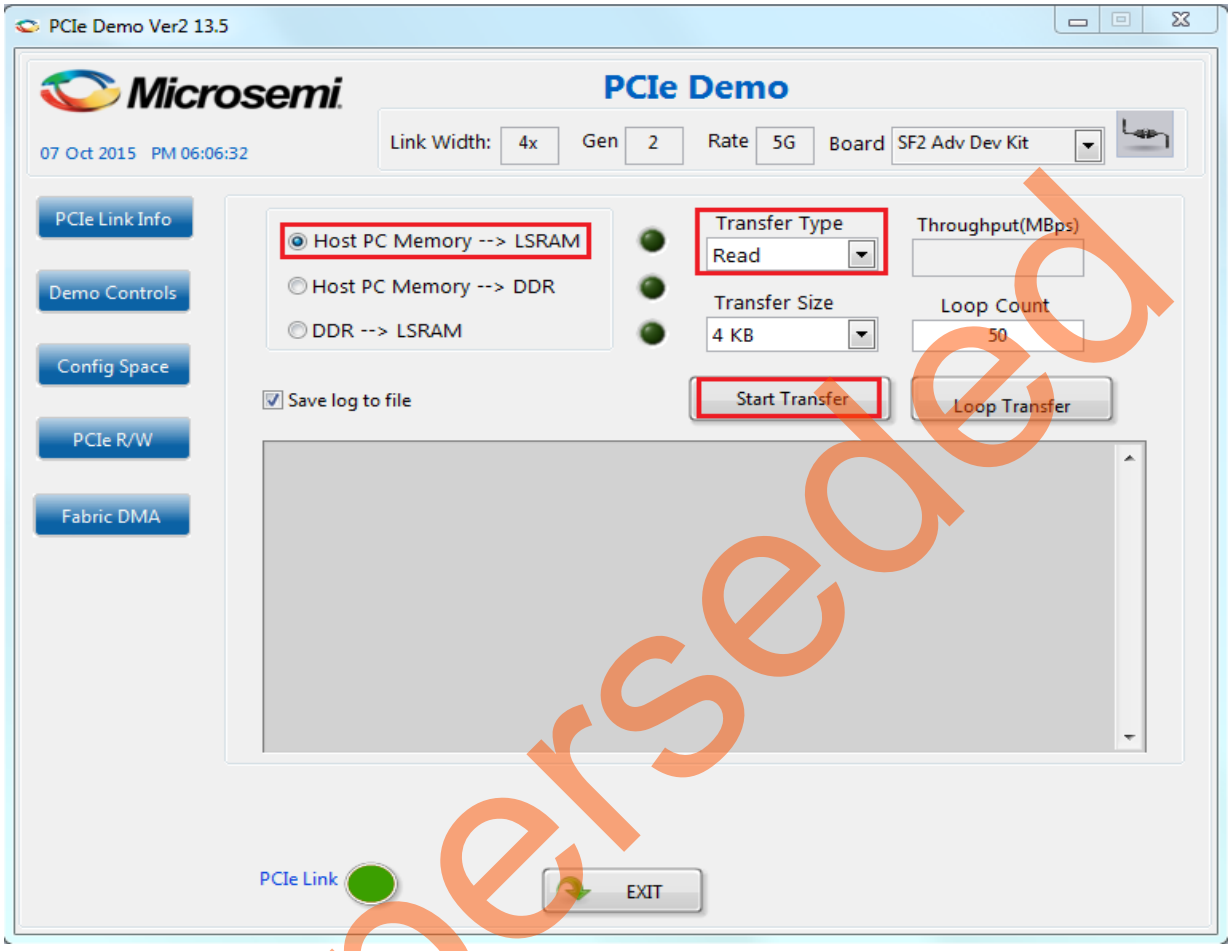

Figure 25 • **DMA Transactions between Host PC Memory and LSRAM**

16. After completion of data transfer, the throughput is displayed as shown in Figure 26.

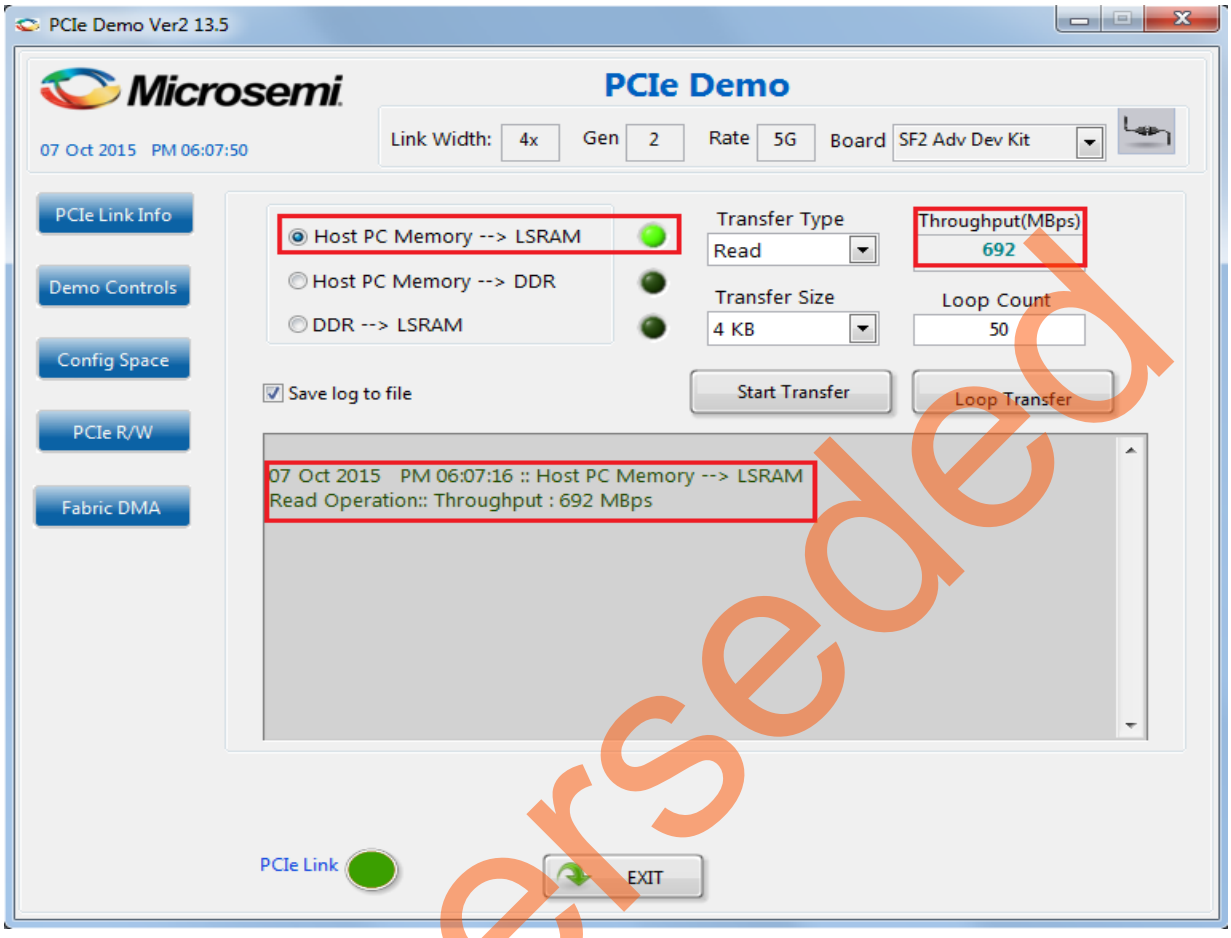

Figure 26 • **DMA between Host PC Memory and LSRAM**

17. Enter 10 in the **Loop Count** field and click **Loop Transfer** to perform 10 sequential DMA transactions. After completion of data transfer, the PCIE_DEMO application displays the throughputs as shown in Figure 27. The average throughput is also logged. The log file is stored in the Host PC at C:\PCIe_Demo\DriverInstall.

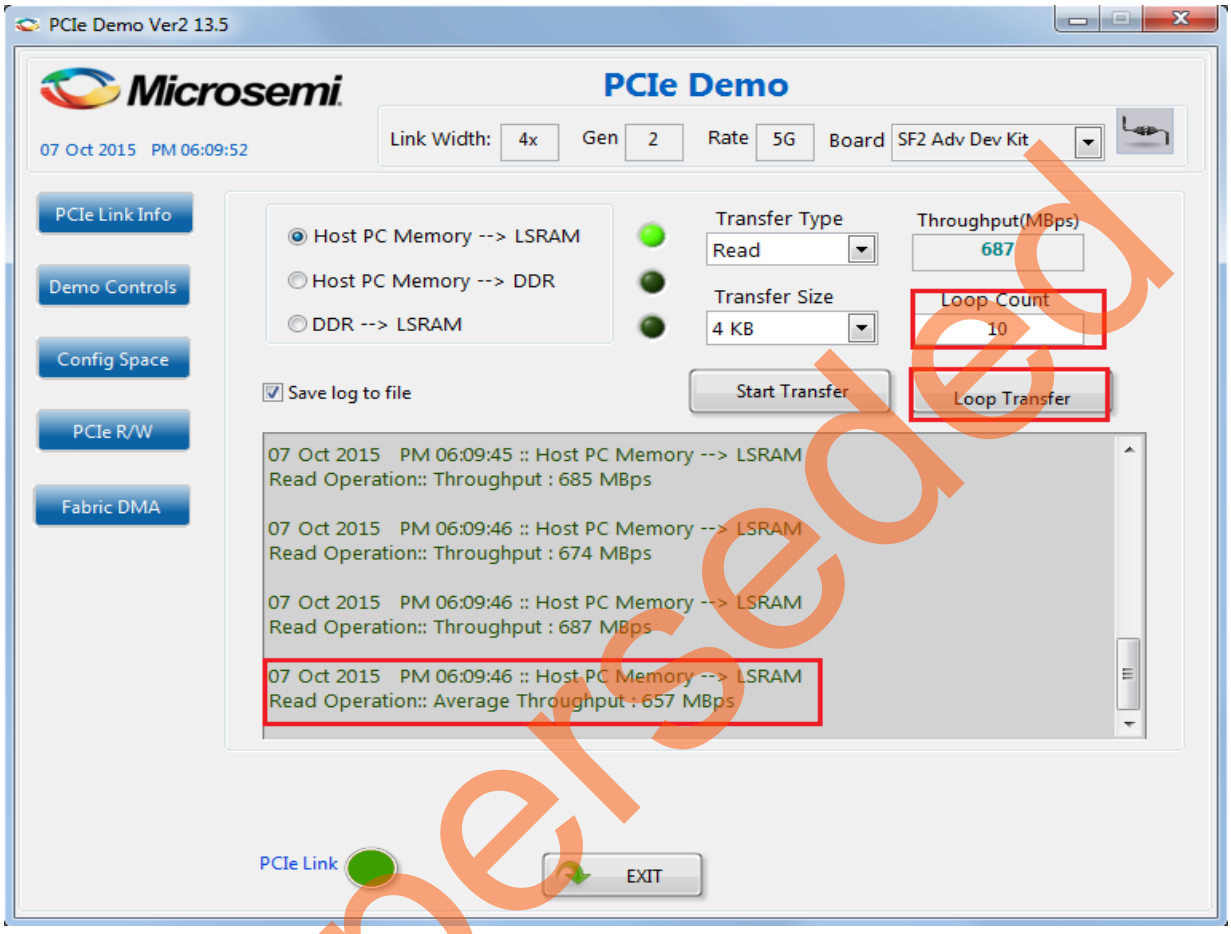

Figure 27 • **DMA between Host PC Memory and LSRAM - Loop Transfer**

18. Select **Transfer Type** as **Write** and then select **Host PC Memory < - - LSRAM** to execute DMA transactions from LSRAM to Host PC. Click **Start Transfer** to perform a single DMA transaction. After completion of data transfer the throughput is displayed as shown in Figure 28 on page 36.

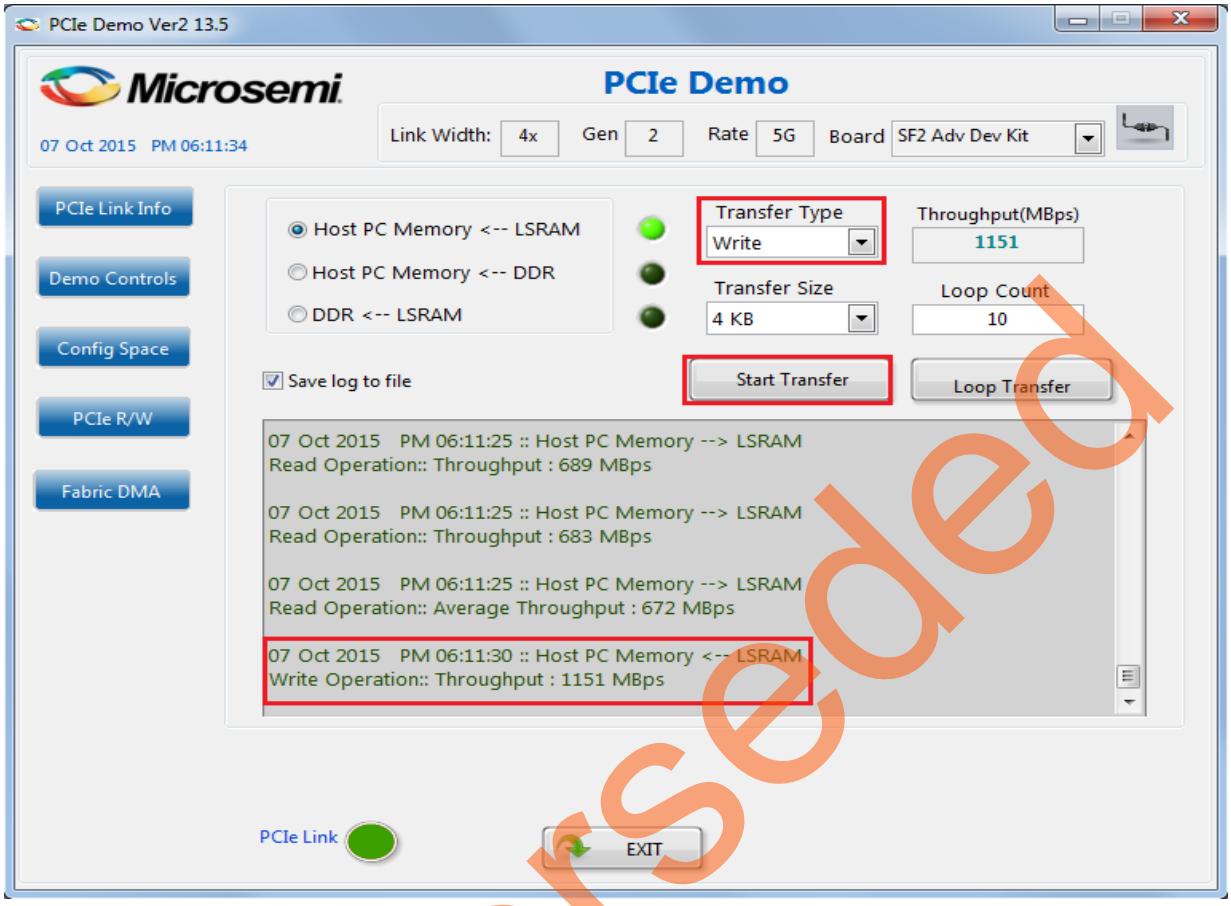

Figure 28 • **DMA between Host PC Memory and LSRAM**

19. Enter 10 in the **Loop Count** field and click **Loop Transfer** to perform 10 repeated DMA transactions. After completion of data transfer, the throughputs are displayed as shown in Figure 29.

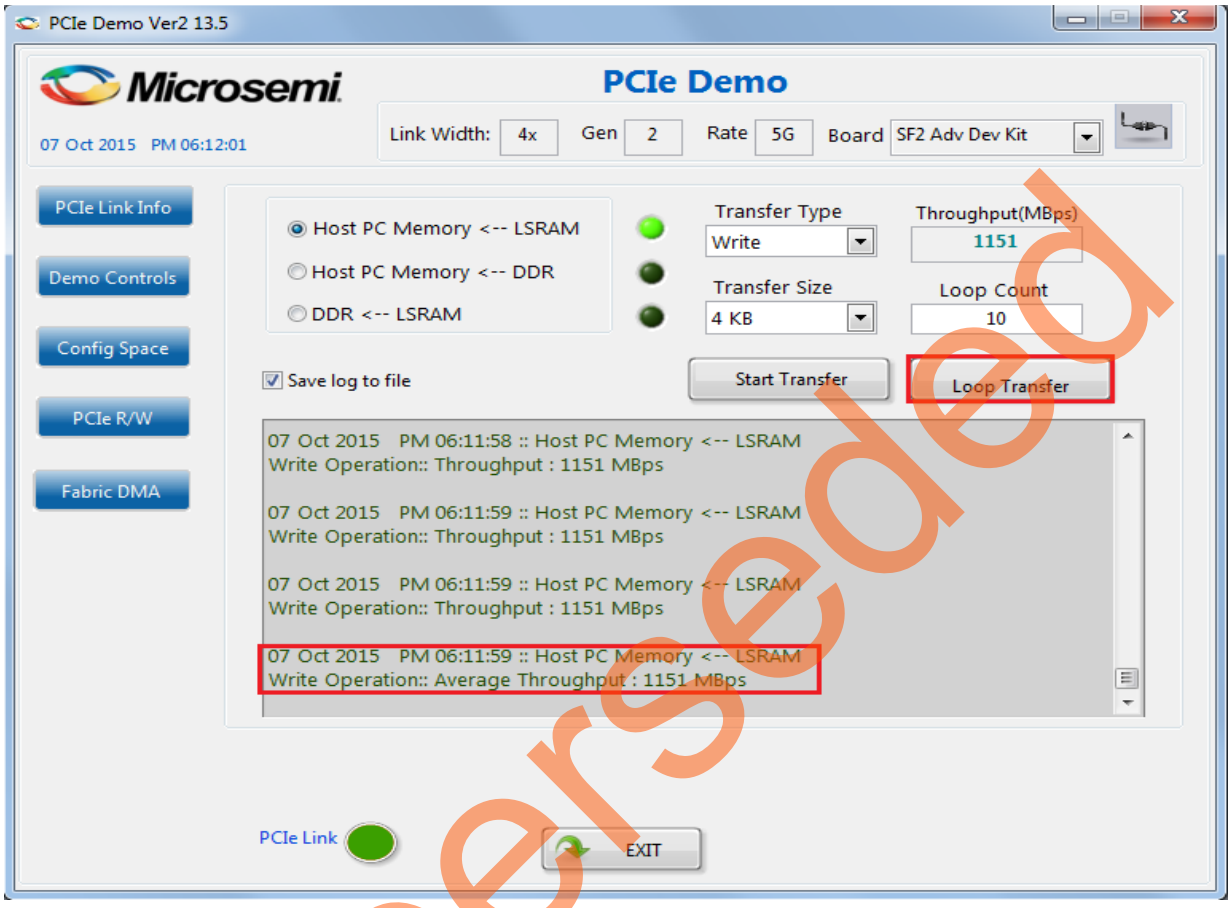

Figure 29 • **DMA between Host PC Memory and LSRAM - Loop Transfer**

20. Select **Transfer Type** as **Read/Write** to perform simultaneous read and writes. Click **Start Transfer** to perform a single DMA transaction. After completion of data transfer the throughput is displayed as shown in Figure 30.

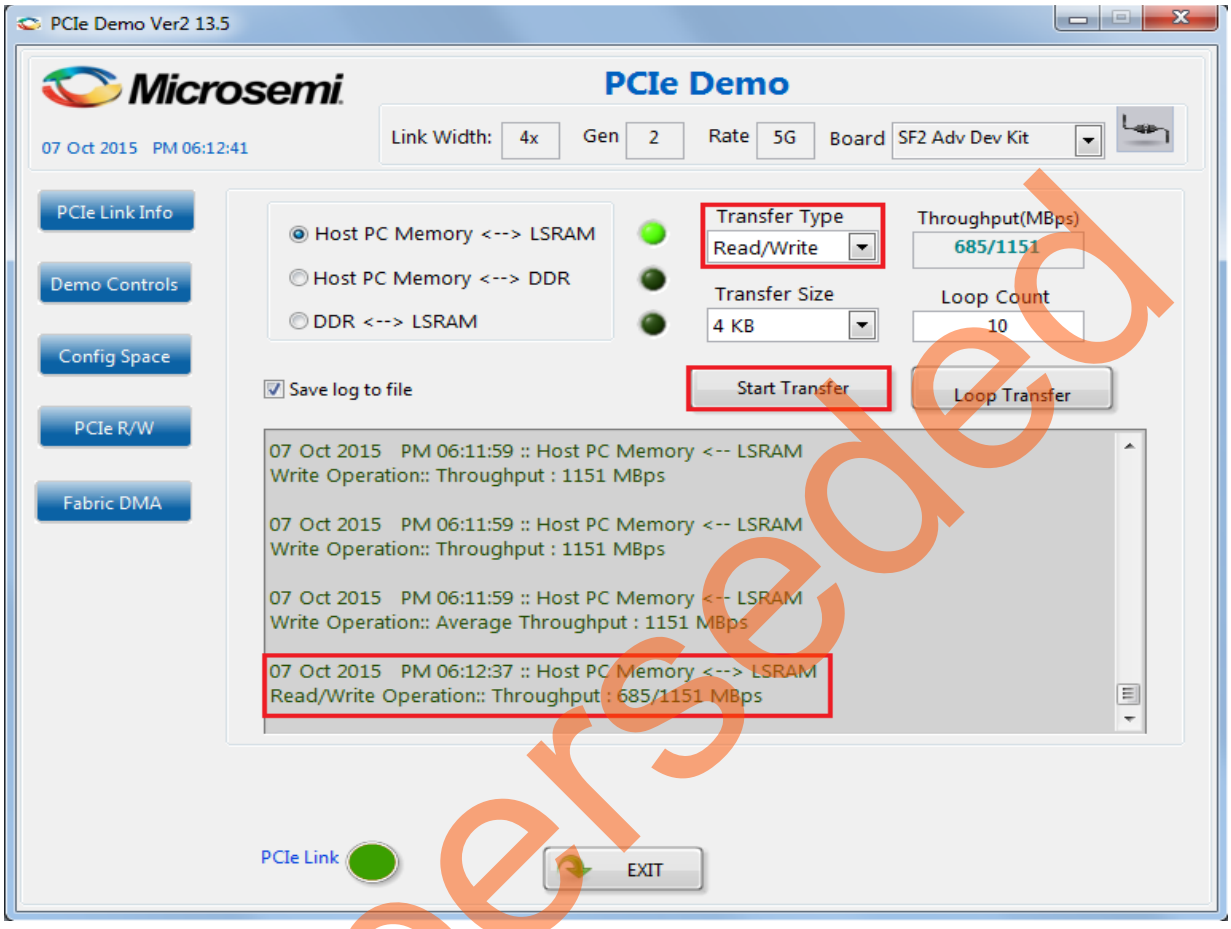

Figure 30 • **DMA between Host PC Memory and LSRAM**

21. Enter 10 in the **Loop Count** field and click **Loop Transfer** to perform 10 sequential DMA transactions. After completion of data transfer, the throughput is displayed as shown in Figure 31.

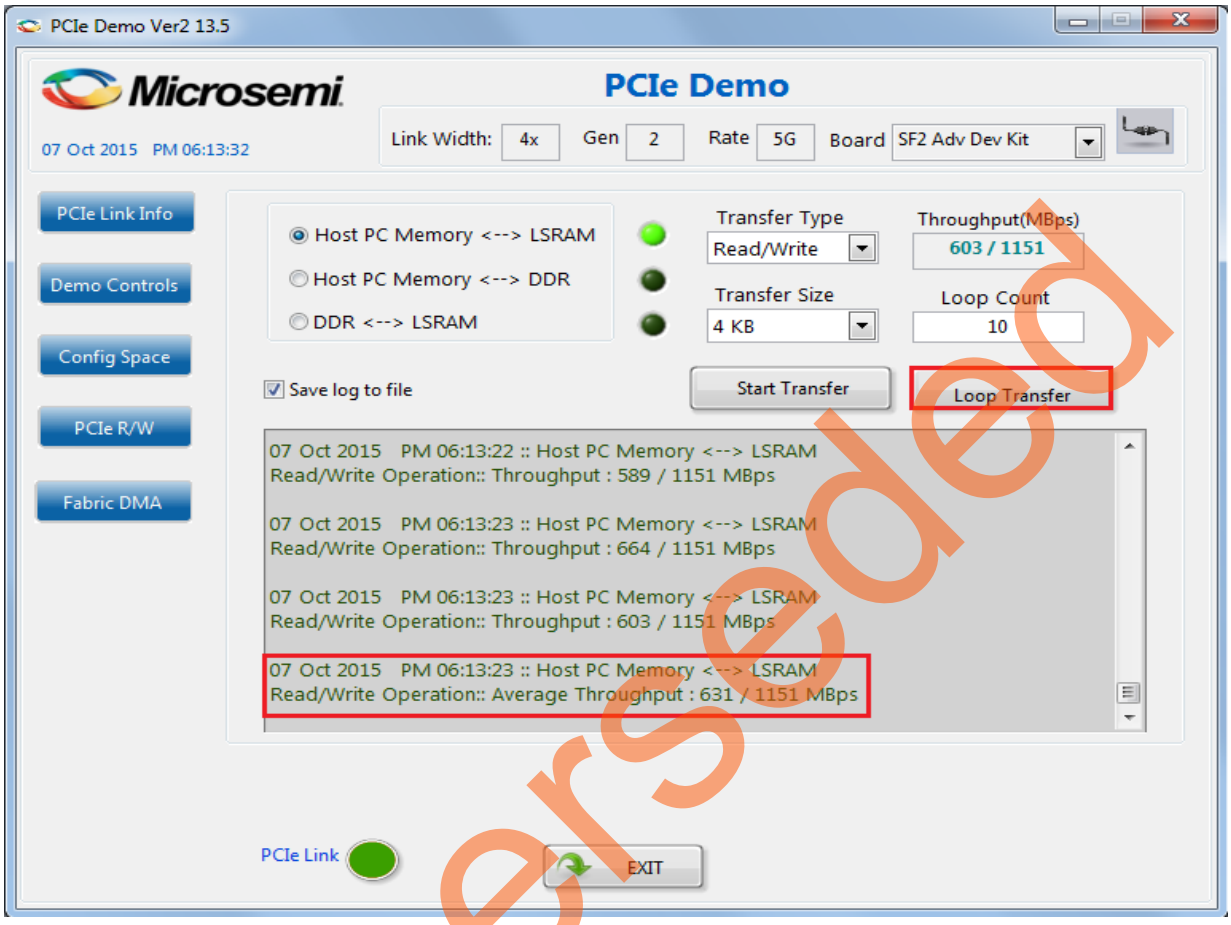

Figure 31 • **DMA between Host PC Memory and LSRAM**

22. Select the type of DMA transfer as Host PC Memory to DDR3, select **Transfer Type** as **Read/Write** to perform simultaneous read and writes. Click **Loop Transfer** to perform 10 repeated DMA transactions. After completion of data transfer the throughputs is displayed as shown in Figure 32.

    The **Transfer Type** can be selected as **Read** or **Write** also.

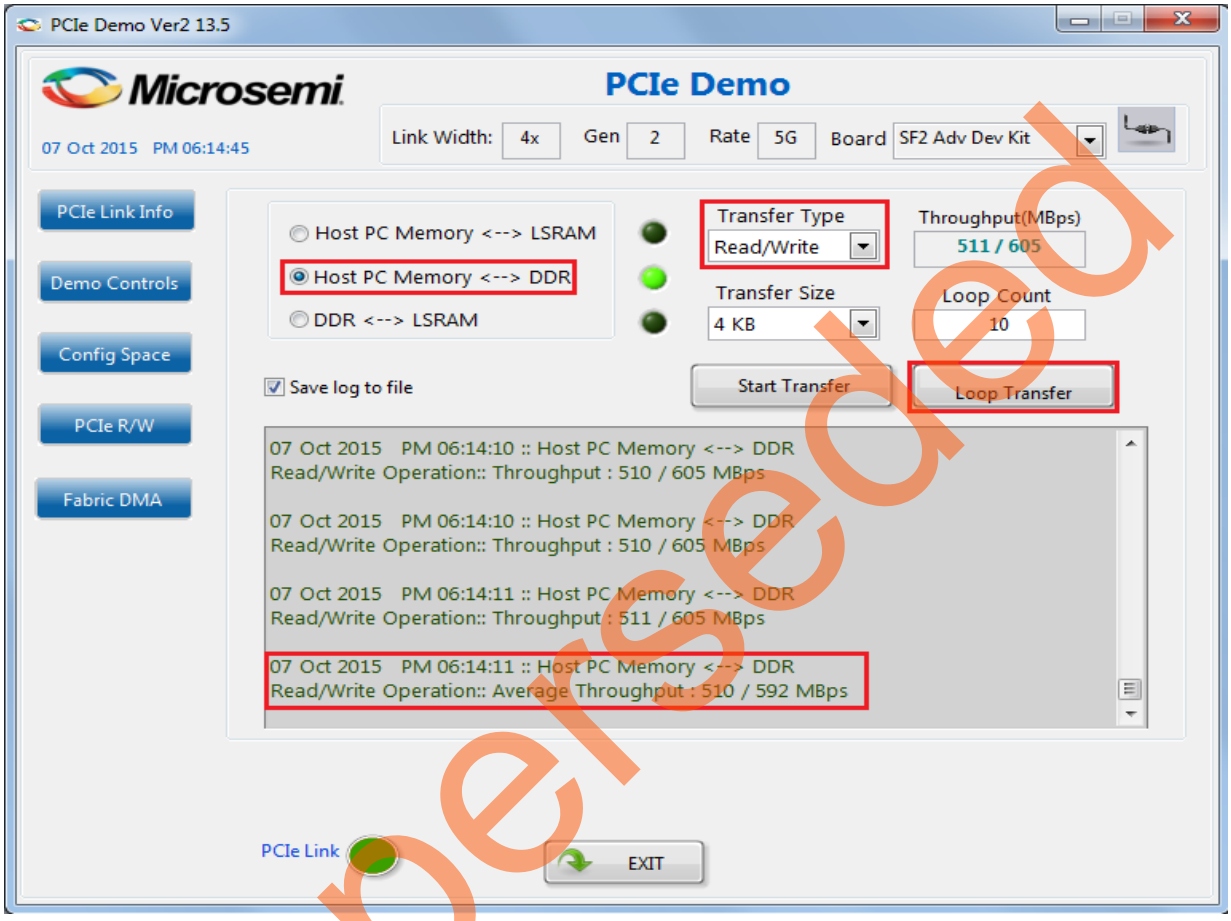

Figure 32 • **DMA between Host PC Memory and DDR**

23. Select the type of DMA transfer as LSRAM to DDR. Select **Transfer Type** as **Read/Write** to perform simultaneous read and writes. Click **Loop Transfer** to perform 10 repeated DMA transactions. After completion of data transfer, the throughput is displayed as shown in Figure 33.

    The **Transfer Type** can be selected as **Read** or **Write**.

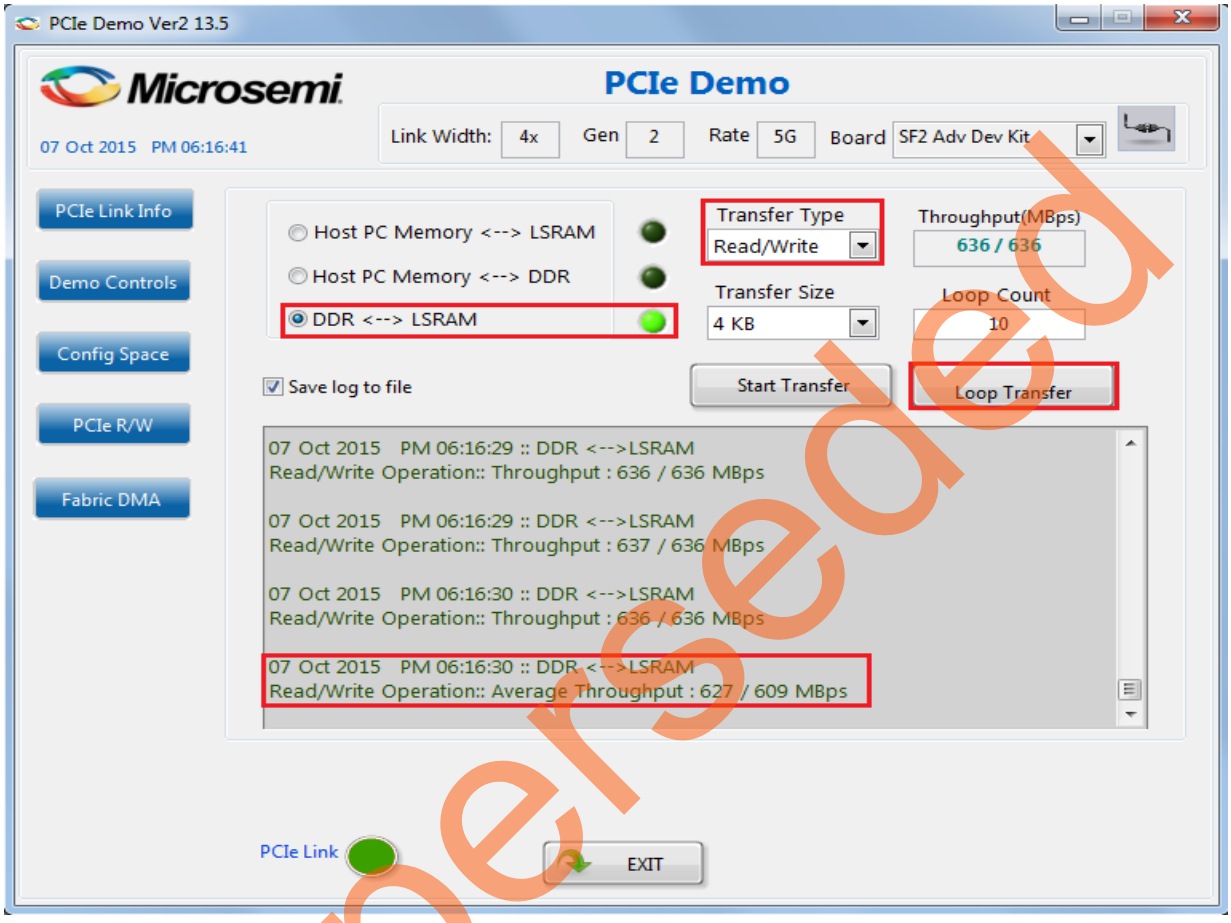

Figure 33 • **DMA between LSRAM and DDR**

24. Click **Exit** to quit the demo.

Summary

This demo shows how to implement a PCIe Data Plane Design using AXI based fabric DMA controller. Throughput for data transfers is dependent on Host PC system configuration and type of PCIe slots used. Table 4 shows the throughput values observed on the HP Workstation Z220 PCIe slot 4.

Table 4 • **Throughput Summary**

DMA Transfer Type		Throughput in Mbytes/sec							
		SmartFusion2 (X4 Lane)				IGLOO2 (X1 Lane)			
		Gen1		Gen2		Gen1		Gen2	
		Single xfer	Loop xfer (50)	Single xfer	Loop xfer (50)	Single xfer	Loop xfer (50)	Single xfer	Loop xfer (50)
Host PC to LSRAM	Read	545	540	1125	1085	180	177	363	359
	Write	812	808	1151	1151	237	236	492	490
	R/W	542/811	540/810	1125/1151	1088/1151	180/237	180/236	361/491	360/490
DDR to LSRAM	Read	638	623	638	623	555	550	555	550
	Write	636	620	636	620	355	355	355	355
	R/W	637/636	627/609	637/636	627/609	554/355	554/345	554/355	554/345
Host PC to DDR	Read	531	532	635	623	178	178	299	295
	Write	626	624	626	605	232	232	430	425
	R/W	530/620	530/626	635/626	623/605	177/232	177/231	312/447	313/446

Appendix 1: IGLOO2 Evaluation Kit Board Setup for Laptop

Figure 1 shows how to line up the IGLOO2 Evaluation Kit PCIe connector with the adapter card slot.

Figure 1 • **Lining up the IGLOO2 Evaluation Kit Board**

Note: The Notch (highlighted in red) does not go into the adapter card.

Figure 2 shows IGLOO2 Evaluation Kit PCIe connector inserted into the PCIe adapter card slot.

Figure 2 • **Inserting the IGLOO2 Evaluation Kit PCIe Connector**

Figure 3 shows the PCIe adapter card and the IGLOO2 Evaluation Kit connected to the laptop.

Figure 3 • **IGLOO2 Evaluation Kit Connected to the Laptop**

Appendix 2: Register Details

Table 1 shows the registers used to interface with the Fabric DMA Controller. These registers are in BAR1 address space.

Table 1 • **Register Details**

Register Name	Register Address	Description
PC_BASE_ADDR	0x8028	Host PC memory base address provided by the driver.
DMA_DIR	0x8008	DMA direction: **Direction** — **Register Value** 1. PCIe → DDR memory — 0x11AA0001 2. DDR → PCIe memory — 0x11AA0002 3. LSRAM → DDR memory — 0x11AA0003 4. DDR → LSRAM memory — 0x11AA0004 5. PCIe → LSRAM memory — 0x11AA0005 6. LSRAM → PCIe memory — 0x11AA0006 To reset the DMA, the register value is 0x11AA0007. *Note: Before initiating DMA transactions, reset the DMA with the register value, 0X11AA0007.* *Note: The DMA transactions 1 and 2, 3 and 4, or 5 and 6 can be performed simultaneously by writing the corresponding values one after other.*
DMA_CH0_STATUS	0x8100	DMA Channel-0 status • DMA_CH0_STATUS[31] 1 = DMA operation completed 0 = DMA operation not completed • DMA_CH0_STATUS[15:0] = CLK count
DMA_CH1_STATUS	0x8108	DMA Channel-1 status • DMA_CH1_STATUS[31] 1 = DMA operation completed 0 = DMA operation not completed • DMA_CH1_STATUS[15:0] = CLK count
RW_REG	0X0	Scratchpad register for PCIe R/W.
LED_CTRL	0xA0	LEDs control register.
SWITCH_STATUS	0x90	DIP switch status.
Note: For the DDR memory, the source memory address is fixed as 0x0100_0000 and the destination memory address is fixed as 0x0000_0000.		

A – List of Changes

The following table shows important changes made in this document for each revision.

Date	Changes	Page
Revision 6 (October 2015)	Updated the document for Libero v11.6 software updates (SAR 72063).	NA
Revision 5 (August 2014)	Updated the designs files links.	NA
Revision 4 (July 2014)	Updated the document for Libero v11.4 software updates (SAR 59587).	NA
Revision 3 (April 2014)	Updated document for Libero v11.3 and for other enhancements (SAR 56080).	N/A
	MDDR throughput displayed in Mbps (SAR 53589).	N/A
	Throughput for Read and Write Transfer type is reversed in Throughput "Summary" section (SAR 53822).	42
	Updated throughput values in "Summary" section (SAR 53490).	42
Revision 2 (December 2013)	Updated Table 4 (SAR 53490).	42
Revision 1 (December 2013)	Initial Release	NA

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You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

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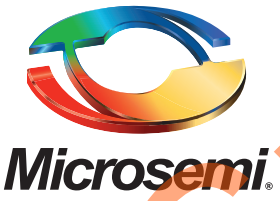

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