SmartFusion2 SoC FPGA DSP FIR Filter - Libero SoC v11.6

DG0438 Demo Guide

October 2015

Microsemi

Revision History

Date	Revision	Change
7 October 2015	5	Sixth release
28 January 2015	4	Fifth release
22 August 2014	3	Fourth release
2 July 2014	2	Third release
30 November 2013	1	Second release
22 April 2013	0	First release

Confidentiality Status

This is a non-confidential document.

Table of Contents

Preface

About this document

This demo is for SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) devices. It provides instructions on how to use the corresponding reference design.

Intended Audience

SmartFusion2 devices are used by:

- FPGA designers
- Embedded designers
- System-level designers

References

Microsemi Publications

- *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*
- *SmartFusion2 System Builder User Guide*
- *SmartFusion2/IGLOO2 Digital Signal Processing Reference Guide*

Refer to the following web page for a complete and up-to-date listing of SmartFusion2 device documentation: *http://www.microsemi.com/products/fpga-soc/soc-fpga/sf2docs*

SmartFusion2 SoC FPGA - DSP FIR Filter Demo

Introduction

SmartFusion2 SoC FPGA devices integrate a fourth generation flash-based FPGA fabric and an ARM® Cortex®-M3 processor. SmartFusion2 SoC FPGA fabric includes embedded mathblocks, which are optimized specifically for digital signal processing (DSP) applications such as, finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast fourier transform (FFT) functions.

This demo shows a DSP FIR filter application using the SmartFusion2 device. In this DSP FIR filter application, the FIR filter is implemented in fabric for Low pass, High pass, Band pass, and Band reject filtering operations. The Host interface is implemented in microcontroller subsystem (MSS) to communicate with the Host PC. A user friendly graphical user interface (GUI) generates the filter coefficients, input signals (Pass-band frequency + Stop-band frequency) and also plots the input/output waveforms and the required spectrum. Microsemi® CoreFIR filter IP is used to suppress the unwanted frequency components, and CoreFFT IP is used to generate the output spectrum to verify the filtering operation.

Figure 1 shows the top-level diagram for DSP FIR filter demo.

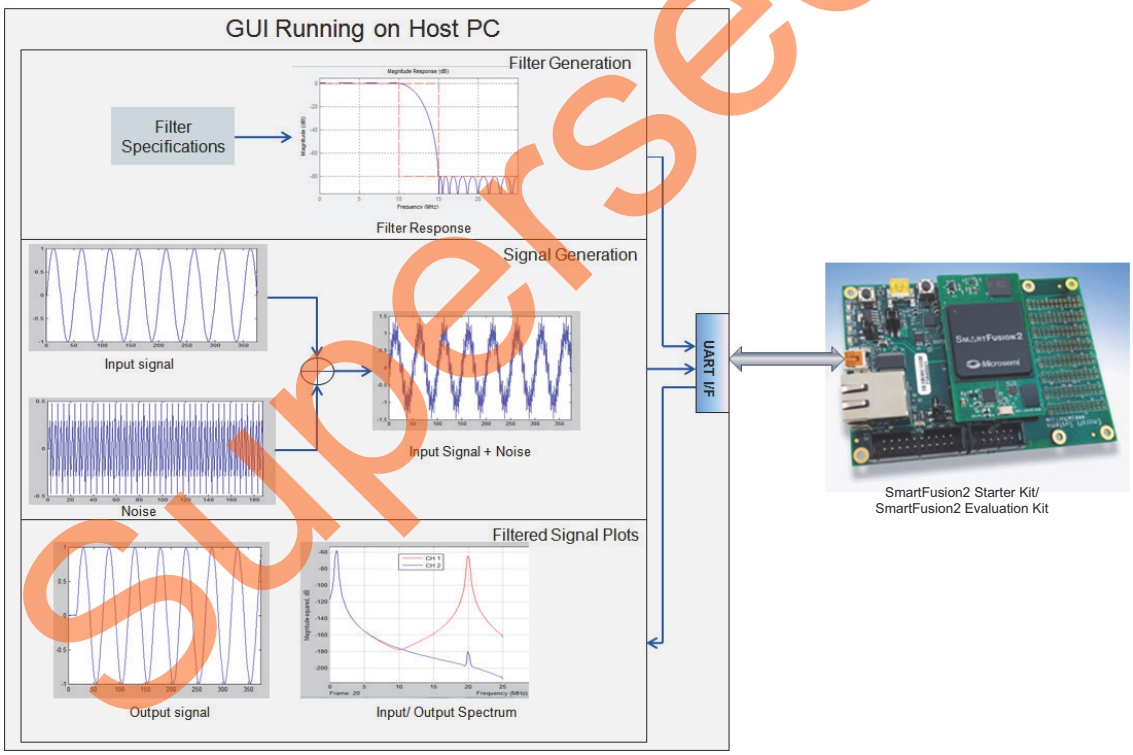

***Figure 1* • Top-Level Diagram of DSP FIR Filter Demo**

Design Requirements

Table 1 • **Design Requirements**

Design Requirements	Description
Hardware Requirements	
SmartFusion2 Starter Kit • FlashPro4 programmer • USB A to Mini-B cable	SF2-484-STARTER-KIT (M2S010-FGG484)
SmartFusion2 Security Evaluation Kit • FlashPro4 programmer • USB A to Mini-B cable	Rev D or later (M2S090TS-FGG484)
Host PC or Laptop	Windows 7 64-bit Operating System
Software Requirements	
Libero® System-on-Chip (SoC)	v11.6
FlashPro Programming Software	v11.6
Host PC Drivers	USB to UART drivers
Framework	Microsoft .NET Framework 4 client for launching demo GUI

Demo Design

Introduction

The design files are available for download from the following paths in the Microsemi website:

- SmartFusion2 Starter Kit:
  http://soc.microsemi.com/download/rsc/?f=m2s_dg0438_starter_fir_filter_liberov11p6_df
- SmartFusion2 Security Evaluation Kit:
  http://soc.microsemi.com/download/rsc/?f=m2s_dg0438_eval_fir_filter_liberov11p6_df

The design files include:

- Design files
- Programming file
- GUI executable
- Readme.txt file

Figure 2 shows the top-level structure of the SmartFusion2 Starter Kit design files. Refer to the Readme.txt file provided in the demo file folder for the complete directory structure.

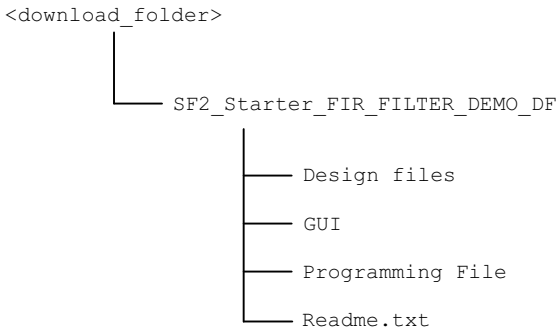

***Figure 2* • SmartFusion2 Starter Kit Demo Design Files Top-Level Structure**

Figure 3 shows the top-level structure of the SmartFusion2 Security Evaluation Kit design files. Refer to the Readme.txt file provided in the demo file folder for the complete directory structure.

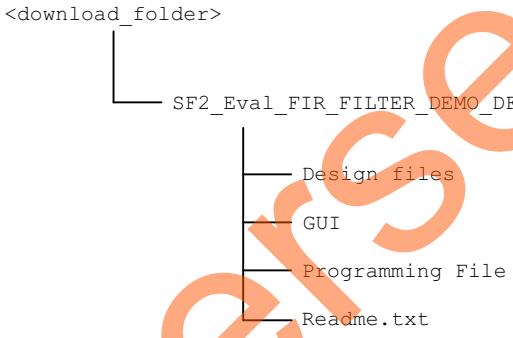

***Figure 3* • SmartFusion2 Security Evaluation Kit Demo Design Files Top-Level Structure**

Demo Design Description

This demo design uses the following blocks:

- "MSS Block"
- "Control Logic" (user RTL)
- "TPSRAM IP" (IPcore)
- "CoreFIR" (IPcore)
- "CoreFFT" (IPcore)

Figure 4 shows the detailed block diagram of the demo design.

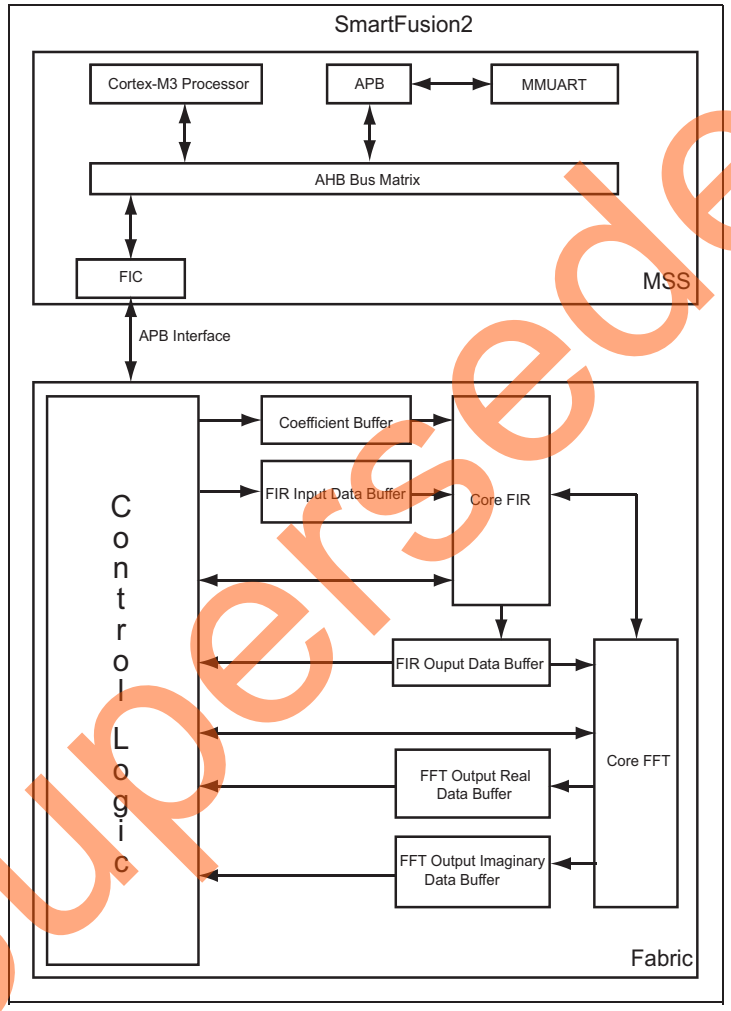

***Figure 4* • DSP FIR Filter Demo Design Block Diagram**

MSS Block

MSS block sends and receives the data between Host PC (GUI interface) and fabric logic. MMUART interface is used to communicate with the Host PC. FIC_0 interface (APB master) is used to communicate with the fabric user logic.

Control Logic

This is the user logic implemented in the fabric and consists of the following two finite-state machine (FSM)s:

- **Data Handling**: Implements and controls operations like loading the filter input data to the corresponding input data buffer and loading filter coefficients to the corresponding coefficient memory buffers. An APB bus slave is implemented to communicate with the MSS APB master.
- **Filter Control**: Controls the FIR filter and FFT operations. Loads the filtered data to corresponding output buffer and moves the FFT output data to the corresponding output data buffer.

TPSRAM IP

TPSRAM IP is used to implement the following:

- Filter coefficient buffer (depth: 63, width: 16)
- Input signal data buffer (depth: 1024, width: 16)
- Output signal buffer (depth: 1024, width: 16)
- Output signal FFT real data buffer (depth: 1024, width: 16)
- Output signal FFT imaginary data buffer (depth: 1024, width: 16)

CoreFIR

The Core FIR IP is used in Reloadable coefficient mode to support Low pass, High pass, Band pass, and Band reject filters. Core FIR IP configuration is as follows:

- Version: 8.5.104
- Filter Type: Single rate fully enumerated
- No of taps: 31
- Coefficients type: Reloadable
- Coefficients bit width: 16(signed)
- Data bit width: 16 (signed)
- Filter structure: Transposed with symmetry

CoreFFT

The Core FFT IP is used for generating the frequency spectrum of the filtered data. Core FFT IP configuration is as follows:

- Version: 6.3.102
- FFT Architecture: In place
- FFT type: Forward
- FFT Scaling: Conditional
- FFT Transform Size: 256
- Width: 16

Setting Up the Demo Design

Setting Up the Demo Design for SmartFusion2 Starter Kit

The following steps describe how to setup the hardware demo for SmartFusion2 Starter Kit:

1. Connect the jumpers on the SmartFusion2 Starter Kit board as shown in Table 2.

Table 2 • **SmartFusion2 Starter Kit Jumper Settings**

Jumper	Configuration	Comments
JP1	1-2 Close, 3-4 Open	Enable power on the M2S-FG484 SOM (VCC3).
JP2	1-2 Open, 3-4 Close	Select appropriate JTAG mode and enable power to the SmartFusion2 JTAG controller.
JP3	1-3 Open, 2-4 Close	Use the mini-USB port as the power source.

2. Connect the FlashPro4 programmer to the P5 connector of the SmartFusion2 Starter Kit board.
3. Connect the Host PC USB port to the P1 Mini USB connector on the SmartFusion2 Starter Kit board using the USB Mini-B cable.

   Figure 5 shows the board setup for running the DSP FIR filter demo on the SmartFusion2 Starter Kit.

Figure 5 • **SmartFusion2 SoC FPGA Starter Kit Setup**

4. Ensure that the USB to UART bridge drivers are automatically detected. This can be verified in the **Device Manager** of the Host PC. Figure 6 shows the USB Serial port.

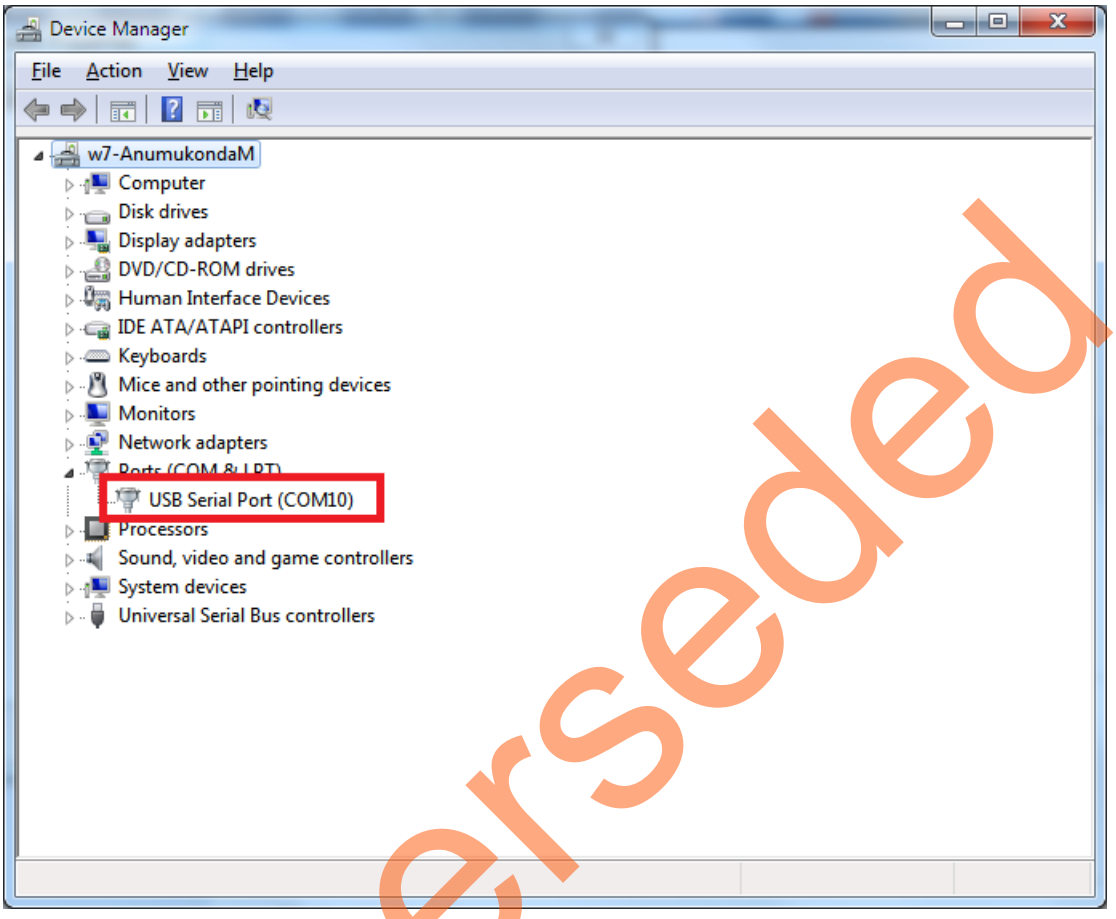

***Figure 6* • USB to UART Bridge Drivers for SmartFusion2 Starter Kit**

5. If USB to UART bridge drivers are not installed, download and install the drivers from *www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip*.

Setting Up the Demo Design for SmartFusion2 Security Evaluation Kit

The following steps describe how to setup the hardware demo for SmartFusion2 Security Evaluation Kit:

1. Connect the jumpers on the SmartFusion2 Security Evaluation Kit board as shown in Table 3.

Table 3 • **SmartFusion2 Security Evaluation Kit Jumper Settings**

Jumper	Configuration	Comments
J23	–	Jumper to select switch-side MUX inputs of A or B to the lineside.
	Close	Pin 1-2 (Input A to the lineside) that is on board 125 MHz differential clock oscillator output will be routed to lineside.
	Open	Pin 2-3 (Input B to the lineside) that is external clock required to source through SMA connectors to the lineside.
J22	–	Jumper to select the output enables control for the lineside outputs.
	Close	Pin 1-2 (Lineside output enabled)
	Open	Pin 2-3 (Lineside output disabled)
J24	Open	Jumper to provide the VBUS supply to USB when using in Host mode.
J8	–	JTAG selection jumper to select between RVI header or FP4 header for application debug.
	Close	Pin 1-2 FP4 for SoftConsole/FlashPro
	Open	Pin 2-3 RVI for Keil™ ULINK™/IAR J-Link®
	Open	Pin 2-4 for Toggling JTAG_SEL signal remotely using GPIO capability of FT4232 chip.
J3	–	Jumpers to select either SW2 input or signal ENABLE_FT4232 from FT4232H chip.

Notes:

1. Ensure that the power supply switch SW7 is OFF while making the jumper connections.
2. Connect the Power supply to the J6 connector, switch on the power supply switch, SW7.

2. Connect the FlashPro4 programmer to the J5 connector of the SmartFusion2 Security Evaluation Kit board.
3. Connect the Host PC USB port to the P1 Mini USB connector on the SmartFusion2 Security Evaluation Kit board using the USB Mini-B cable.

Figure 7 shows the board setup for running the DSP FIR filter demo on the SmartFusion2 Security Evaluation Kit.

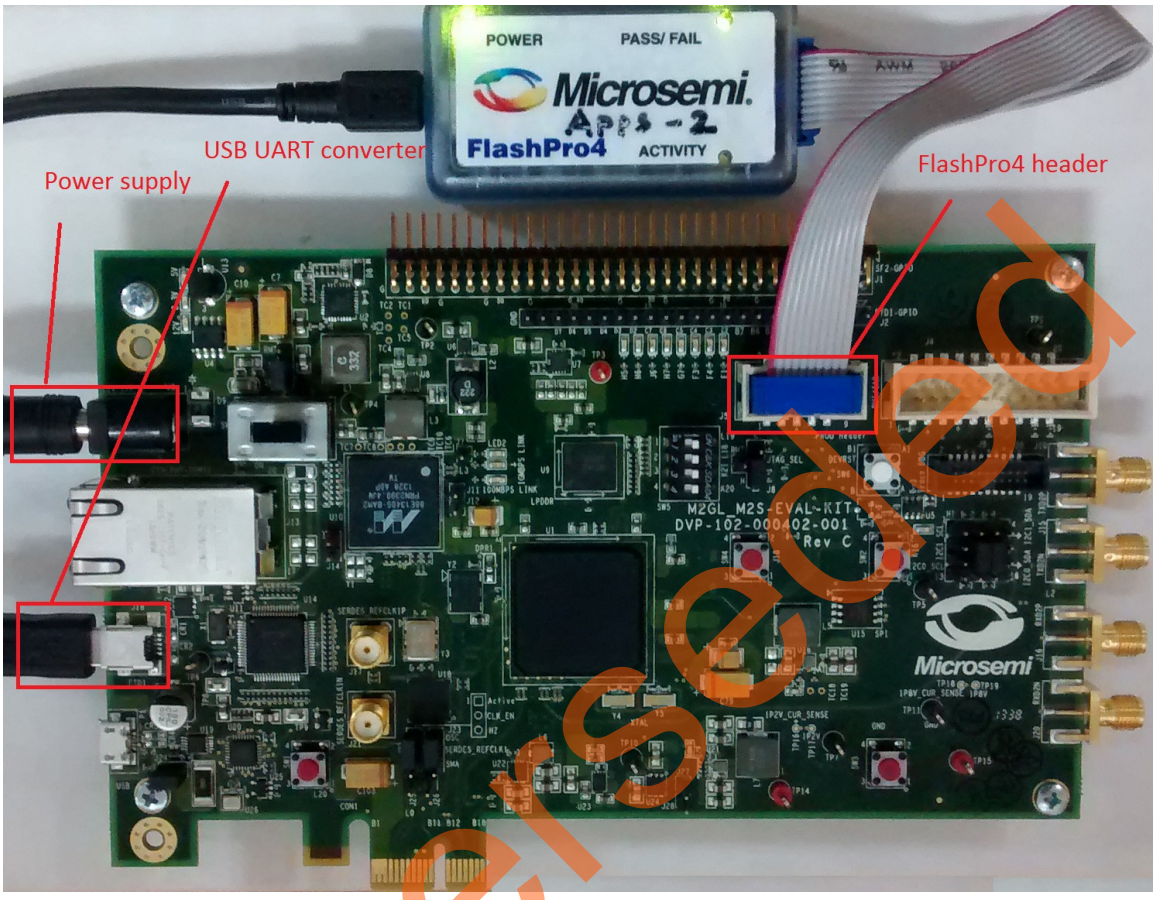

Figure 7 • **SmartFusion2 Security Evaluation Kit Setup**

4. Switch **ON** the SW7 power supply switch.

5. Ensure that the USB to UART bridge drivers are automatically detected. This can be verified in the **Device Manager** of the Host PC. Figure 8 shows the USB Serial port.

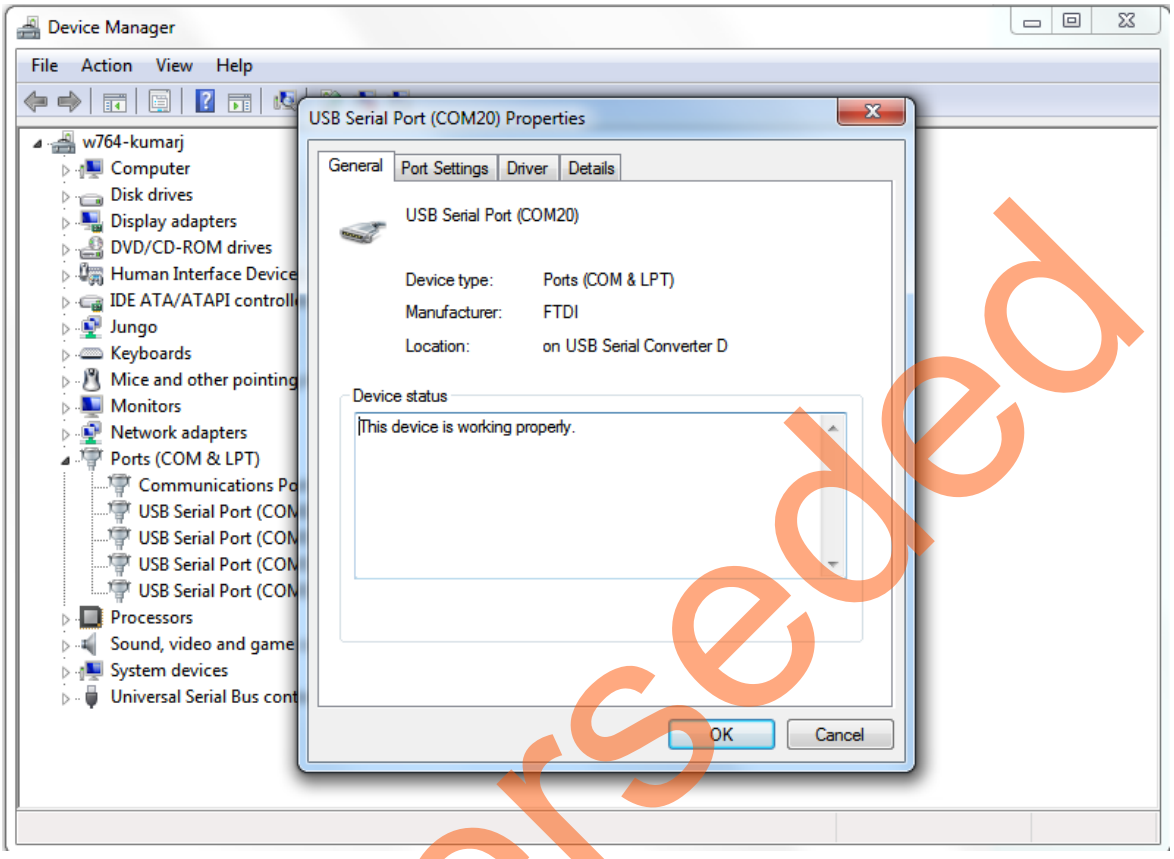

***Figure 8* • USB to UART Bridge Drivers for SmartFusion2 Security Evaluation Kit**

6. If USB to UART bridge drivers are not installed, download and install the drivers from *www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip*.

Programming the Demo Design

The following steps describe how to program the demo design from the following links:

1. Download the demo design from:
   - SmartFusion2 Starter Kit: *http://soc.microsemi.com/download/rsc/?f=m2s_dg0438_starter_fir_filter_liberov11p6_df*
   - SmartFusion2 Security Evaluation Kit: *http://soc.microsemi.com/download/rsc/?f=m2s_dg0438_eval_fir_filter_liberov11p6_df*
2. Launch the FlashPro software.
3. Click **New Project**.

4. In the **New Project** window, enter the project name as SF2_FIR_FILTER.

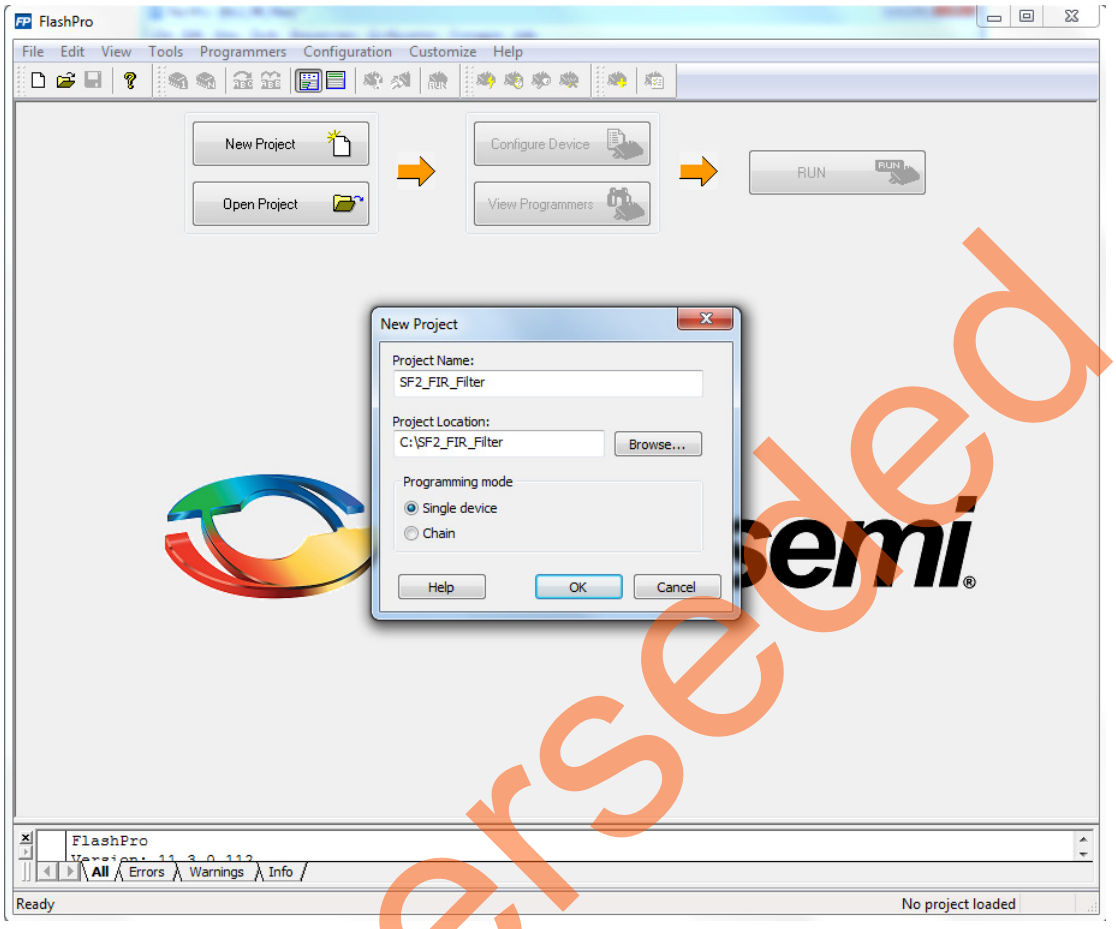

***Figure 9* • FlashPro - New Project**

5. Click **Browse** and navigate to the location where you want to save the project.
6. Select **Single device** as the **Programming mode**.
7. Click **OK** to save the project.

Setting Up the Device

The following steps describe how to configure the device:

1. Click **Configure Device** on the FlashPro GUI.
2. Click **Browse** and navigate to the location where the `FILTER_FIR_DEMO.stp` file is located and select the file. The default location of the programming file is:
   - SmartFusion2 Starter Kit:
     <download_folder>\SF2_Starter_FIR_FILTER_DEMO_DF\Programming File\FIR_FILTER_top.stp
   - SmartFusion2 Security Evaluation Kit:
     <download_folder>\SF2_Eval_FIR_FILTER_DEMO_DF\Programming File\FIR_FILTER_top.stp
3. Click **Open**. The required programming file is selected and is ready to be programmed in the device.
4. Select **Advanced** as Mode and **PROGRAM** as Action.

Programming the Device

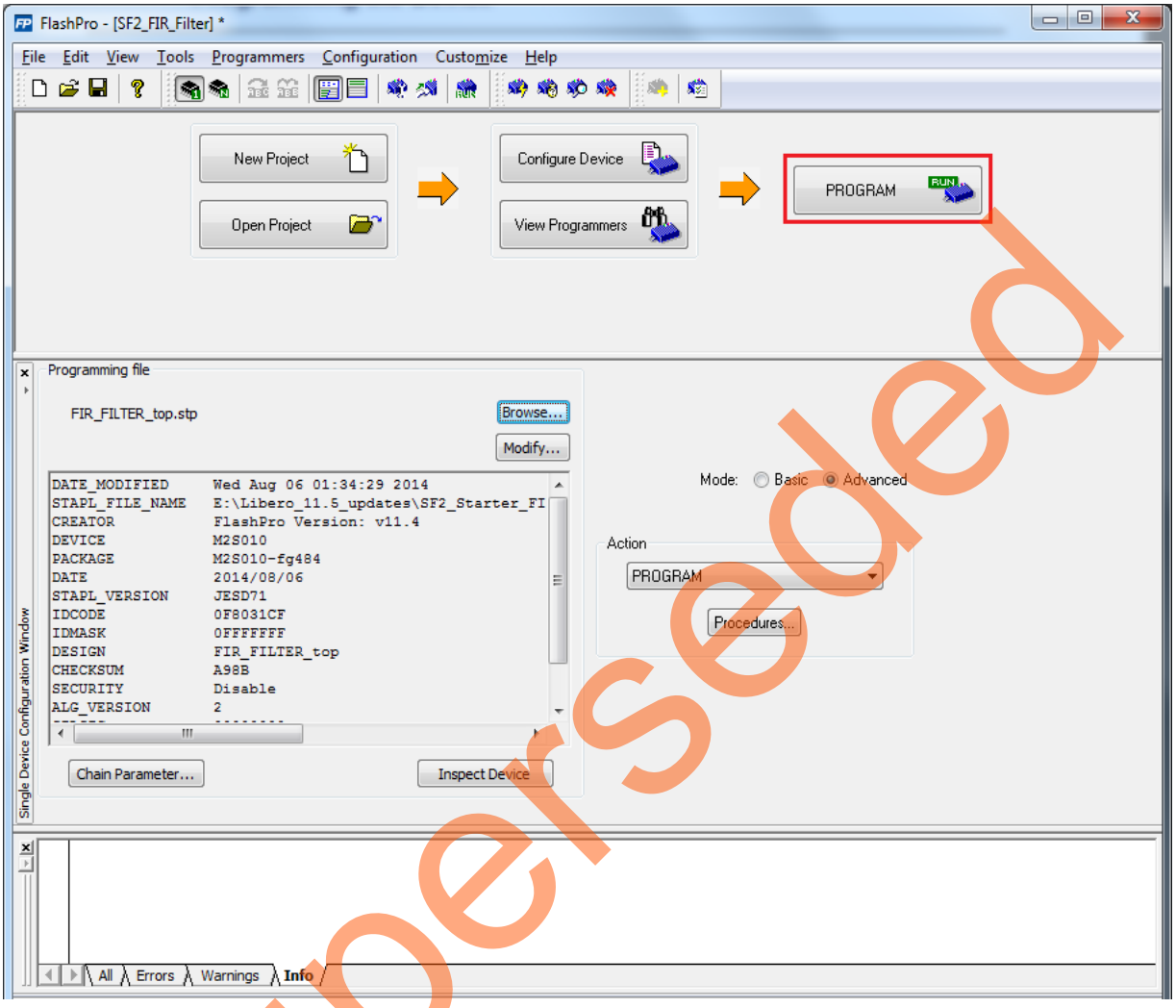

***Figure 10* • FlashPro Project Configuration**

Click **PROGRAM** to start programming the device. Wait until programmer status is changed to **RUN PASSED**.

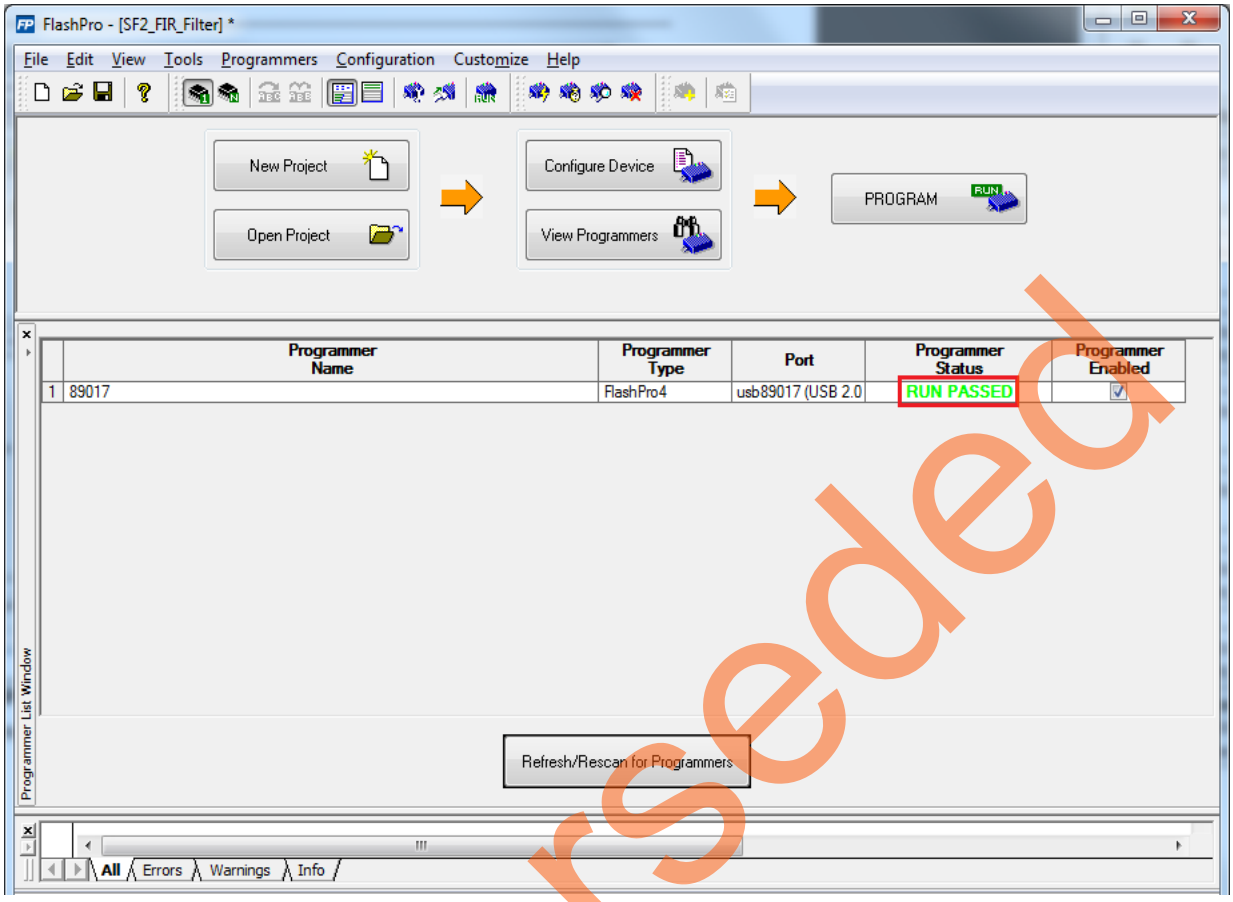

Figure 11 • **FlashPro Project RUN Passed**

DSP FIR Demo GUI

The DSP FIR demo is provided with a user-friendly GUI that runs on the Host PC which communicates with the SmartFusion2 Starter Kit. The UART is used as the underlying communication protocol between the Host PC and SmartFusion2 Starter Kit/SmartFusion2 Security Evaluation Kit. Figure 12 shows the DSP FIR demo GUI.

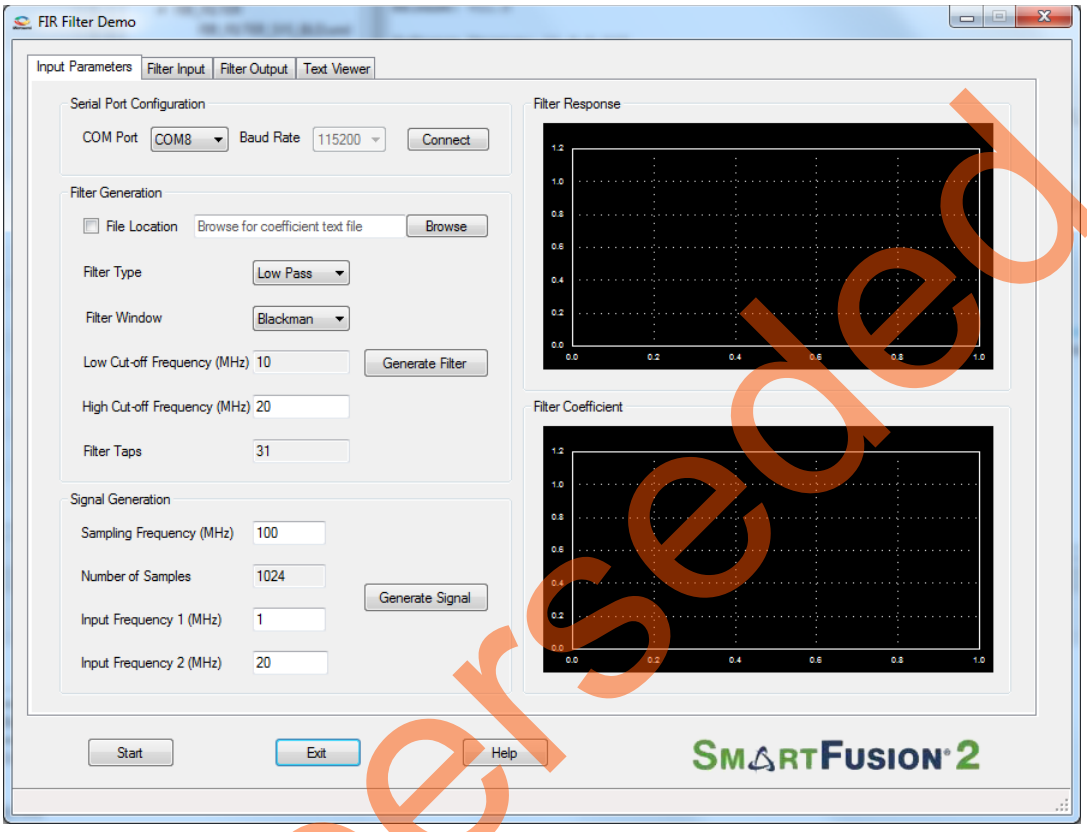

***Figure 12* • DSP FIR Demo Window**

The DSP FIR demo window consists of the following tabs:

- **Input Parameters**: Configures the serial COM port, filter generation, and signal generation.
- **Filter Input**: Plots the input signal and its frequency spectrum
- **Filter Output**: Plots the output signal and its frequency spectrum
- **Text Viewer**: Shows the coefficients, input signal, output signal, and FFT data values

Click **Help** for more information on the GUI.

Running the Demo Design

1. Launch the DSP FIR demo GUI, install and invoke the executable file provided with the design files. The default location of the executable file is:
   – SmartFusion2 Starter Kit:
   <download_folder>\SF2_Starter_FIR_FILTER_DEMO_DF\GUI\SF2_FIR_Filter.exe
   – SmartFusion2 Security Evaluation Kit:
   <download_folder>\SF2_Eval_FIR_FILTER_DEMO_DF\GUI\SF2_FIR_Filter.exe

   The FIR Filter Demo window is displayed, refer to Figure 13.

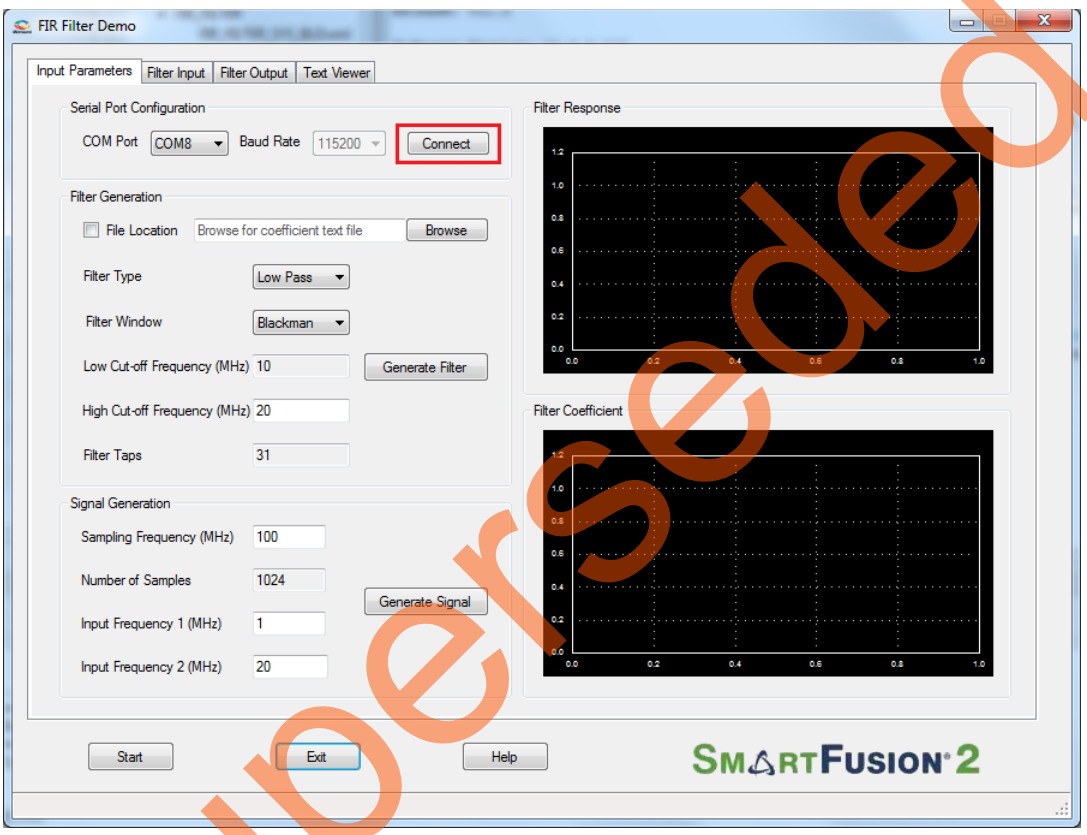

***Figure 13* • Serial Port Configuration**

2. **Serial Port Configuration**: The COM port number is automatically detected and baud rate is fixed at 115200. Click **Connect** as shown in Figure 13.
3. **Filter Generation**: Two options are provided for generating the filter coefficients:

- Generate the coefficients using MATLAB or any similar tool and save it as a text file (Refer "Appendix 3: Coefficient Text File Format" for the format of the text file). The GUI can be used to browse and load this file as shown in Figure 14.

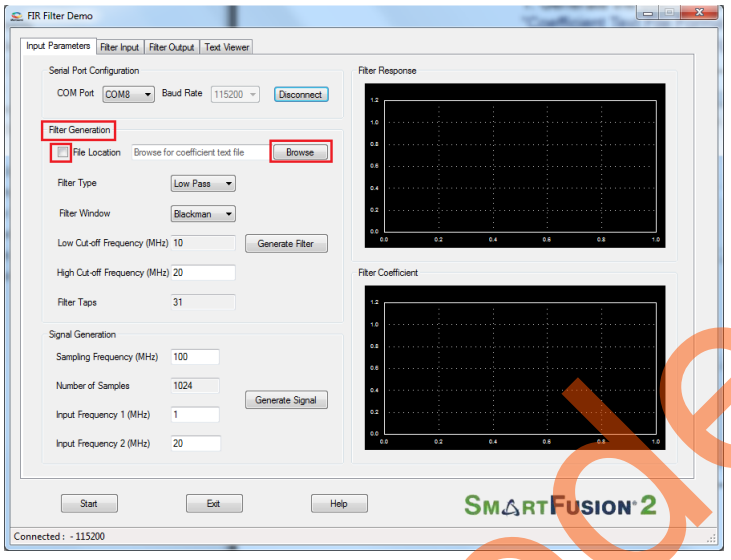

***Figure 14* • Filter Generation - 1**

- Generate the Filter coefficients using GUI as given below:

The following parameters are required to generate filter coefficients. Refer to Figure 15.

- **Filter Type**: Low Pass (Low-pass/High-pass /Band-pass/Band-reject filter)
- **Filter Window**: Blackman (Blackman/Hamming window)
- **Low Cut-off Frequency**: Disabled for Low-pass filter required (High cut-off frequency is disabled for High-pass filter)
- **High Cut-off Frequency**: 20 MHz
- **Filter Taps**: 31 (Fixed)

Press **Generate Filter** to generate the filter coefficients.

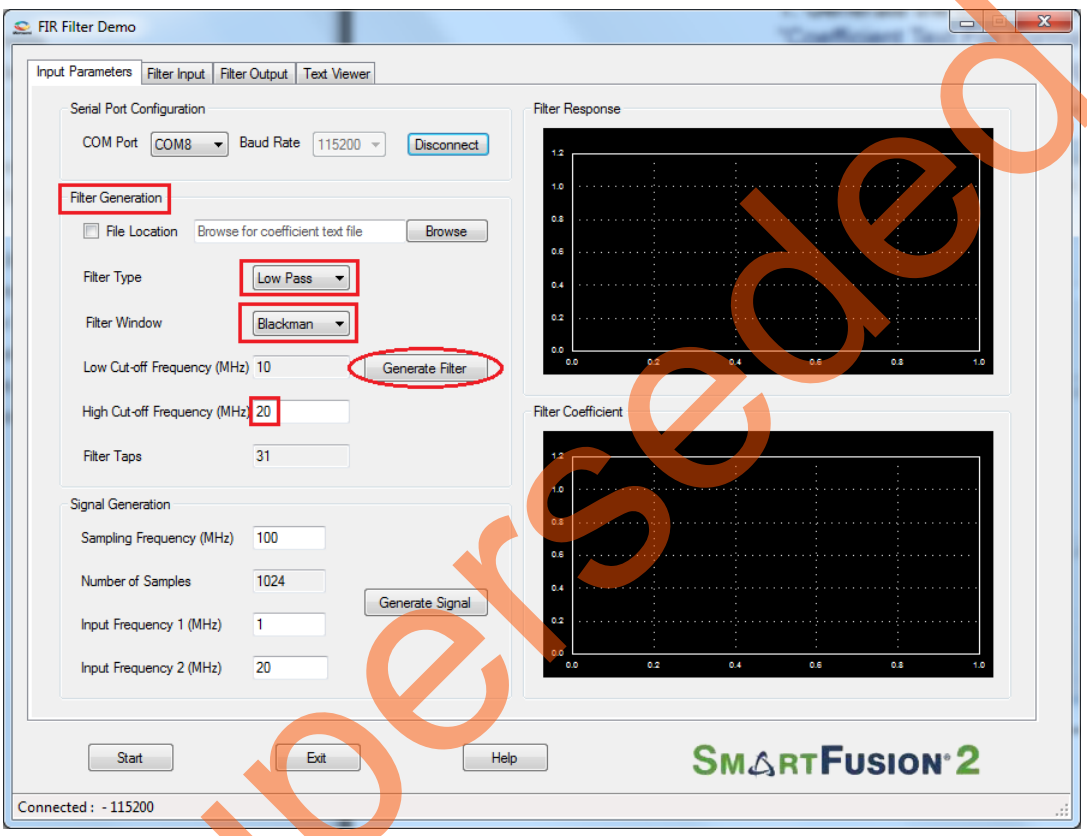

***Figure 15* • Filter Generation - 2**

The successful after-generation graphs of the filter coefficients, filter response, and the filter coefficient plots, are displayed. Refer to Figure 16.

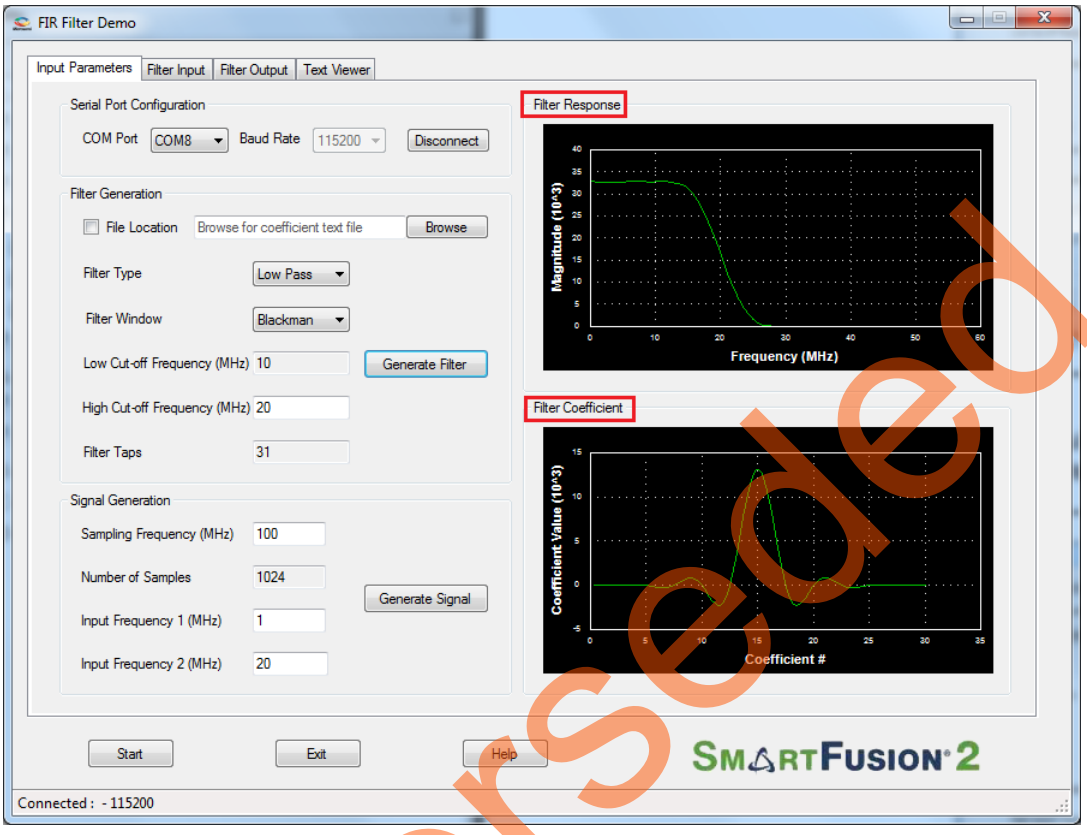

***Figure 16* • Filter Response and Filter Coefficient Plot**

4. **Signal Generation**:
   - **Sampling Frequency**: 100 MHz (Fixed)
   - **Number of Samples**: 1024 (Fixed)
   - **Input Frequency 1**: Enter the signal frequency in the Pass-band region. For example, 1 MHz to High cut-off frequency.
   - **Input Frequency 2**: Enter the signal frequency in the Stop-band region. For example, High cut-off frequency to Sampling frequency/2.

   Click **Generate Signal**, as shown in Figure 17.

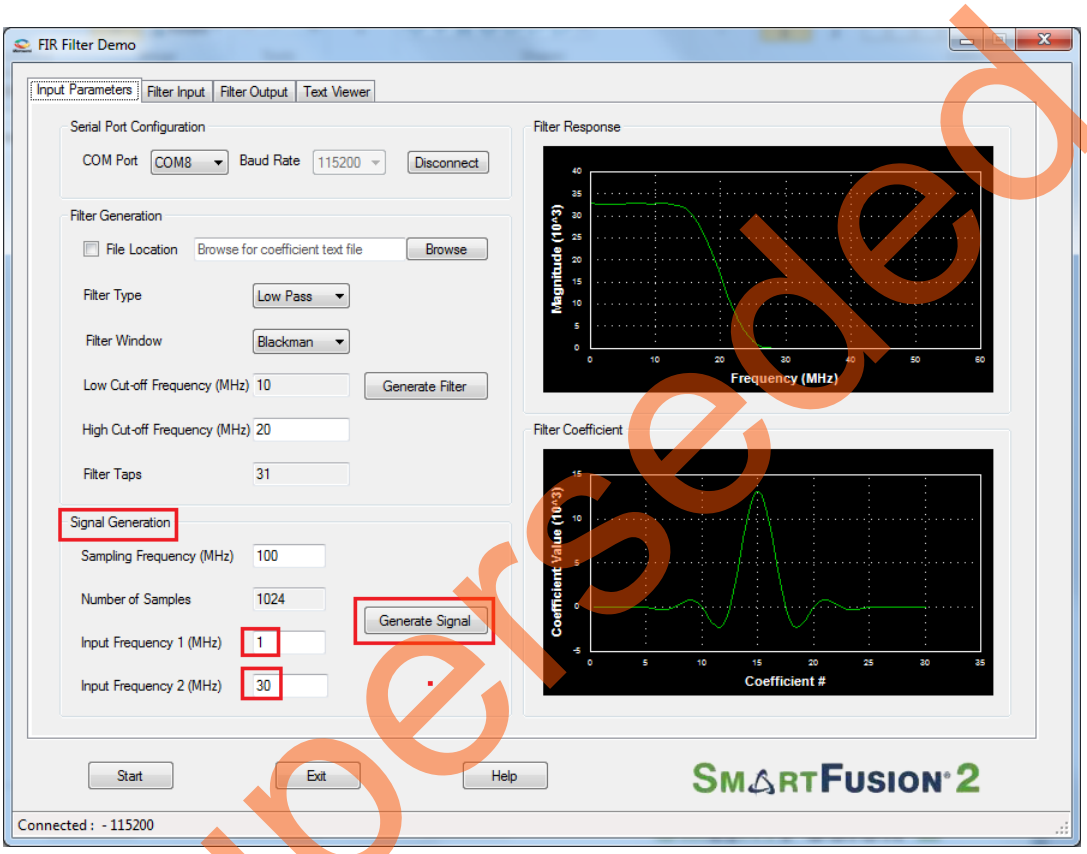

***Figure 17* • Signal Generation**

Input signal and the frequency spectrum of the specified signal are displayed as shown in Figure 18.

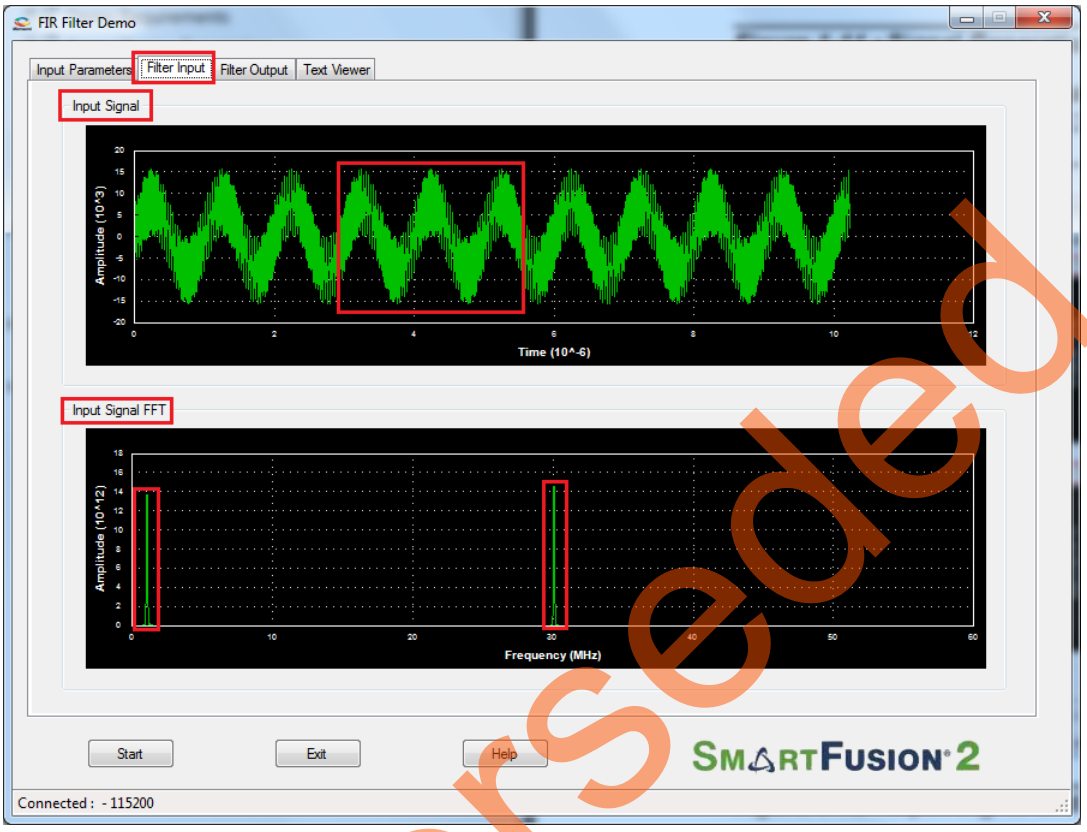

***Figure 18* • Input Signal and Input Signal FFT Plot**

5. To configure the input frequencies and coefficients click **Start**. Refer to Figure 19. It sends the input data (1K samples) and filter coefficients to the SmartFusion2 device for processing the filtering operation.

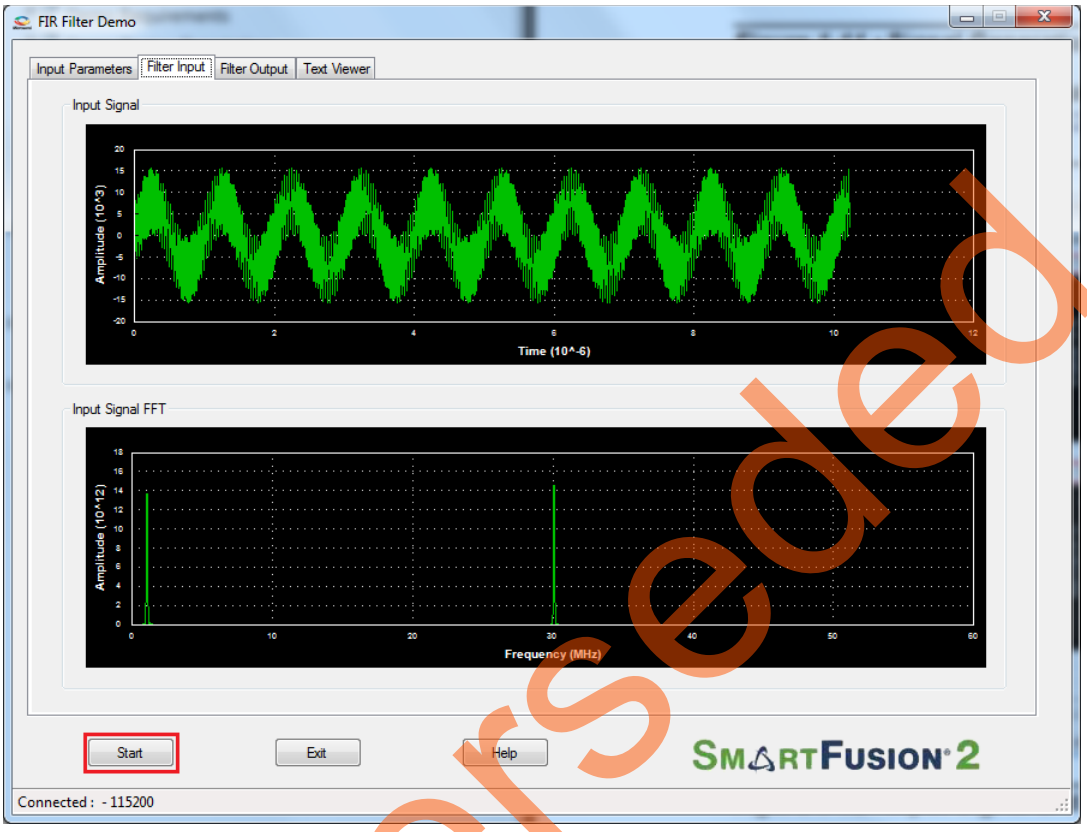

***Figure 19* • DSP FIR Filter Demo - Start**

After completing the filter operation by SmartFusion2, the GUI plots the filtered data and FFT data on filter output window, refer to Figure 20. Since Low-pass filter option was selected, the High frequency component is suppressed while the Low frequency signal is preserved. This can be observed in the frequency spectrum of the output signal.

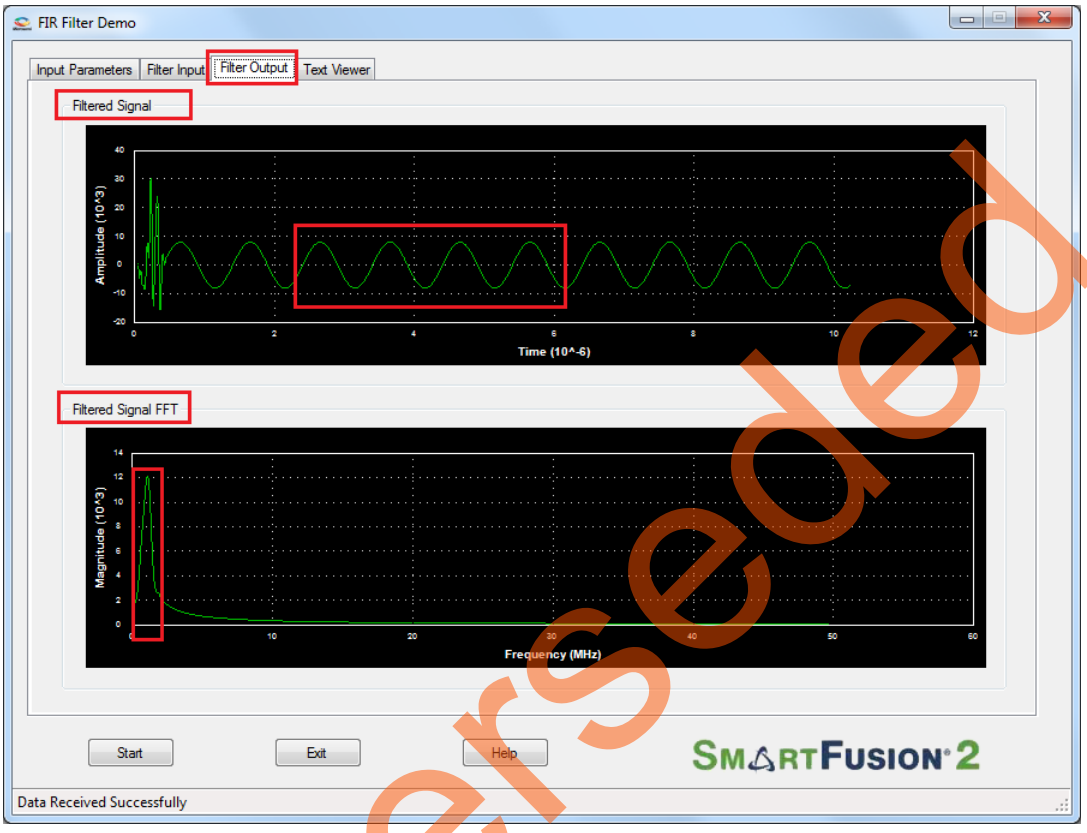

***Figure 20* • Filtered Signal: Time and Frequency Plot**

6. Right-click on the window, it shows different options. Refer to Figure 21. The data can be copied, saved, and exported to the CSV plot for analysis purpose. Page setup, print, show point values, zoom, and set scale are set to default.

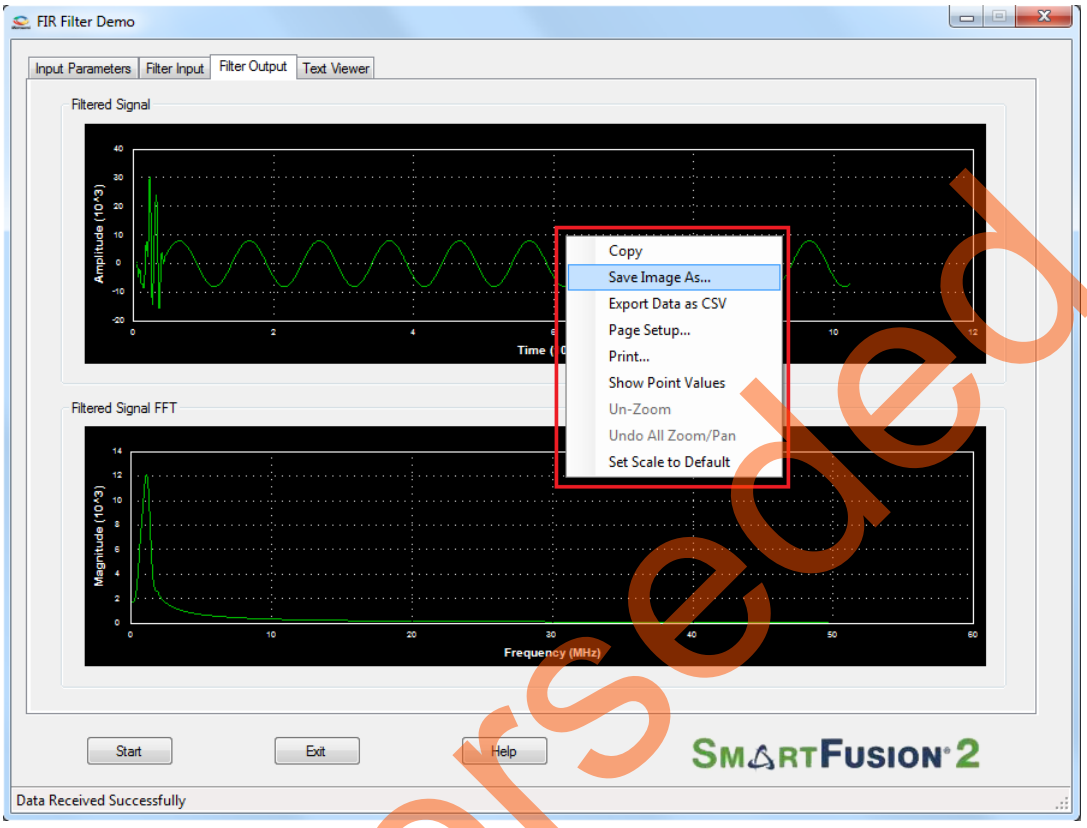

***Figure 21* • Filtered Signal: GUI options**

7. The filter coefficients, input signal, output signal, and FFT output data values can be viewed in **Text viewer**. Click the **Text Viewer** tab and then click the corresponding **View** button as shown in Figure 22.

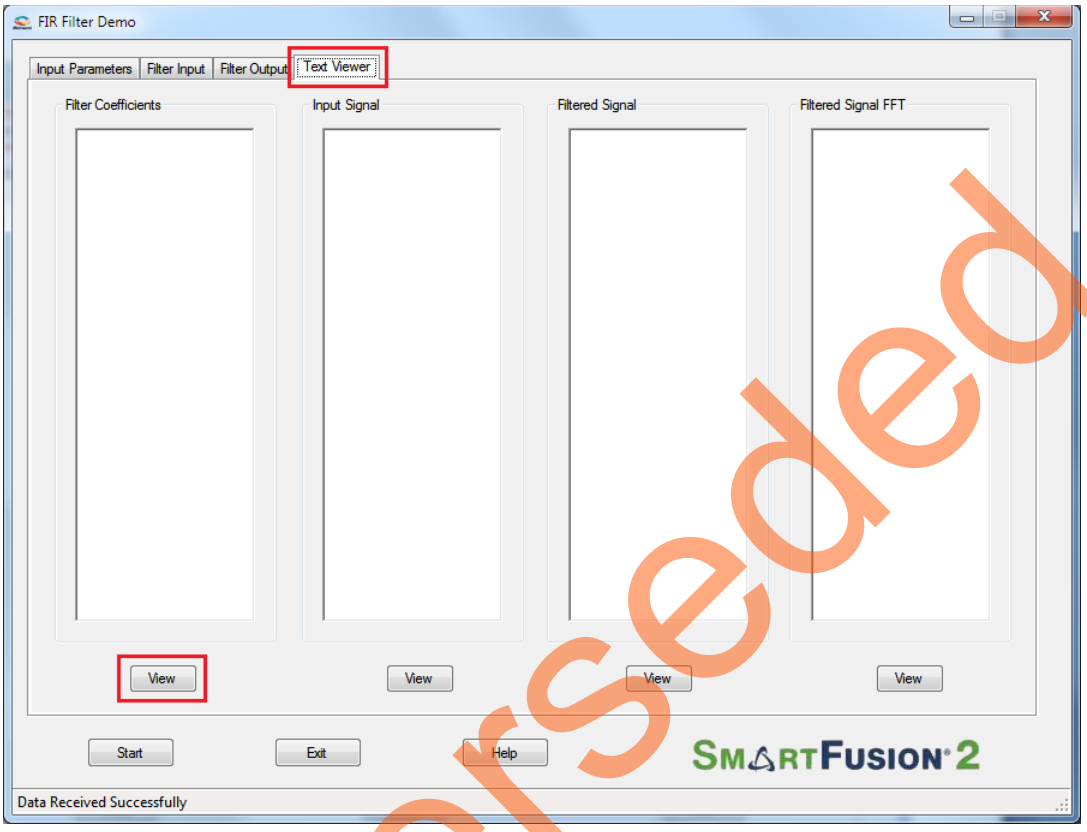

Figure 22 • **Text Viewer**

The values can be observed as shown in Figure 23.

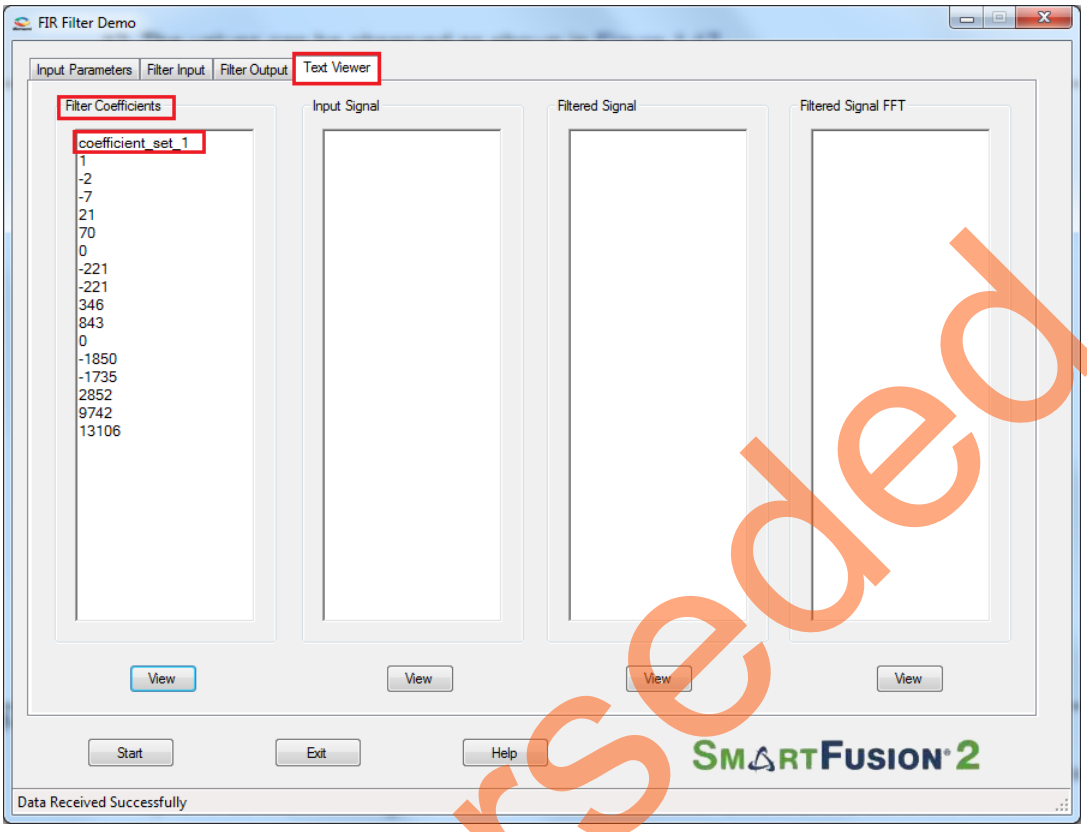

***Figure 23* • Text Viewer: Filter Coefficient Values**

8. To save the coefficients as a text file, right-click the **Filter Coefficients** window, it shows different options, as shown in Figure 24. Now click **Save**. Select **OK** to save the text file.

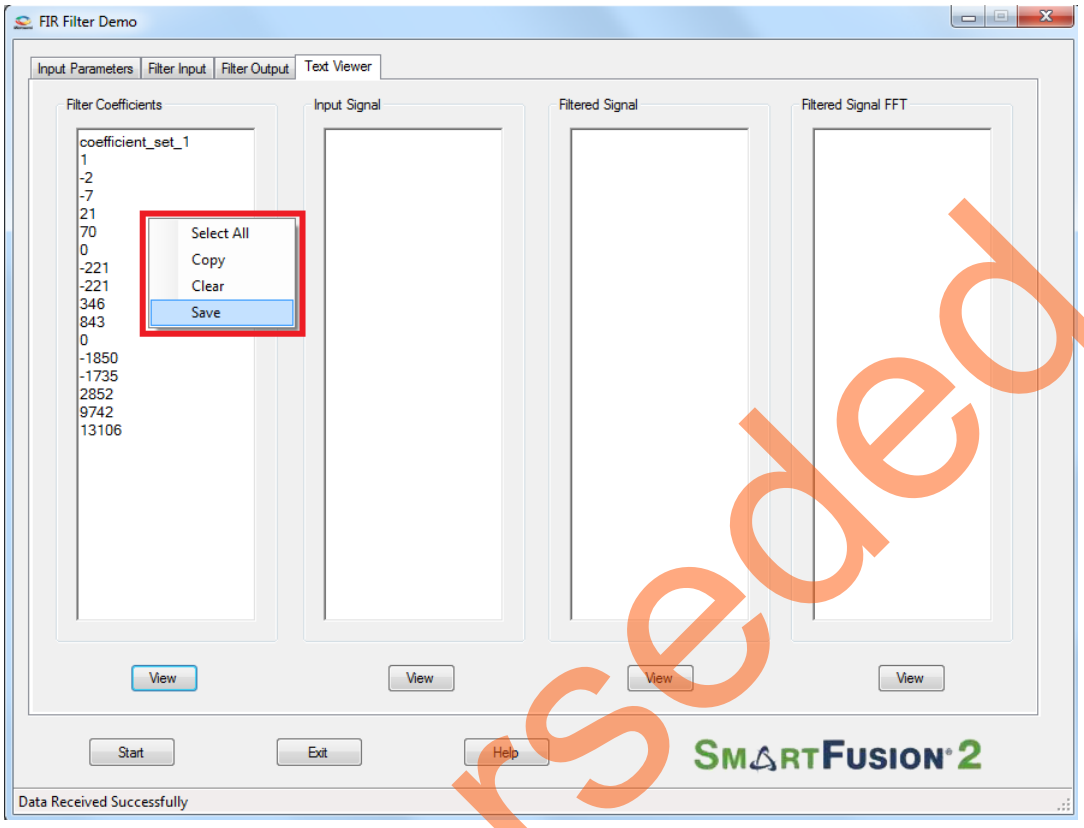

Figure 24 • **Text Viewer: Coefficients Save Options**

9. Click **Exit** to stop the demo. Refer to Figure 25.

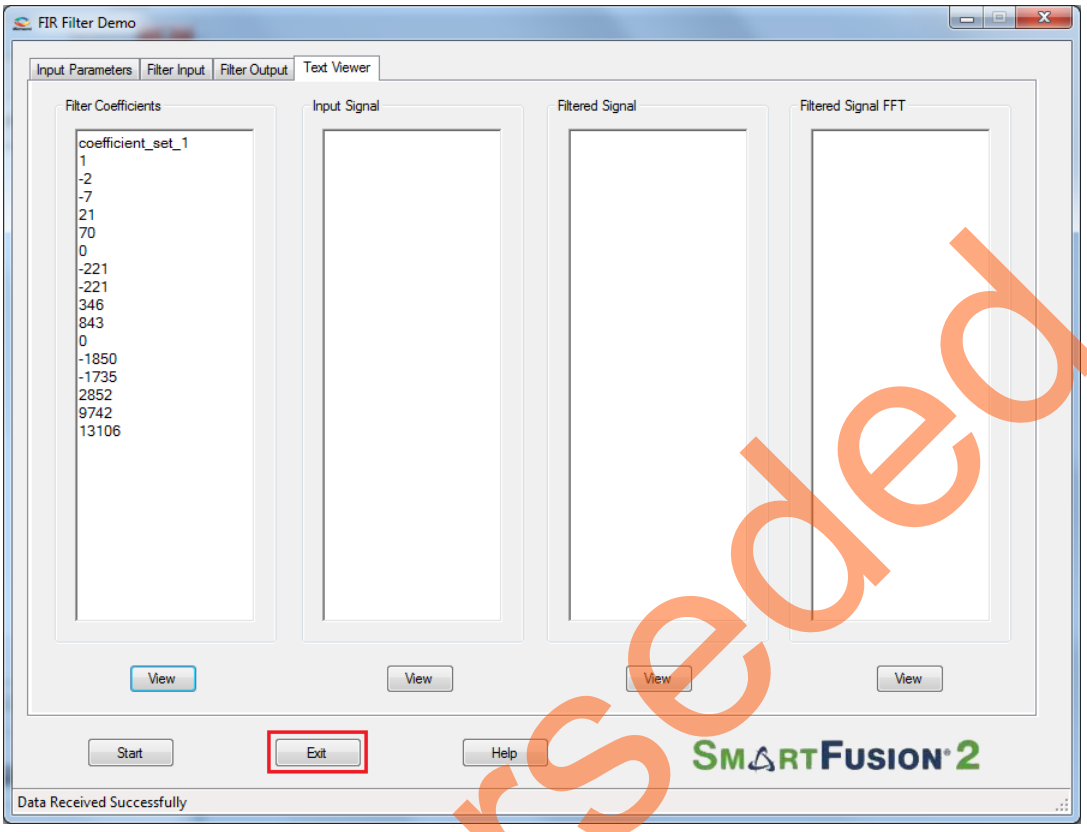

***Figure 25* • Exit Demo**

Conclusion

This demo shows the features of the SmartFusion2 device including MSS, mathblocks, and LSRAMS for DSP specific applications. Also provides information about how to use the Microsemi DSP IP cores (CoreFIR, CoreFFT). This GUI-based demo is easy to use and provides several options to understand and implement DSP filters on the SmartFusion2 device.

Appendix 1: Smart Design Implementation

DSP FIR filter SmartDesign is shown in Figure 1.

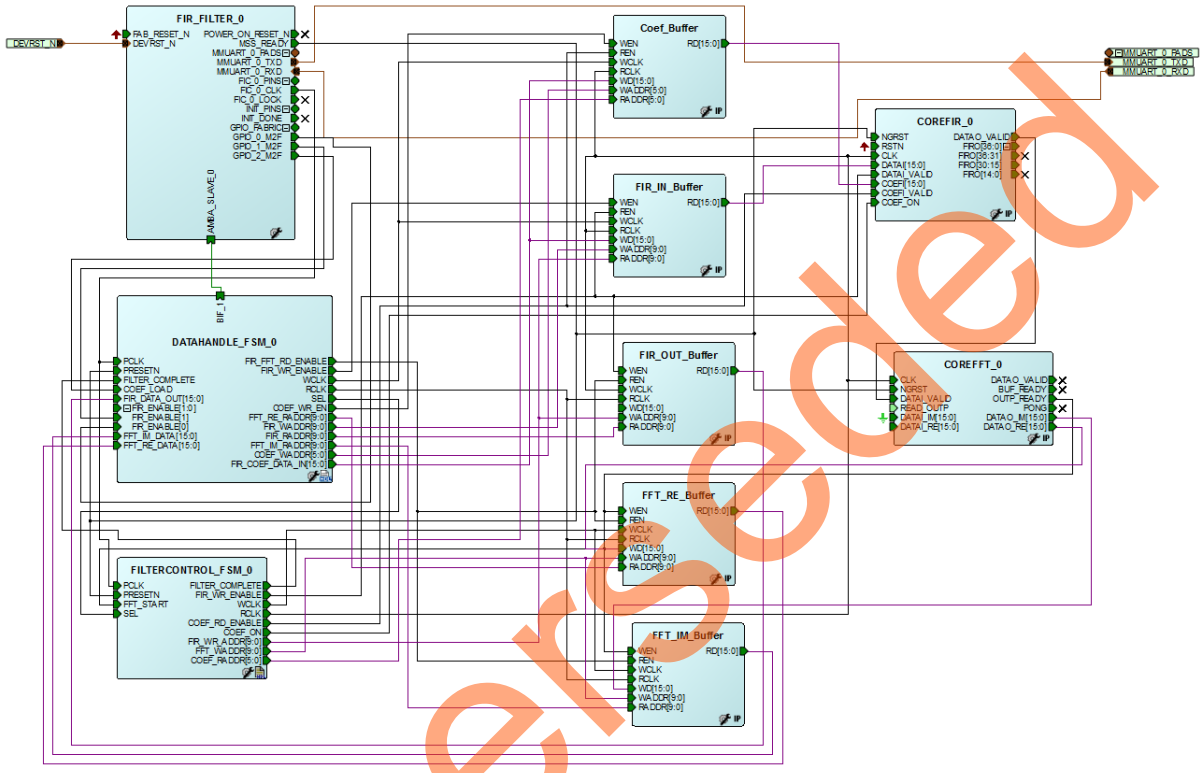

Figure 1 • **DSP FIR Filter Smart Design**

Table 1 shows SmartDesign blocks in DSP FIR Filter.

Table 1 • **DSP FIR Filter Demo Smart Design Blocks and Description**

S.No	Block Name	Description
1	FIR_FILTER_0	FIR_FILTER_0 is a System Builder generated component, in which MMUART is configured to handle the communication between the host PC and fabric logic. To generate a System Builder component, refer to the *SmartFusion2 System Builder User Guide*.
2	DATAHANDLE_FSM	Control logic to send/receive the data between MSS and data buffers.
3	FILTERCONTROL_FSM	Control logic to generate the control signals for FIR and FFT operations.
4	Coef_Buffer	TPSRAM IP for filter coefficient buffer
	FIR_IN_Buffer	TPSRAM IP for FIR input signal data buffer
	FIR_Out_Buffer	TPSRAM IP for FIR output signal buffer
	FFT_Im_Buffer	TPSRAM IP for FFT output imaginary data buffer
	FFT_Re_Buffer	TPSRAM IP for FFT output real data buffer

Table 1 • **DSP FIR Filter Demo Smart Design Blocks and Description (continued)**

S.No	Block Name	Description
5	COREFIR	COREFIR IP
6	COREFFT	COREFFT IP

Appendix 2: Resource Usage Summary

Table 1 shows DSP FIR filter resource usage summary.

Device: SmartFusion2 device

Die: M2S010

Package: 484 FBGA

Table 1 • **DSP FIR Filter Demo Resource Usage Summary**

Type	Used	Total	Percentage
4LUT	2653	12084	21.95
DFF	3575	12084	29.58
RAM64x18	0	22	0.00
RAM1Kx18	12	21	57.14
MACC	20	22	90.91

Table 2 shows DSP FIR filter resource usage summary.

Device: SmartFusion2 device

Die: M2S090TS

Package: 484 FBGA

Table 2 • **DSP FIR Filter Demo Resource Usage Summary**

Type	Used	Total	Percentage
4LUT	2649	86184	3.07
DFF	3374	86184	3.91
RAM64x18	0	112	0.00
RAM1K18	12	109	11.01
MACC	20	84	23.81

Table 3 shows MACC blocks usage summary.

Table 3 • **MACC Blocks Usage Summary**

CoreFIR	CoreFFT	Total
16	04	20

Table 4 shows RAM1Kx18 blocks usage summary.

Table 4 • **RAM1Kx18 Blocks Usage Summary**

CoreFIR	CoreFFT	Fabric Buffers	Total
0	7	5	12

Appendix 3: Coefficient Text File Format

The FIR filter coefficients can be loaded from an ASCII text file (*.txt). Create the coefficient file using a text editor. The format of text file should be as shown in Figure 1. Coefficient values must be entered as integer numbers. For a symmetric or anti-symmetric filter, only half of the coefficients must be listed in the file (applies to the Fully Enumerated type only). Only one coefficient value per line is permitted. An extra empty line must be placed after the last coefficient of the last set.

```
coefficient_set_1
5
6
10
25
63
- 1
- 11
- 32
- 63
```

***Figure 1* • Coefficient File Example - 9 Taps, Decimal Values**

A – List of Changes

The following table shows important changes made in this document for each revision.

Date	Changes	Page
Revision 5 (October 2015)	Updated the document for Libero v11.6 software release (SAR 71411)	NA
Revision 4 (January 2015)	Updated the document for Libero v11.5 software release (SAR 63931).	NA
Revision 3 (August 2014)	Updated the document for Libero v11.4 software release (SAR 60160).	NA
Revision 2 (July 2014)	Updated the document for Libero v11.3 software release (SAR 58923).	NA
	Updated the "Demo Design" section (SAR 58923).	6
	Updated the "Setting Up the Demo Design" section (SAR 58923).	10
Revision 1 (November 2013)	Updated the document for Libero v11.2 software release (SAR 52985).	NA
Revision 0 (April 2013)	Initial release	NA

B – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

For Microsemi SoC Products Support, visit
http://www.microsemi.com/products/fpga-soc/designsupport/fpga-soc-support

Website

You can browse a variety of technical and non-technical information on the SoC home page, at
http://www.microsemi.com/products/fpga-soc/fpga-and-soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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