Total Ionizing Dose

No. 16T-RTAX4000D-CQ352-D82W41

TR0027 Test Report

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com
www.microsemi.com

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Summary

The overall tolerance is limited by the standby power-supply current (ICC). The room temperature annealing allowed by TM1019 to anneal down ICC is performed for approximately seven days. Every deviec-under-test (DUT) passes the major specifications listed in the Table 1 for 200 krad (SiO_2) of irradiation.

Table 1 lists the tolerances of each tested parameters.

Table 1 • **Tolerances for Each Tested Parameter**

Parameter	Tolerance
Gross Functionality	Passed 300 krad (SiO_2)
Power Supply Current (ICCA/ICCI)	Passed 200 krad (SiO_2)
Input Threshold (VIL/VIH)	Passed 300 krad (SiO_2)
Output Drive (VOL/VOH)	Passed 300 krad (SiO_2)
Propagation Delay	Passed 200 krad (SiO_2) for 10% degradation criterion
Transition Time	Passed 300 krad (SiO_2)

Total Ionizing Dose (TID) Testing

This testing is designed on the basis of an extensive database (see, for example, TID data of antifuse-based FPGAs at *http://www.klabs.org* and *http://www.microsemi.com/soc*) accumulated from the TID testing of many generations of antifuse-based FPGAs.

Device-Under-Test and Irradiation Parameters

During irradiation, all inputs are grounded except for the inputs Burnin, oe_EAQ, enable_HSB, and the utilized clocks (Rclock1-3 and Hclock1-4). The inputs Burnin, oe_EAQ, and enable_HSB are set high to 3.3 V and a 1 KHz clock is provided to all clocks in order for the design to remain stable during irradiation. During anneal, each input and output is tied to ground or VCCI through a 4.7 kΩ resistor.

Table 2 lists the DUT and irradiation parameters.

Table 2 • **DUT and Irradiation Parameters**

Part Number	RTAX4000S
Package	CQFP352
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	MASTER_RTAX4000D_DESIGN_80_SP1
Die Lot Number	D82W41
Quantity Tested	6
Serial Number	300 krad: 1190, 1194, 1198, 1200 200 krad: 1197, 1216
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad (SiO_2)/min
Irradiation Temperature	Room

Table 2 • **DUT and Irradiation Parameters (continued)**

Part Number	RTAX4000S
Irradiation and Measurement Bias	Static at 3.3 V / 1.5 V
I/O Configuration	Single ended: LVTTL Differential pair: LVPECL

Test Method

The test method generally follows the guidelines in the military standard TM1019.

The accelerated aging, or rebound test mentioned in TM1019, is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by sub- micron CMOS technology. Elevated temperature annealing actually reduces the effects originated from radiation-induced leakages. As indicated by testing data in the following sections, the predominant radiation effects in RTAX4000D are due to radiation-induced leakages.

Room temperature annealing is performed in this test; the duration is approximately seven days.

Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

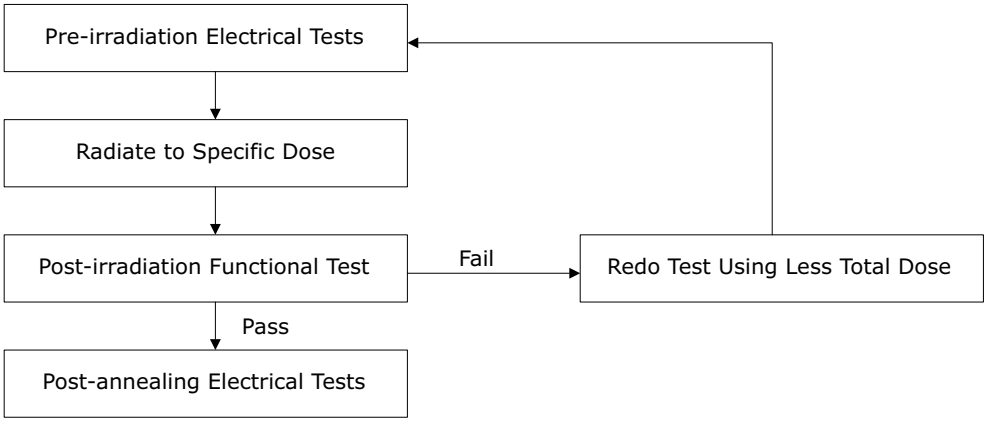

Figure 1 • **Parametric Test Flow Chart**

Design and Parametric Measurements

The DUT uses a high utilization generic design (RTAX4000D_CQ352_MASTER) to evaluate total dose effects for typical space applications.

The functionality is measured at 1 MHz and 50 MHz using the minimum and maximum power specifications shown in Table 3.

Table 3 • **Minimum and Maximum Power Specifications for RTAX-S Devices**

Supply Voltage	Minimum	Recommended	Maximum
1.5 V Core	1.4 V	1.5 V	1.6 V
3.3 V I/O	3.0 V	3.3 V	3.6 V
3.3 V VCCDA I/O	3.0 V	3.3 V	3.6 V

The functionality test design is subdivided into two blocks, the enhanced anti-fuse qualification (EAQ) and the qualification burn-in (QBI). The EAQ block includes three 1458-bit shift registers and tests the I/Os (1560 I/O registers and 520 I/Os) and RAM (1x16384 RAM). The QBI block tests all offered macros and I/O standards. The results from the functional tests are obtained from the following outputs: IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI.

ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic threshold (VIL/VIH) is tested on single-ended inputs Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, and A_Pattern_Length_0. The output-drive voltage (VOL/VOH) is measured on single-ended outputs Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, and RAM_out_EAQ_8.

The propagation delays are measured on the outputs of five delay strings; each one comprises of 1,170 NAND4-inverters. There are six delay measurements: one measurement for each delay string and a total delay measurement obtained from cascading all the delay strings. The propagation delay is defined as the time delay from the triggering edge at the HClock1 input to the switching edge at the output. The delay measurements are taken for both rising and falling edges, the average reading of the two measurements is reported. The transition characteristics, measured on the output delay_out_SEU4, are shown as oscilloscope captures.

Table 4 lists the measured electrical parameters and the corresponding logic design.

Table 4 • **Logic Design for Parametric Measurements**

Parameters	**Logic Design**
Functionality	IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and
ICC (ICCA/ICCI)	DUT power supply
Input Threshold (VIL/VIH)	Single ended inputs (Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1,
Output Drive (VOL/VOH)	Single-ended outputs (Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ,
Propagation Delay	String of NAND4-inverters. Measured from output delay_out_SEU4
Transition Characteristic	NAND4-inverter output (delay_out_SEU4)

Test Results

The test results mainly compare the electrical parameter measured pre-irradiation with the same parameter measured post-irradiation-and-annealing, or post-annealing.

Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests.

Power Supply Current (ICCA and ICCI)

The logic-array power supply (VCCA) is 1.5 V, and the I/O power supply (VCCI) is 3.3 V. Their standby currents, ICCA and ICCI, are monitored influx. Figure 2 to Figure 7 on page 8 show the influx ICCA and ICCI versus total dose for the DUTs.

Referring to TM1019 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICC, should be defined as the addition of highest ICCI, ICCDA, and ICCDIFFA values in table 2-6 of the RTAX-S/SL and RTAX-DSP Radiation-Tolerant FPGAs datasheet posted on the Microsemi website: *RTAX-S/SL and RTAX-DSP Radiation-Tolerant FPGAs Datasheet*

Therefore, the PIPL for ICCA is 600 mA, and the PIPL for ICCI is 83.7 mA.

Table 5 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 5 • **Pre-irradiation, Post Irradiation and Post-Annealing ICC**

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-Irrad	Post-Irrad	Post-Ann	Pre-Irrad	Post-Irrad	Post-Ann
1190	300 krad	14	216.08	27	16	304.97	66
1194	300 krad	16	203.68	25	21	273.69	71
1198	300 krad	21	166.73	30	19	267.75	76
1200	300 krad	15	169.26	32	21	296.51	75
1197	200 krad	26	34.58	25	22	138.09	33
1216	200 krad	15	23.68	15	21	132.6	30

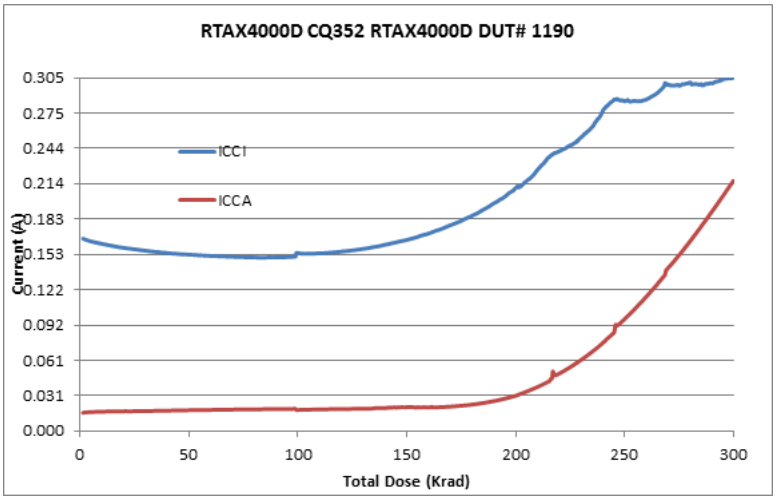

Figure 2 • **DUT 1190 Influx ICCI and ICCA**

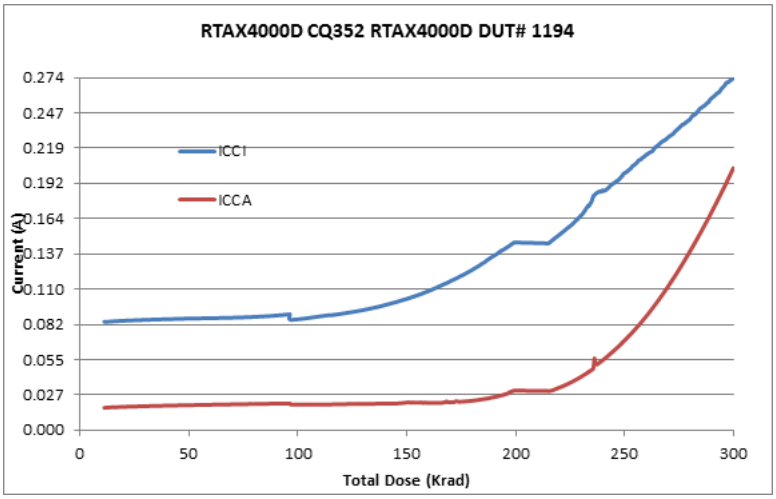

***Figure 3* • DUT 1194 Influx ICCI and ICCA**

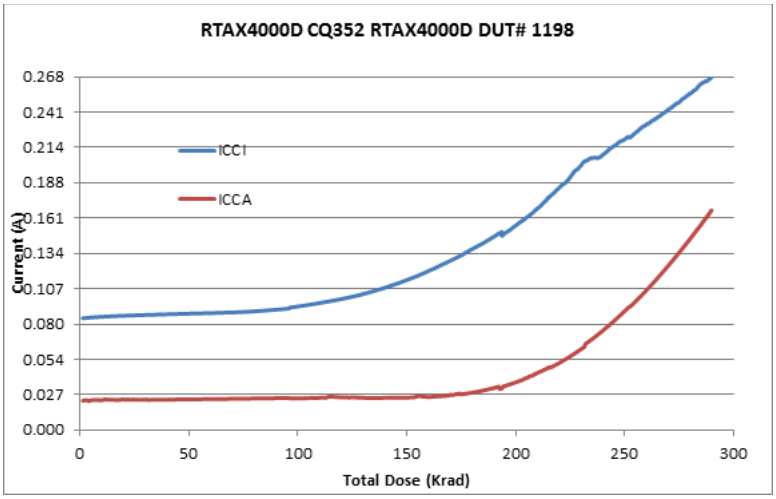

***Figure 4* • DUT 1198 Influx ICCI and ICCA**

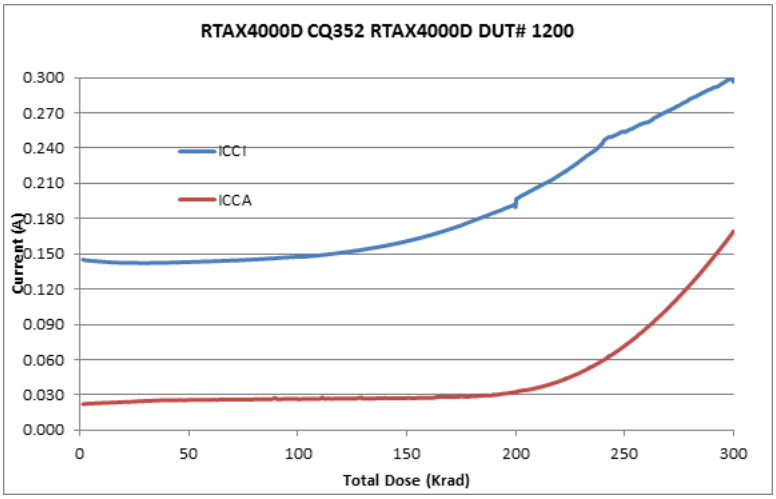

***Figure 5* • DUT 1200 Influx ICCI and ICCA**

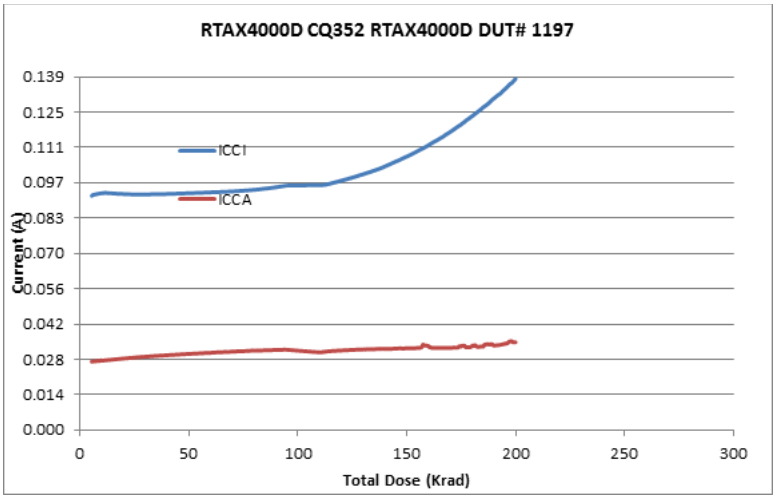

***Figure 6* • DUT 1197 Influx ICCI and ICCA**

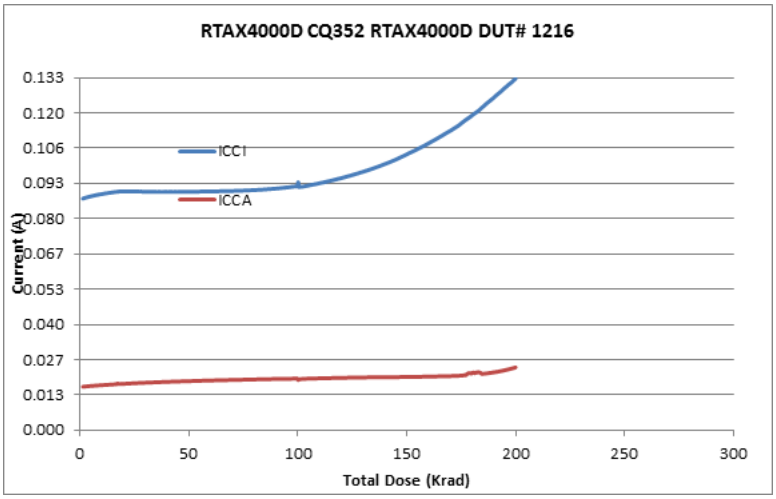

***Figure 7* • DUT 1216 Influx ICCI and ICCA**

Single-Ended 3.3 V LVTTL Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design, often just input and output buffers, starts to switch: VIH is the input trip point when the input is going high to low; VIL is the input trip point when the input is going low to high. The difference between the pre-irradiation and post-annealing data is usually negligibly small.

The pre-irradiation and post-annealing VIL/VIH are listed in Table 6, Table 7 on page 9, Table 8 on page 9, and Table 9 on page 9. The post-annealing data are within the specification limits; in each case, the radiation-induced degradation is small.

***Table 6* • Pre-Irradiation and Post-Annealing Input Thresholds (VIL)**

	1190 (300 krad)		1194 (300 krad)		1198 (200 krad)	
Pin \ DUT (Dose)	**Pre-Rad**	**Pos-Ann**	**Pre-Rad**	**Pos-Ann**	**Pre-Rad**	**Pos-Ann**
SEU_sel	1.3650	1.3400	1.3700	1.3450	1.3600	1.3350
zoom_sel_n_0	1.3700	1.3450	1.3700	1.3450	1.3650	1.3450
zoom_sel_n_1	1.3650	1.3450	1.3650	1.3450	1.3650	1.3400
zoom	1.3600	1.3400	1.3650	1.3400	1.3600	1.3350
TOG_n	1.3800	1.3700	1.3750	1.3650	1.3700	1.3600
Set_n	1.3600	1.3550	1.3600	1.3450	1.3600	1.3450
Resetn	1.3700	1.3600	1.3650	1.3550	1.3700	1.3600
oe_EAQ	1.3800	1.3600	1.3750	1.3700	1.3750	1.3650
enable_HSB	1.3650	1.3550	1.3650	1.3450	1.3700	1.3450
IO_Pattern_Length_1	1.3700	1.3650	1.3750	1.3650	1.3750	1.3650

Table 7 • **Pre-Irradiation and Post-Annealing Input Thresholds (VIL)**

	1200 (300 krad)		1197 (200 krad)		1216 (200 krad)	
Pin \ DUT (Dose)	**Pre-Rad**	**Pos-Ann**	**Pre-Rad**	**Pos-Ann**	**Pre-Rad**	**Pos-Ann**
SEU_sel	1.3650	1.3450	1.3650	1.3450	1.3600	1.3450
zoom_sel_n_0	1.3700	1.3450	1.3700	1.3500	1.3700	1.3500
zoom_sel_n_1	1.3650	1.3450	1.3600	1.3450	1.3600	1.3450
zoom	1.3600	1.3400	1.3600	1.3450	1.3550	1.3400
TOG_n	1.3750	1.3650	1.3800	1.3700	1.3700	1.3600
Set_n	1.3650	1.3550	1.3650	1.3550	1.3600	1.3450
Resetn	1.3650	1.3600	1.3700	1.3600	1.3650	1.3600
oe_EAQ	1.3750	1.3550	1.3800	1.3700	1.3750	1.3650
enable_HSB	1.3700	1.3600	1.3700	1.3500	1.3600	1.3450
IO_Pattern_Length_1	1.3750	1.3700	1.3750	1.3650	1.3750	1.3650

Table 8 • **Pre-Irradiation and Post-Annealing Input Thresholds (VIH)**

	1190 (300 krad)		1194 (300 krad)		1198 (200 krad)	
Pin \ DUT (Dose)	**Pre-Rad**	**Pos-Ann**	**Pre-Rad**	**Pos-Ann**	**Pre-Rad**	**Pos-Ann**
SEU_sel	1.6550	1.6250	1.6550	1.6300	1.6500	1.6200
zoom_sel_n_0	1.6500	1.6200	1.6500	1.6200	1.6450	1.6150
zoom_sel_n_1	1.6550	1.6300	1.6550	1.6300	1.6550	1.6250
zoom	1.6550	1.6300	1.6550	1.6300	1.6500	1.6250
TOG_n	1.6700	1.6600	1.6650	1.6550	1.6600	1.6500
Set_n	1.6550	1.6450	1.6500	1.6350	1.6500	1.6350
Resetn	1.6500	1.6350	1.6450	1.6350	1.6450	1.6350
oe_EAQ	1.6550	1.6300	1.6550	1.6400	1.6500	1.6400
enable_HSB	1.6550	1.6450	1.6600	1.6350	1.6600	1.6350
IO_Pattern_Length_1	1.6650	1.6550	1.6700	1.6550	1.6650	1.6550

Table 9 • **Pre-Irradiation and Post-Annealing Input Thresholds (VIH)**

	1200 (300 krad)		1197 (200 krad)		1216 (200 krad)	
Pin \ DUT (Dose)	**Pre-Rad**	**Pos-Ann**	**Pre-Rad**	**Pos-Ann**	**Pre-Rad**	**Pos-Ann**
SEU_sel	1.6550	1.6300	1.6550	1.6300	1.6500	1.6300
zoom_sel_n_0	1.6450	1.6150	1.6450	1.6250	1.6450	1.6250
zoom_sel_n_1	1.6600	1.6300	1.6500	1.6300	1.6550	1.6300
zoom	1.6550	1.6300	1.6500	1.6300	1.6500	1.6300
TOG_n	1.6650	1.6550	1.6650	1.6600	1.6600	1.6500
Set_n	1.6600	1.6450	1.6550	1.6450	1.6500	1.6350
Resetn	1.6450	1.6350	1.6450	1.6400	1.6450	1.6350
oe_EAQ	1.6550	1.6300	1.6550	1.6450	1.6500	1.6400
enable_HSB	1.6600	1.6500	1.6600	1.6400	1.6500	1.6300
IO_Pattern_Length_1	1.6700	1.6600	1.6650	1.6550	1.6650	1.6550

Output-Drive Voltage (VOL/VOH)

The post-annealing data are within the specification limits; in each case, the radiation-induced degradation is small.

Table 10 to Table 13 on page 11 list the pre-irradiation and post-annealing VOL/VOH.

***Table 10* • Pre-Irradiation and Post-Annealing VOL (mV)**

Pin \ DUT (Dose)	1190 (300 krad)		1194 (300 krad)		1198 (200 krad)	
	Pre-Rad	Pos-Ann	Pre-Rad	Pos-Ann	Pre-Rad	Pos-Ann
Shiftout_0	190.9020	183.7059	191.0391	189.5289	188.4581	187.0693
Shiftout_5	179.0639	178.5171	179.8457	166.4649	178.4395	181.8763
Array_out_EAQ_0	169.0791	162.8216	168.4364	160.6081	167.1068	160.6315
Array_out_EAQ_2	191.5880	182.5250	187.3335	173.5707	185.6927	179.6342
delay_out_SEU_1	13.2093	13.0530	13.3655	12.8906	13.0531	12.9749
delay_out_SEU_4	12.9622	12.8060	13.0615	13.1797	13.1397	13.0403
RAM_Monitor_EAQ	17.1154	16.4123	17.8967	16.3277	17.5842	17.0373
RAM_out_EAQ_0	17.5698	16.8659	17.8042	16.8639	17.6477	17.4916
RAM_out_EAQ_4	17.2716	16.0998	17.3498	16.7183	17.3498	16.8029
RAM_out_EAQ_8	17.2716	17.3498	17.8967	16.2496	17.2717	16.7248

***Table 11* • Pre-Irradiation and Post-Annealing VOL (mV)**

Pin \ DUT (Dose)	1200 (300 krad)		1197 (200 krad)		1216 (200 krad)	
	Pre-Rad	Pos-Ann	Pre-Rad	Pos-Ann	Pre-Rad	Pos-Ann
Shiftout_0	188.3208	179.9514	187.1286	192.3428	188.4581	193.8279
Shiftout_5	178.5171	178.2827	178.3614	166.8555	176.8770	165.9181
Array_out_EAQ_0	168.4533	162.5087	165.8555	160.5299	166.5594	160.9208
Array_out_EAQ_2	191.5880	181.4312	188.1148	175.9941	185.3802	173.4925
delay_out_SEU_1	12.8968	12.8968	13.1312	12.6563	13.0531	12.5782
delay_out_SEU_4	12.6497	13.0403	12.9834	12.7106	12.9834	13.0233
RAM_Monitor_EAQ	17.5841	16.5685	17.7404	16.4839	17.1936	16.4058
RAM_out_EAQ_0	17.7263	17.2570	17.3349	17.0984	17.2567	16.8639
RAM_out_EAQ_4	17.2716	16.4123	17.4279	16.6401	17.0373	16.3277
RAM_out_EAQ_8	17.3498	17.8185	17.3498	16.3277	17.2717	16.1715

***Table 12* • Pre-Irradiation and Post-Annealing VOH (V)**

Pin \ DUT (Dose)	1190 (300 krad)		1194 (300 krad)		1198 (200 krad)	
	Pre-Rad	Pos-Ann	Pre-Rad	Pos-Ann	Pre-Rad	Pos-Ann
Shiftout_0	2.7210	2.7161	2.7225	2.7112	2.7244	2.7106
Shiftout_5	2.7356	2.7231	2.7394	2.7373	2.7392	2.7198
Array_out_EAQ_0	2.7455	2.7389	2.7490	2.7431	2.7498	2.7405
Array_out_EAQ_2	2.7184	2.7152	2.7285	2.7284	2.7302	2.7202
delay_out_SEU_1	2.9595	2.9588	2.9631	2.9598	2.9629	2.9591
delay_out_SEU_4	2.9594	2.9587	2.9622	2.9606	2.9619	2.9588
RAM_Monitor_EAQ	2.9572	2.9549	2.9607	2.9556	2.9606	2.9551
RAM_out_EAQ_0	2.9567	2.9543	2.9591	2.9551	2.9589	2.9559

***Table 12* • Pre-Irradiation and Post-Annealing VOH (V) (continued)**

Pin \ DUT (Dose)	1190 (300 krad)		1194 (300 krad)		1198 (200 krad)	
	Pre-Rad	Pos-Ann	Pre-Rad	Pos-Ann	Pre-Rad	Pos-Ann
RAM_out_EAQ_4	2.9577	2.9552	2.9610	2.9559	2.9604	2.9551
RAM_out_EAQ_8	2.9573	2.9563	2.9606	2.9556	2.9608	2.9549

***Table 13* • Pre-Irradiation and Post-Annealing VOH (V)**

Pin \ DUT (Dose)	1200 (300 krad)		1197 (200 krad)		1216 (200 krad)	
	Pre-Rad	Pos-Ann	Pre-Rad	Pos-Ann	Pre-Rad	Pos-Ann
Shiftout_0	2.7213	2.7176	2.7258	2.7110	2.7235	2.7085
Shiftout_5	2.7359	2.7240	2.7392	2.7391	2.7406	2.7404
Array_out_EAQ_0	2.7457	2.7395	2.7501	2.7457	2.7495	2.7454
Array_out_EAQ_2	2.7215	2.7188	2.7276	2.7288	2.7295	2.7307
delay_out_SEU_1	2.9593	2.9589	2.9625	2.9603	2.9623	2.9601
delay_out_SEU_4	2.9591	2.9589	2.9618	2.9609	2.9620	2.9610
RAM_Monitor_EAQ	2.9574	2.9543	2.9606	2.9574	2.9609	2.9573
RAM_out_EAQ_0	2.9564	2.9564	2.9586	2.9577	2.9587	2.9569
RAM_out_EAQ_4	2.9576	2.9548	2.9605	2.9572	2.9604	2.9575
RAM_out_EAQ_8	2.9573	2.9562	2.9603	2.9574	2.9603	2.9570

Propagation Delay

The results show small radiation effects; in any case, the percentage change is well below 10%.

Table 14 lists the radiation-induced propagation delay degradations.

***Table 14* • Radiation-Induced Propagation Delay Degradations**

Delay (µs)							
	DUT	Total Dose (krad)	Pre-Rad	100 krad	200 krad	300 krad	Post-Ann
	1190	300	6.61	6.71	6.86	-	6.58
	1194	300	6.58	6.59	6.86	-	6.48
	1198	300	6.59	6.65	6.91	-	6.52
	1200	300	6.54	6.67	6.7	-	6.51
	1197	200	6.58	6.63	6.79	-	6.42
Radiation Δ (%)							
	DUT	**Total Dose (krad)**	**Pre-Rad**	**100 krad**	**200 krad**	**300 krad**	**Post-Ann**
	1190	300	-	1.52 %	3.79 %	-	-0.45 %
	1194	300	-	0.16 %	4.26 %	-	-1.51 %
	1198	300	-	0.92 %	4.86 %	-	-1.06 %
	1200	300	-	1.99 %	2.45 %	-	-0.45 %
	1197	200	-	0.76 %	3.2 %	-	-2.43 %

Transition Time

Figure 8 to Figure 33 on page 24 show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is not observable.

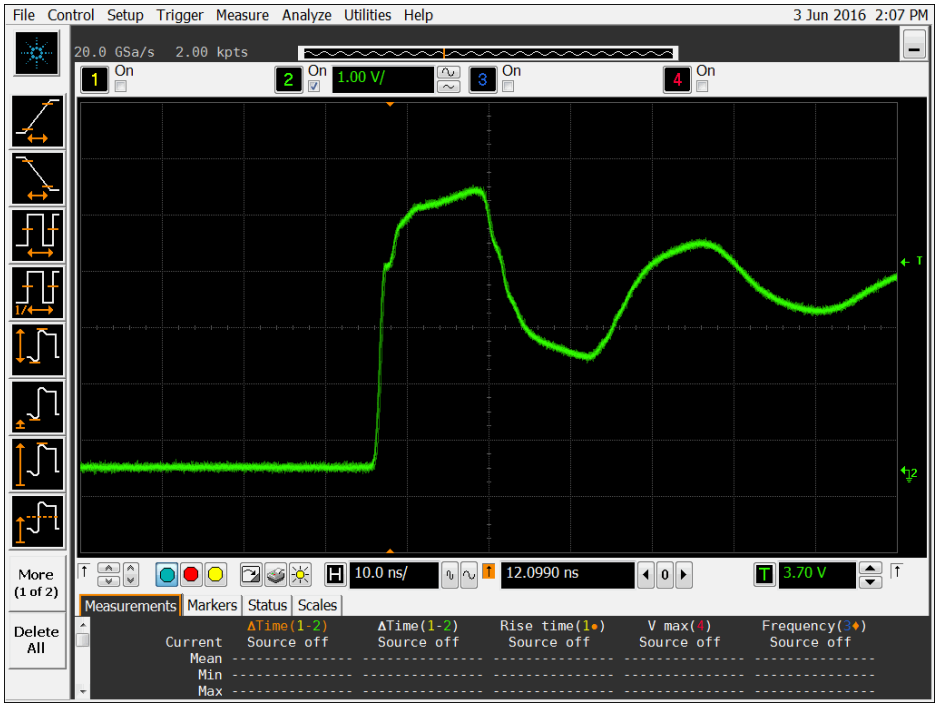

***Figure 8* • DUT 1190 Pre-Irradiation Rising Edge**

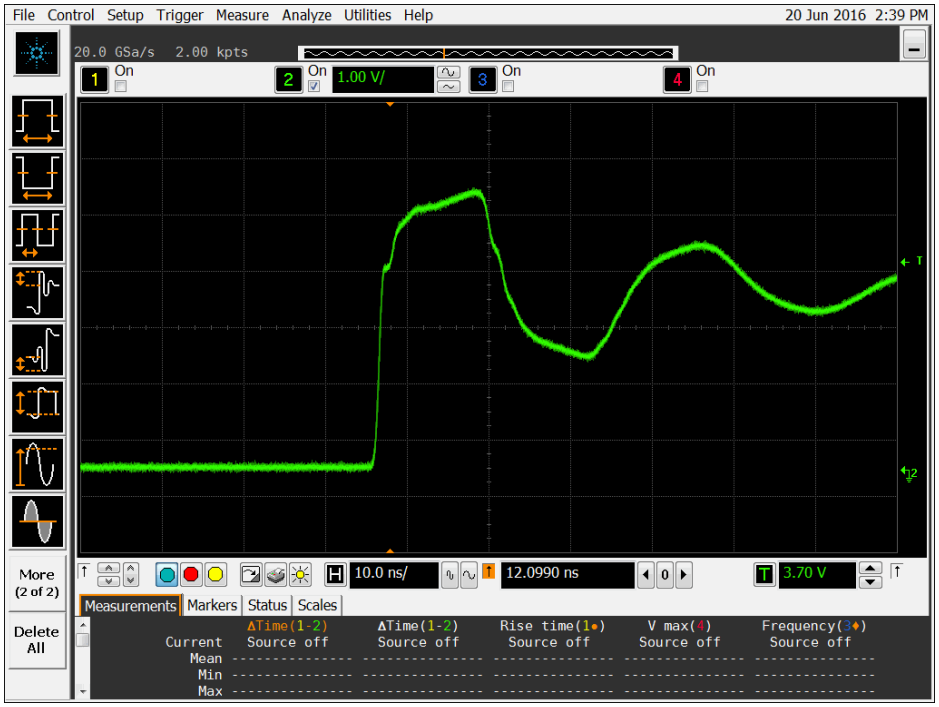

***Figure 9* • DUT 1190 Post-Annealing Rising Edge**

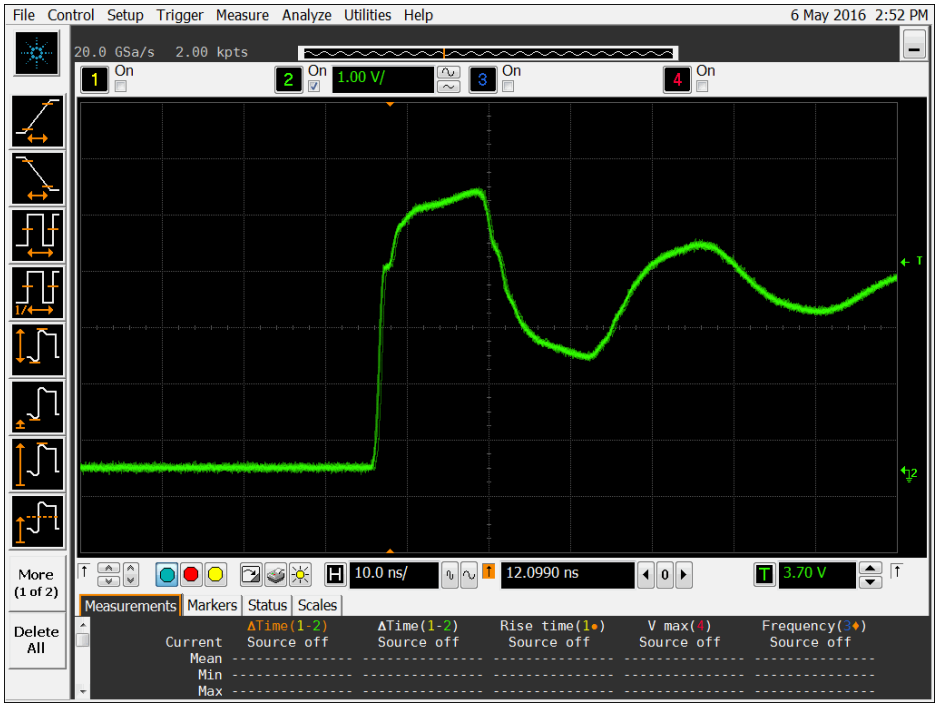

***Figure 10* • DUT 1194 Pre-irradiation Rising Edge**

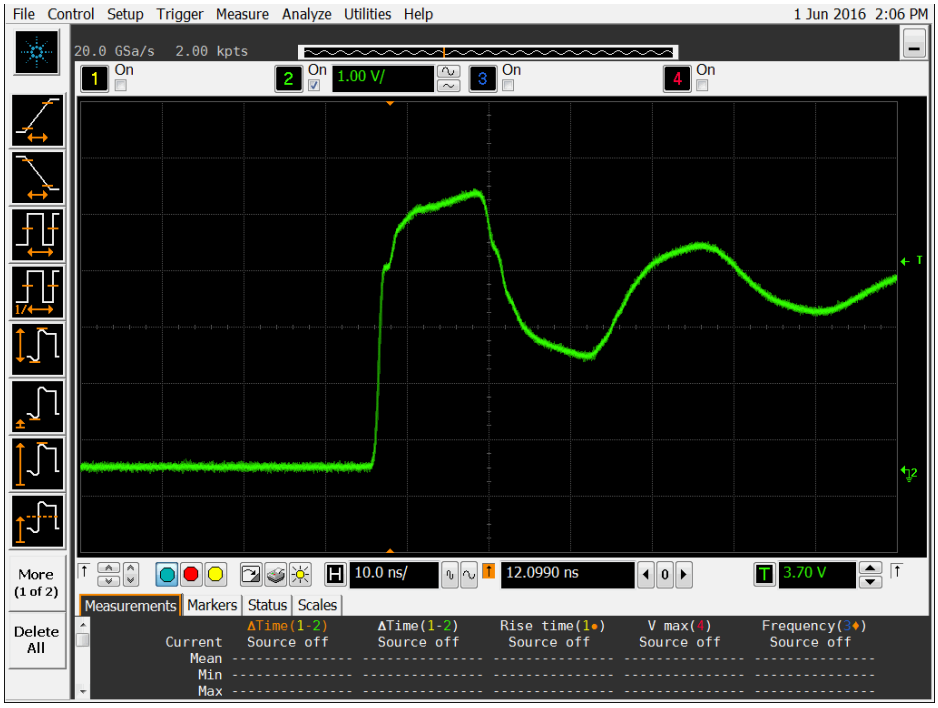

***Figure 11* • DUT 1194 Post-Annealing Rising Edge**

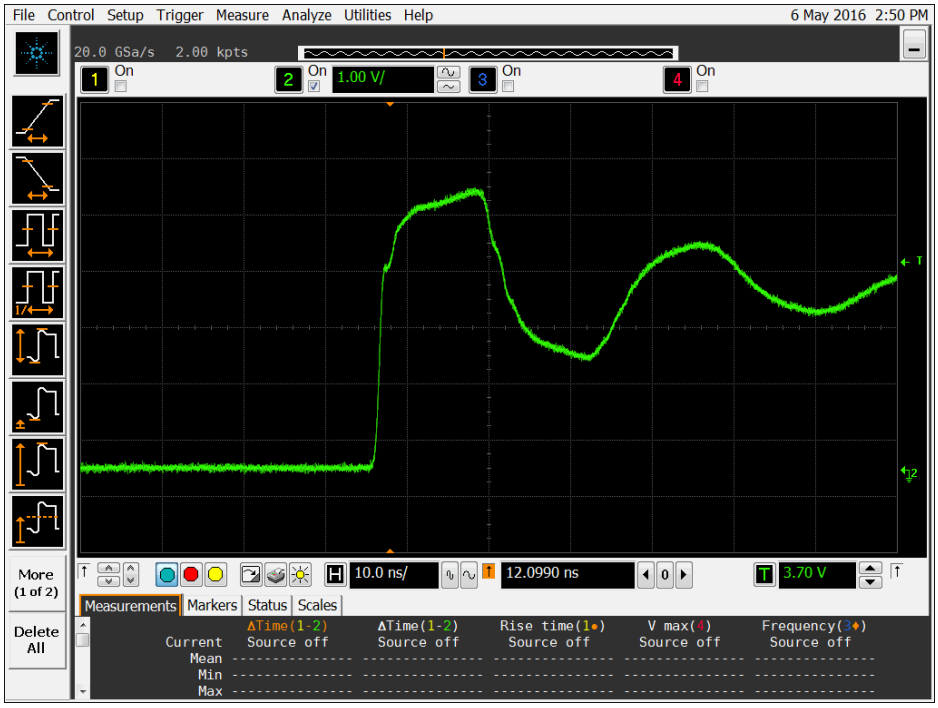

***Figure 12* • DUT 1198 Pre-Irradiation Rising Edge**

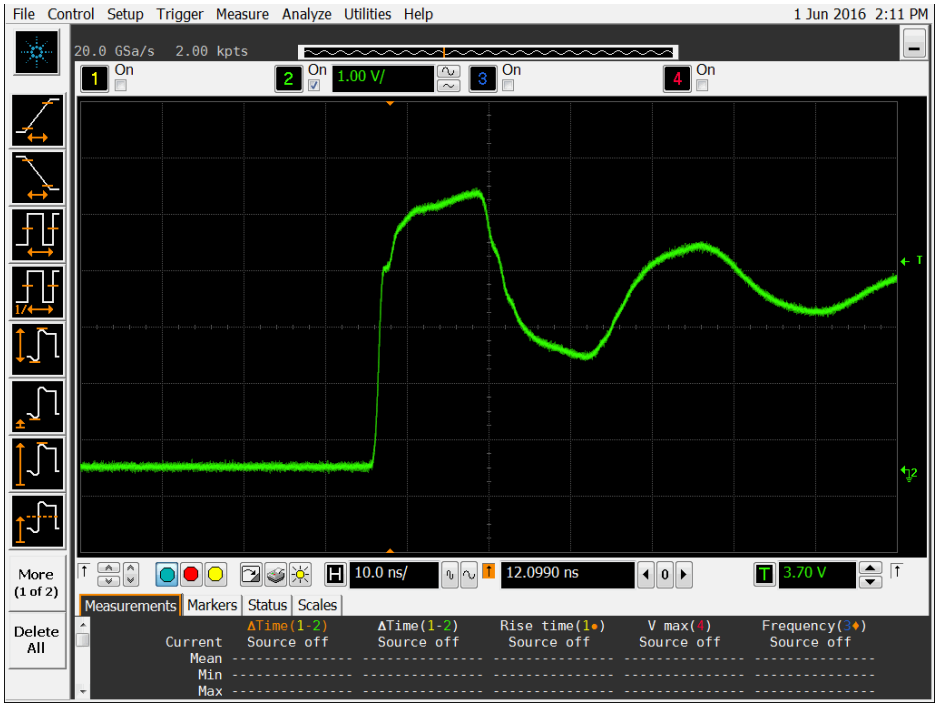

***Figure 13* • DUT 1198 Post-Annealing Rising Edge**

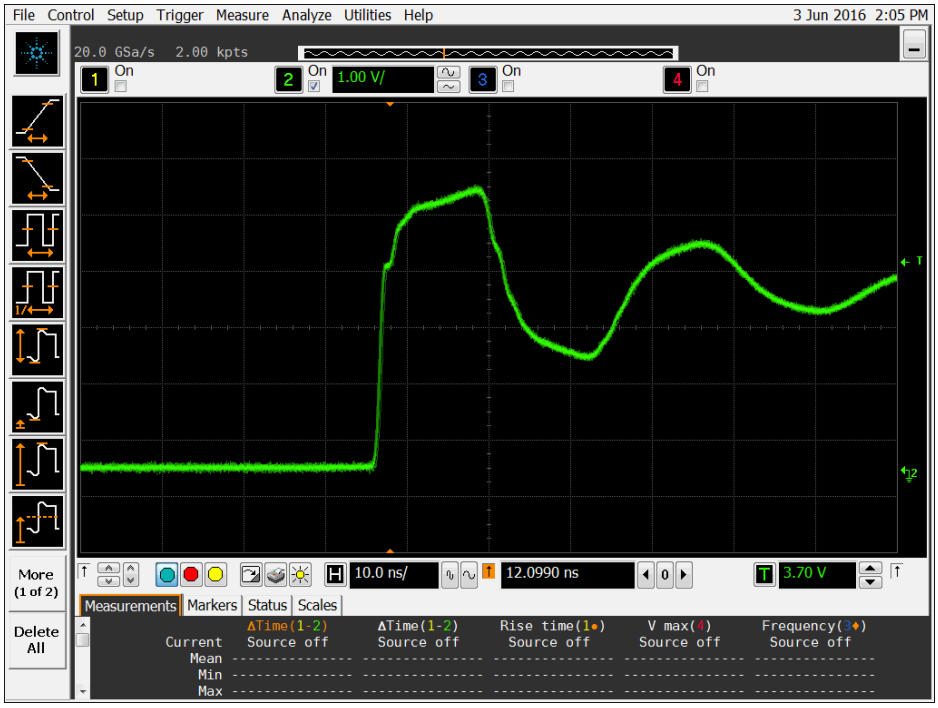

***Figure 14* • DUT 1200 Pre-Irradiation Rising Edge**

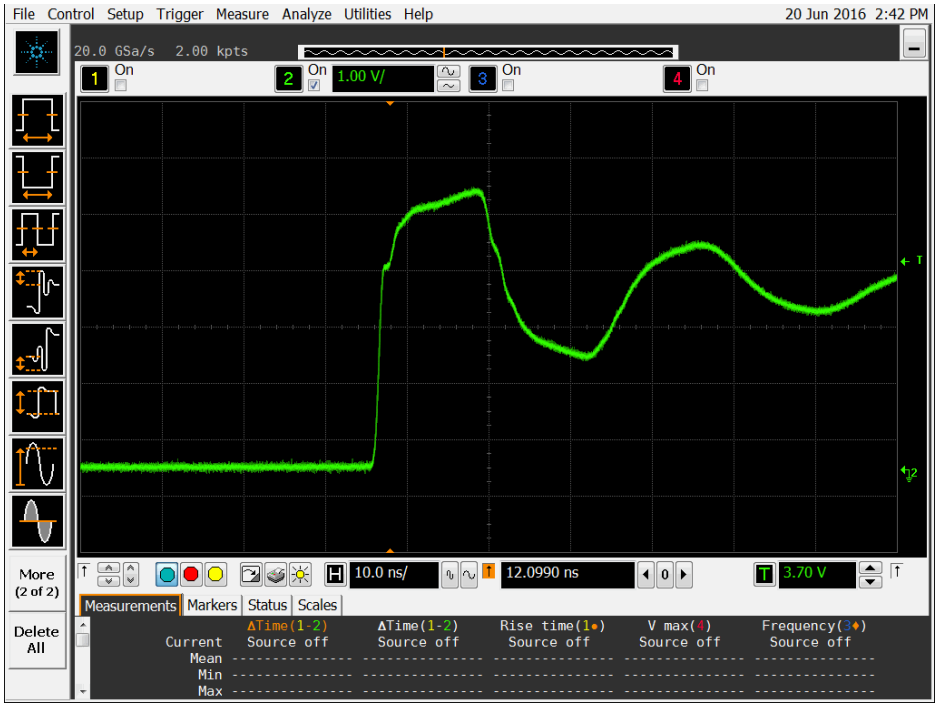

***Figure 15* • DUT 1200 Post-Annealing Rising Edge**

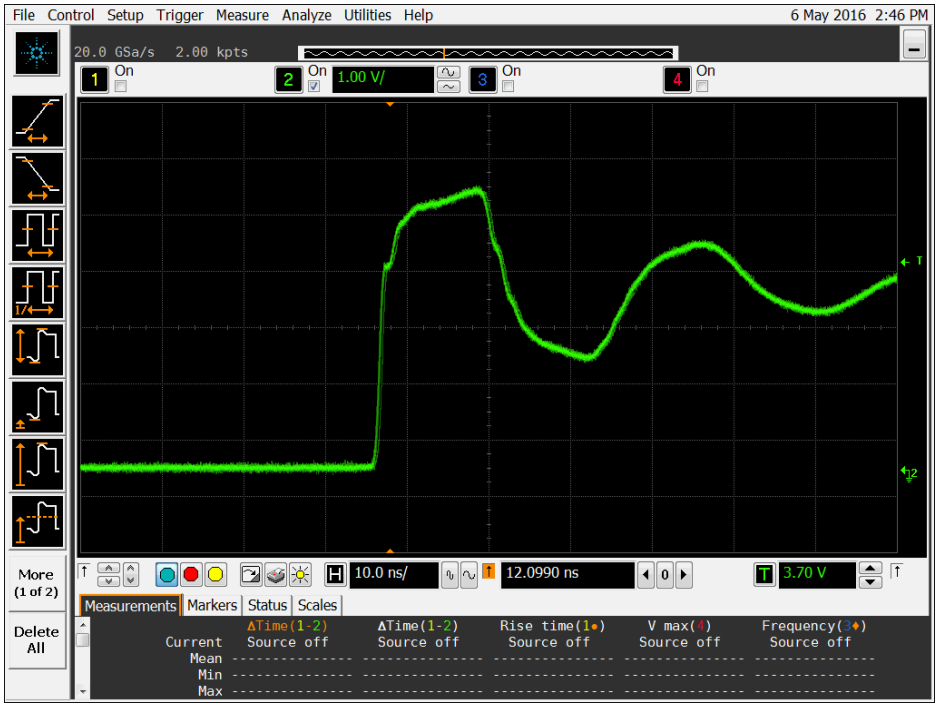

***Figure 16* • DUT 1197 Pre-Irradiation Rising Edge**

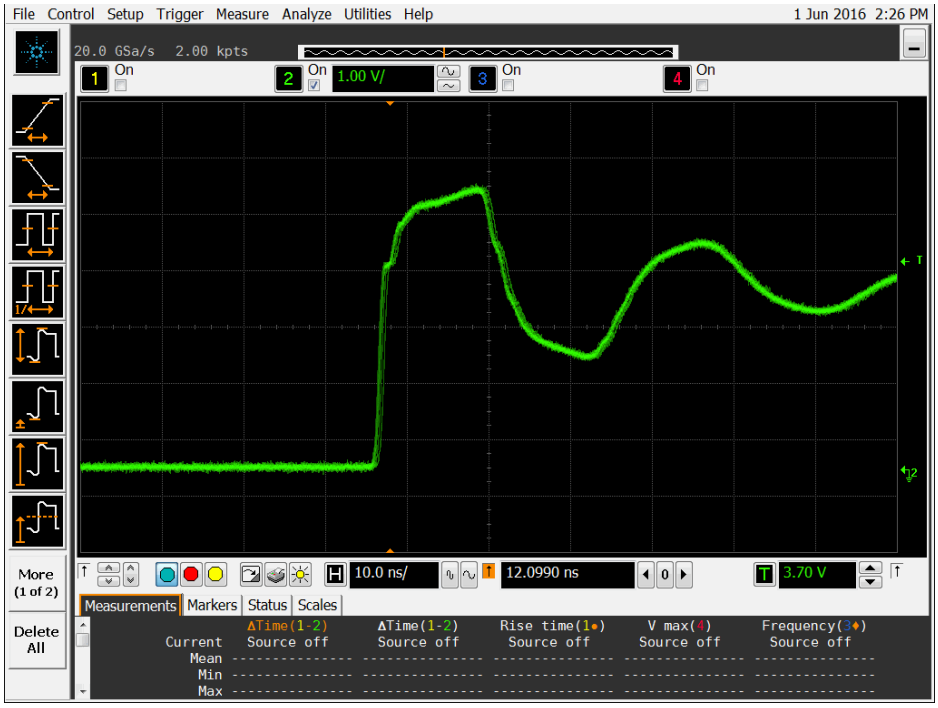

***Figure 17* • DUT 1197 Post-Annealing Rising Edge**

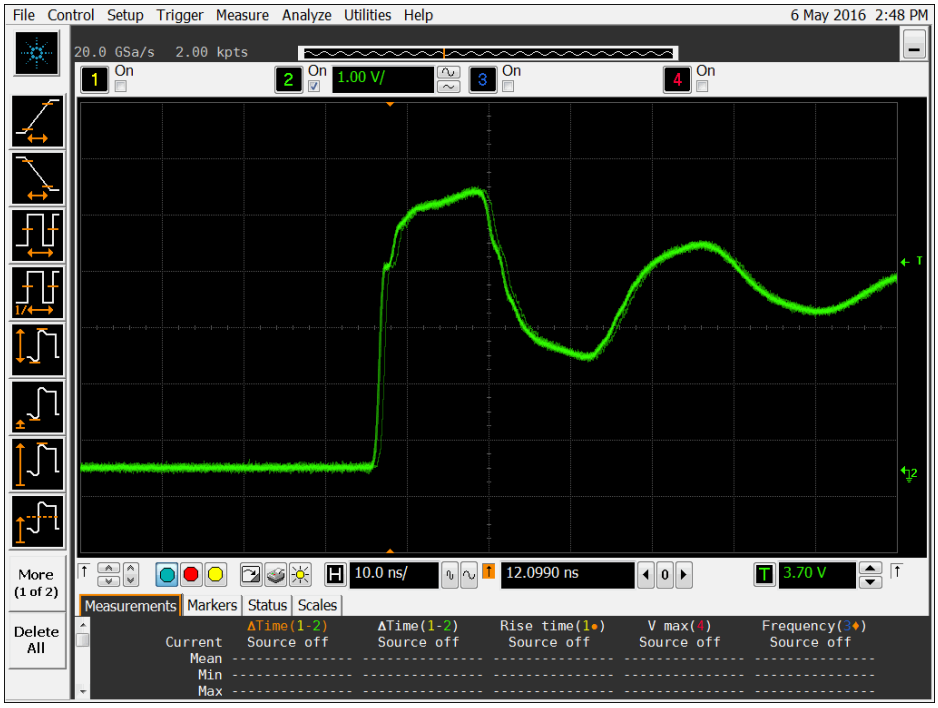

***Figure 18* • DUT 1216 Pre-Irradiation Rising Edge**

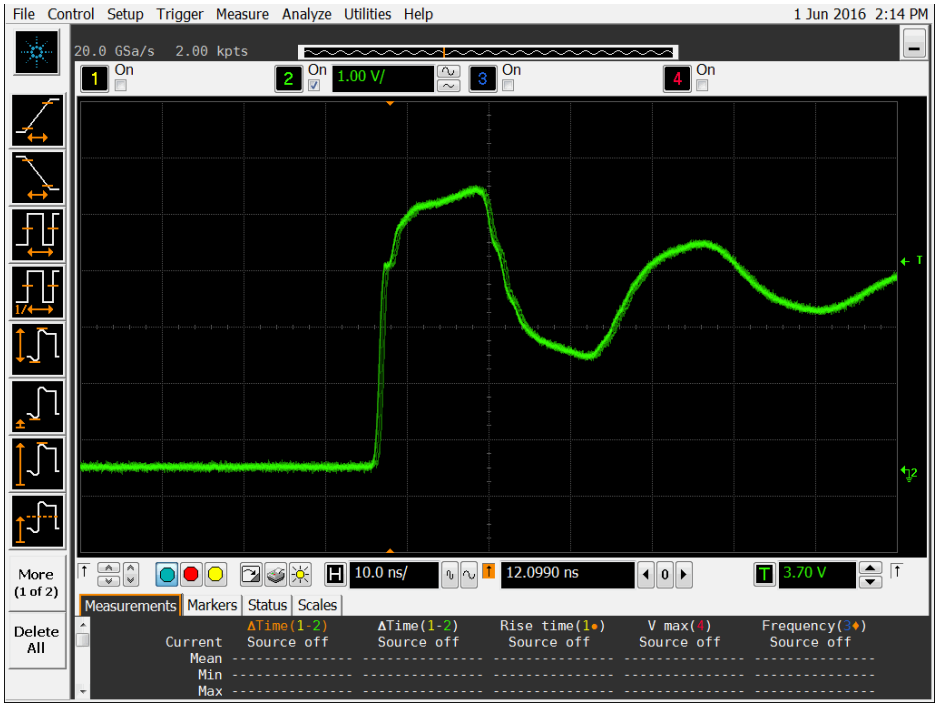

***Figure 19* • DUT 1216 Post-Annealing Rising Edge**

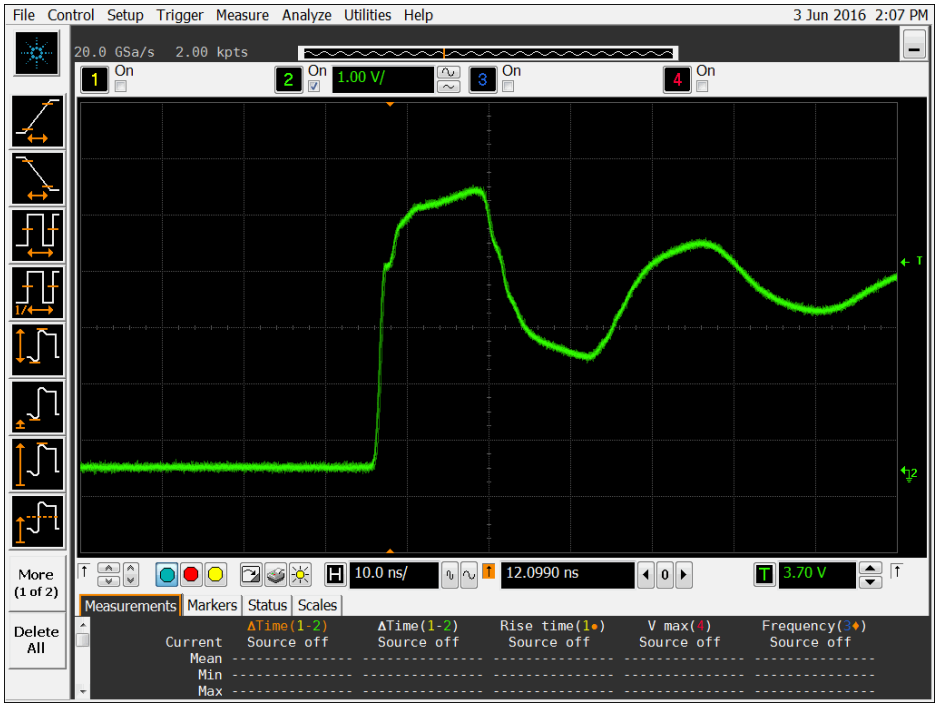

***Figure 20* • DUT 1190 Pre-Annealing Rising Edge**

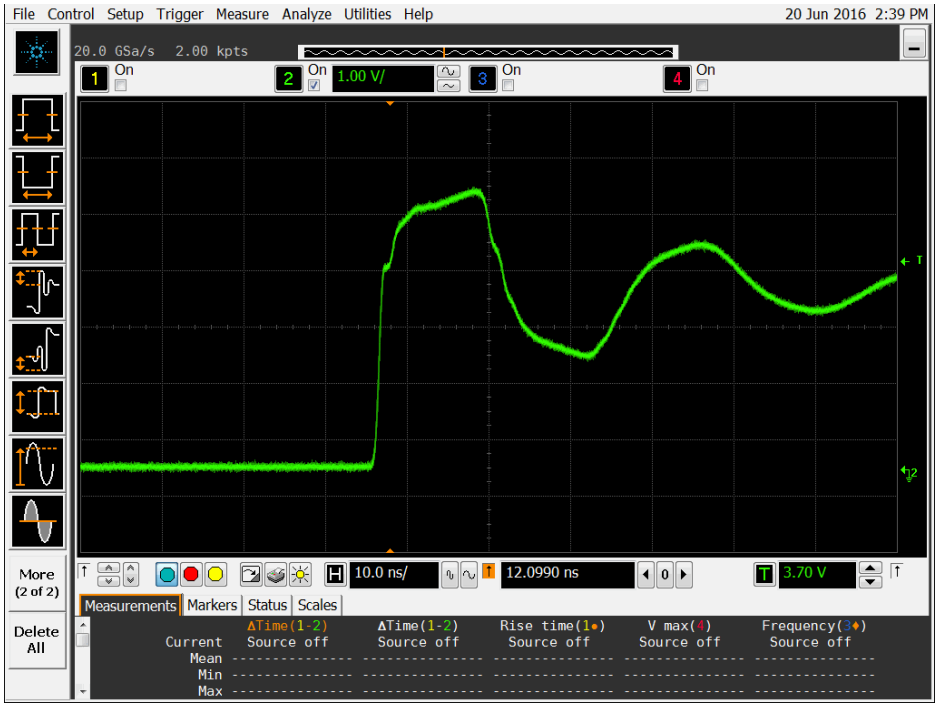

***Figure 21* • DUT 1190 Post-Annealing Rising Edge**

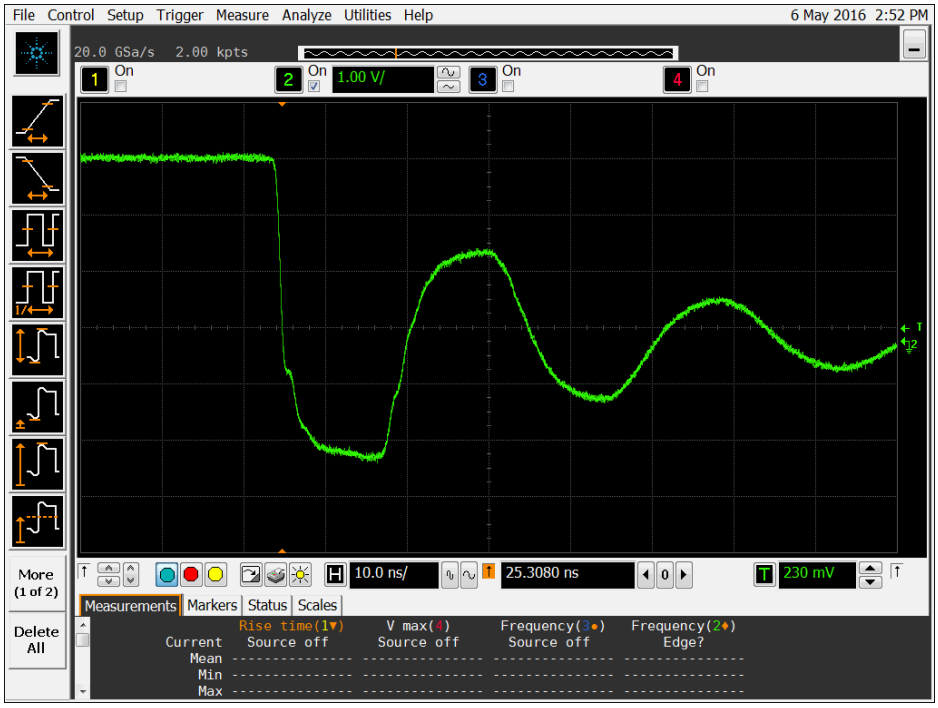

***Figure 22* • DUT 1194 Pre-Irradiation Falling Edge**

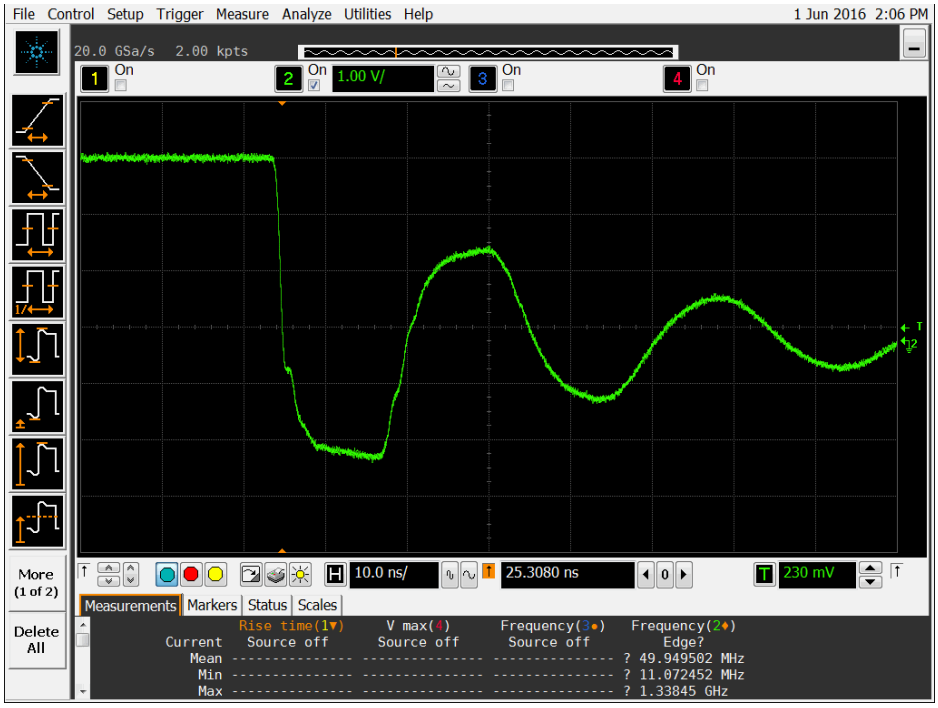

***Figure 23* • DUT 1194 Post-Annealing Falling Edge**

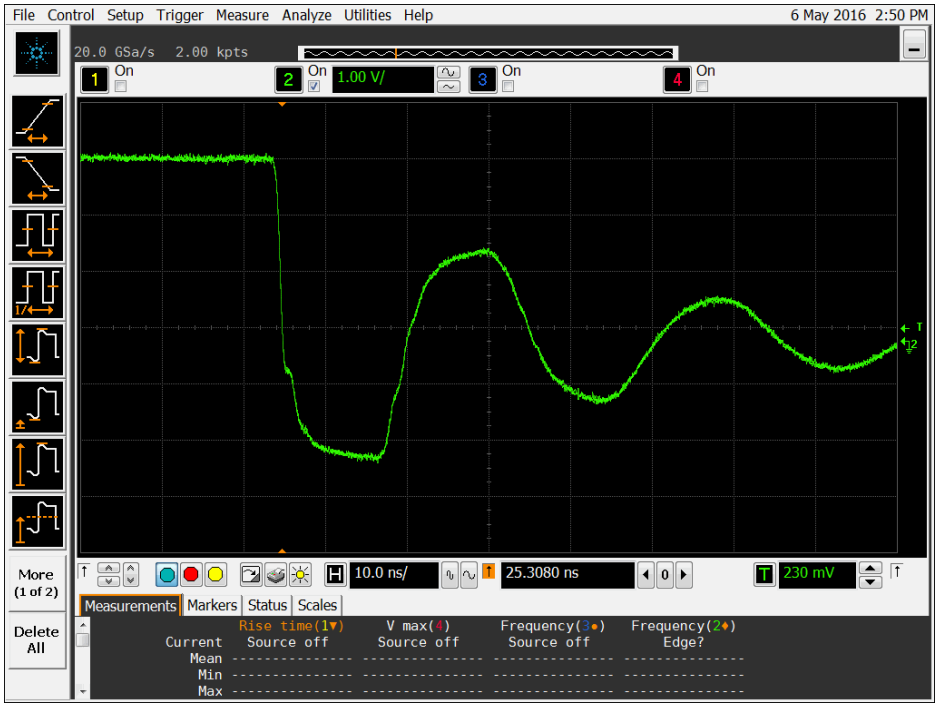

***Figure 24* • DUT 1198 Pre-Irradiation Falling Edge**

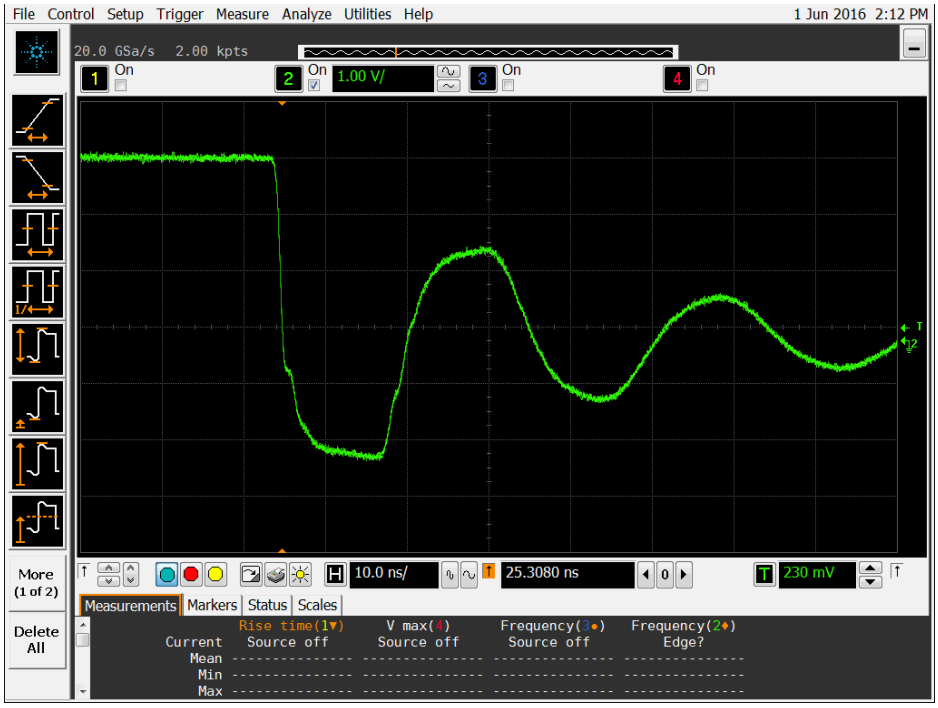

***Figure 25* • DUT 1198 Post-Annealing Falling Edge**

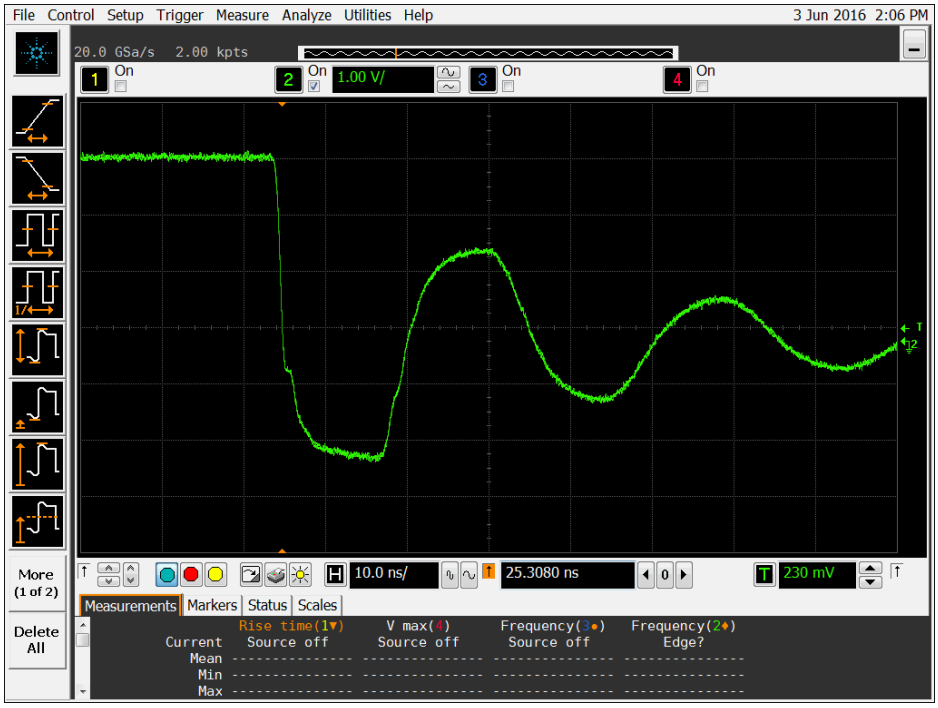

***Figure 26* • DUT 1200 Pre-Irradiation Falling Edge**

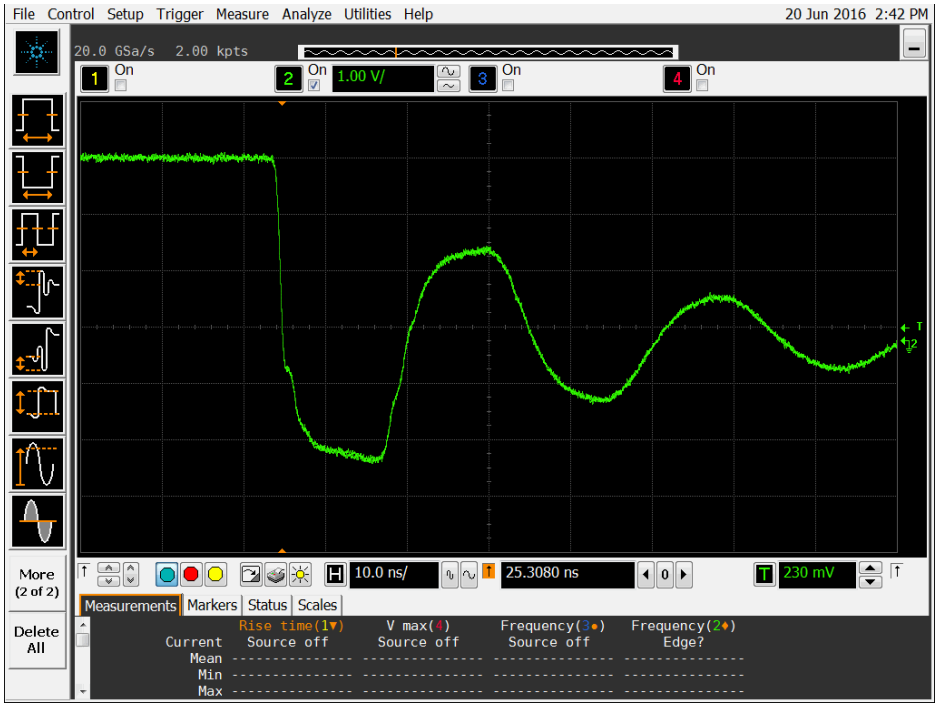

***Figure 27* • DUT 1200 Post-Annealing Falling Edge**

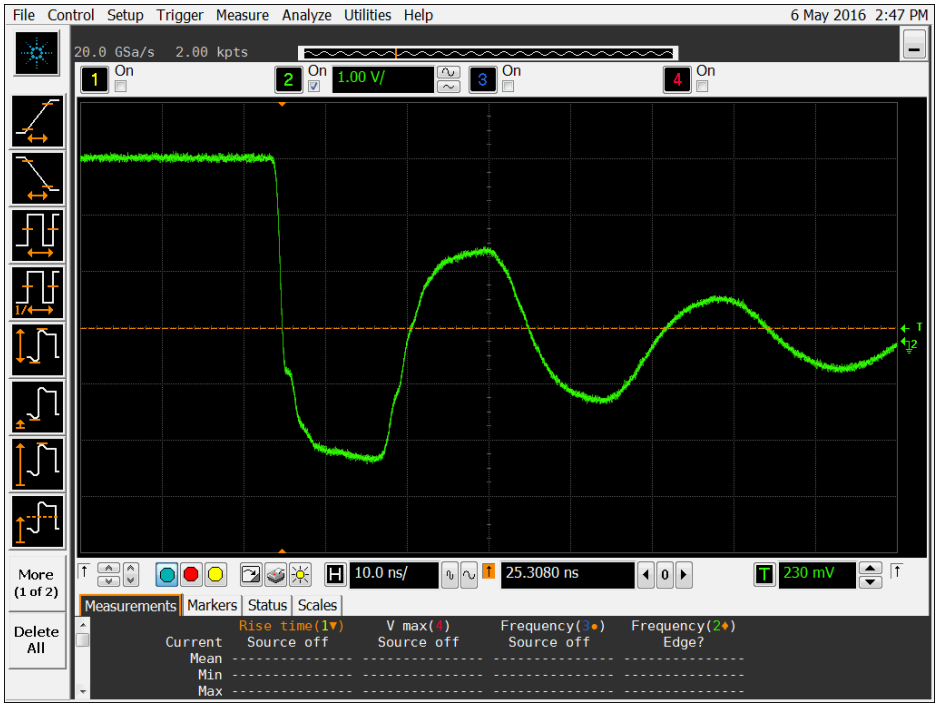

***Figure 28* • DUT 1197 Pre-Irradiation Falling Edge**

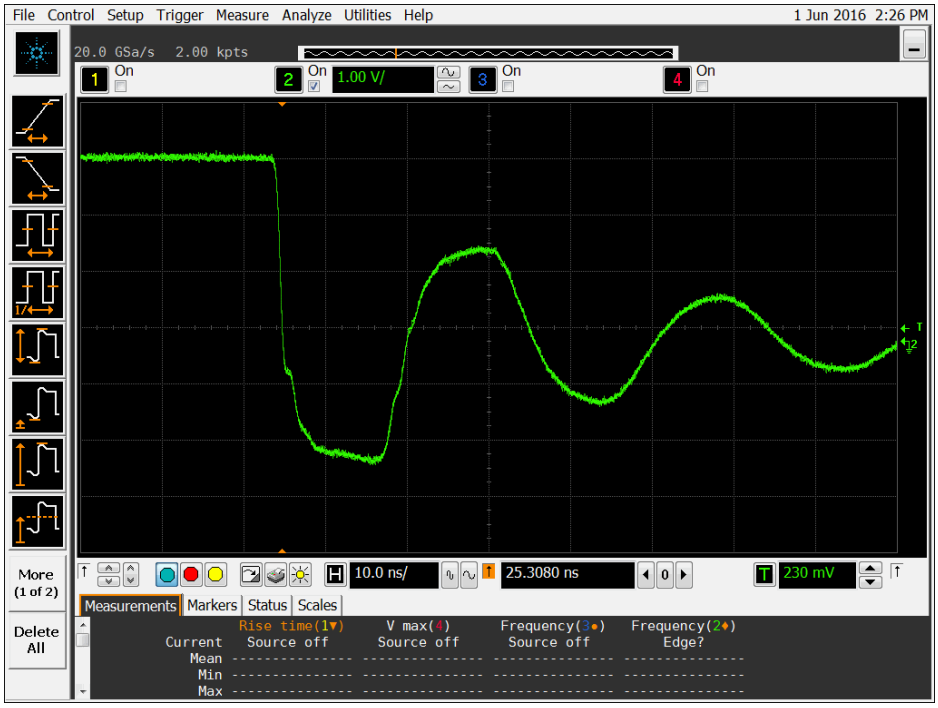

***Figure 29* • DUT 1197 Post-Annealing Falling Edge**

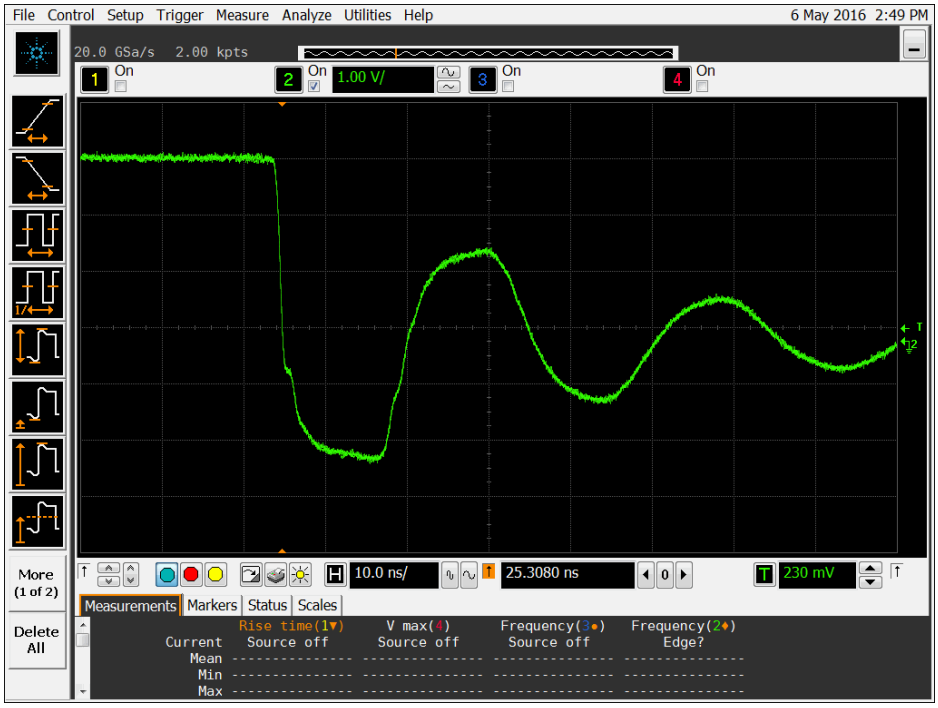

***Figure 30* • DUT 1216 Pre-Irradiation Falling Edge**

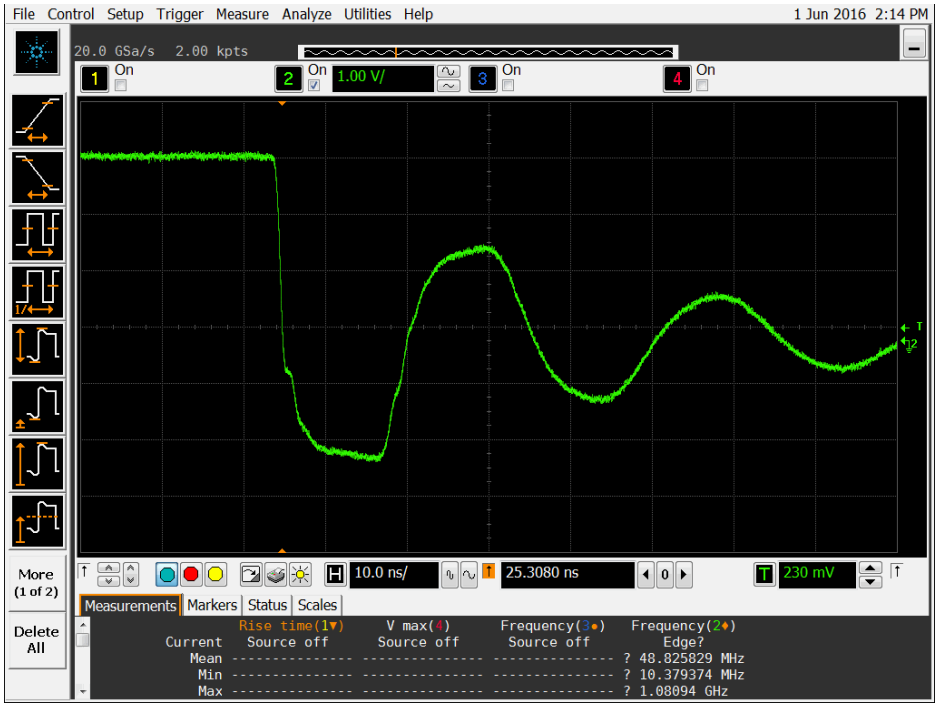

***Figure 31* • DUT 1216 Post-Annealing Falling Edge**

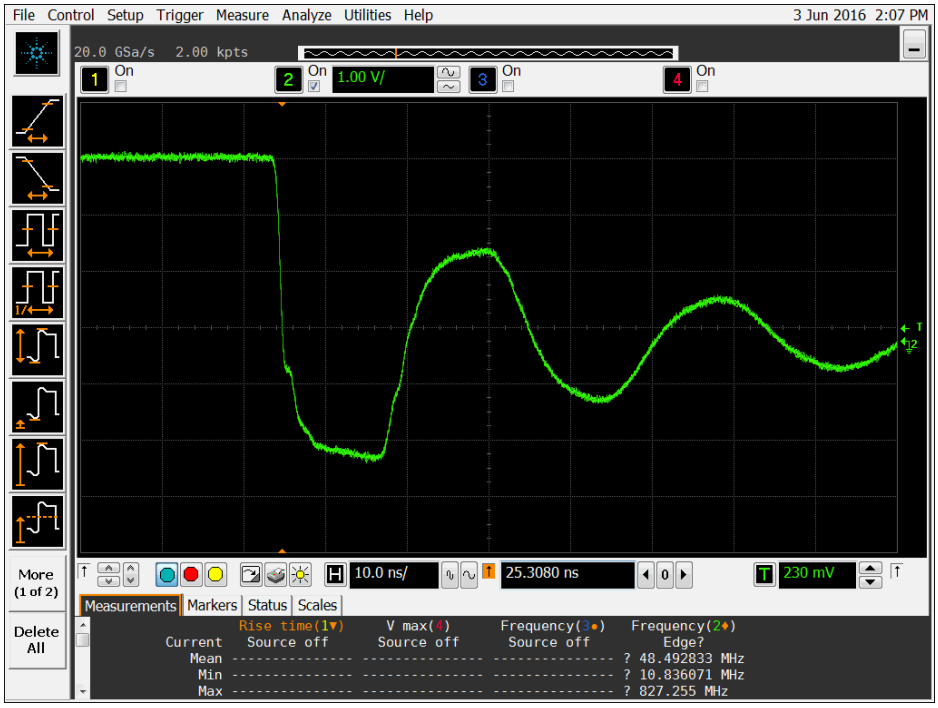

***Figure 32* • DUT 1190 Pre-Irradiation Falling Edge**

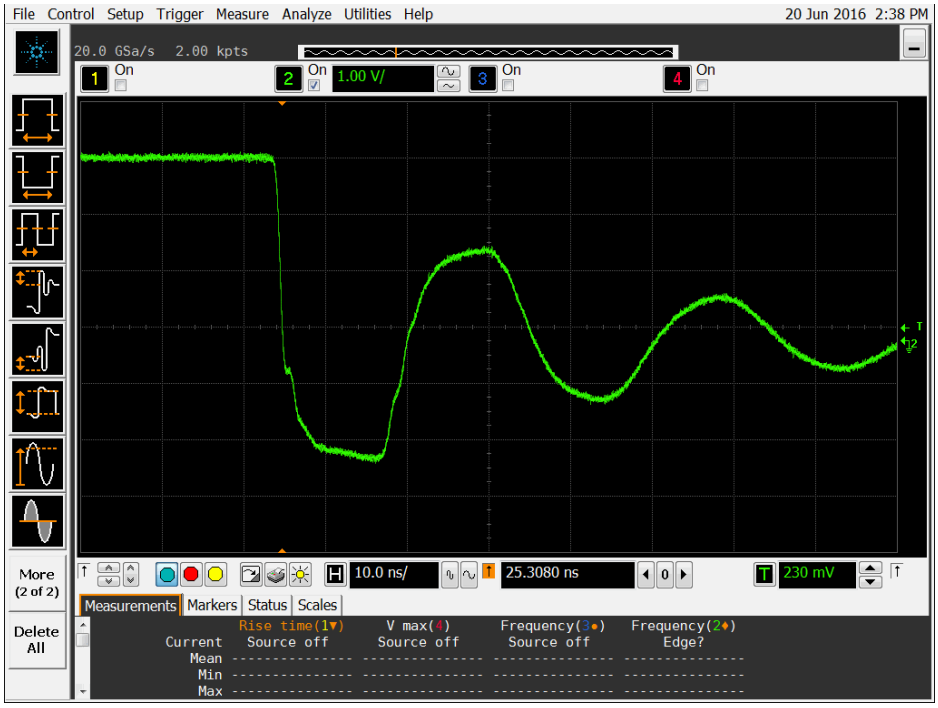

***Figure 33* • DUT 1190 Post-Annealing Falling Edge**