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| REVISION HISTORY | | | | | | | |
| **REV** | **DESCRIPTION** | | | **ECO** | **DATE** | | **UPDATER** |
| A | Initial Release | | | EC05044 | 03/05/12 | | J. Arsenault |
| A1 | Update with Finished Goods packaging | | | EC07378 | 11/01/12 | | D. Gallagher |
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| **Global Quality**  **Flow down Requirements Procedure**  Approvals for this procedure are:  Site Quality Directors  Process Owner: Supplier Quality Manager  **CHECK AGILE FOR CURRENT REVISION PRIOR TO USE.**  **VALID FOR 24 HOURS AFTER PRINTING** | | | | | | | |
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# Purpose/Scope:

The purpose of this procedure is to define specific workmanship requirements for commodities and/or sub assemblies that are either purchased or manufactured internally at Microchip It will also define the packaging requirements for shipping of Finished Goods.

If there is a conflict between this procedure and a part number and/or assembly drawing the drawings takes precedence over the requirements set within this procedure.

# Reference Documents

899-02003-74 Quality Records

699-02003-00 Purchasing Process and Supporting Procedures

699-02003-11 Purchasing Procedure Supplier Guide

799-00005-00 Engineering Change Control

899-00273-000 Global First Article Inspection Procedure

799-00006-00 Engineering Procedure Temporary Deviation Authorization (TDA)

IPC-A-600 Acceptability of Printed Boards

IPC-A-610 Acceptability of Electronic Assemblies

IPC-A-620 Requirements & Acceptance for Cable & Wire Harness Assemblies

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards  
J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

J-STD-003 Solderability Requirements for Printed Circuit Boards

IPC-7711 Rework of Electronic Assemblies

IPC-7721 Repair and Modification of Printed Boards and Electronic Assemblies

ANSI 20.20 ESD S20.20 Standard

ISTA 2A Packaging Test Standard from International Safe Transit Association

GR-78-CORE Generic Requirements for the Physical Design and Manufacture of Telecom Products and Equipment

GR-1221-CORE Reliability Assurance for Passive Optical Component Testing

JIS Z3198-7 Test methods for lead-free solders – Methods for shear strength of solder joints

# Definitions

**Contract Manufacturer**:

An organization producing or procuring certain commodities or services for Microchip.

Examples: PCBA’s, PCB’s Electro-Mechanical Assemblies, Metal Products

**Outside Processes**:

An organization providing Processes /Services beyond Microchip capability.

Examples: Plating, Welding, Calibration, Testing, Silk Screening

**Product Packaging**:

The packaging defined on the BOM for the product.

**Over Pack**:

Packaging used to consolidate Product Packages, may be on the BOM or may be determined at the time of shipment.

# Roles & Responsibilities

Global Supply Chain / Purchasing are responsible to insure this Quality Workmanship Procedure is flowed down to all suppliers prior to issuance of purchase orders for production commodities.

Supplier Quality is responsible to monitor and audit as deemed necessary to insure suppliers are meeting the quality requirements set forth within this procedure.

Contract Manufacturers shall have a Quality record retention process that is approved by Microchip Supplier Quality. As Required per Contract and/or Drawing, Quality Records shall be retained IAW (In Accordance With) Microchip Quality Records Procedure 899-02003-74.

Contract Manufacturers shall ensure the requirements set forth in this workmanship procedure are adhered to both internally as well as their sub-tier suppliers.

# Procedure for Electronic Commodities:

General Flux Requirements: Flux used on all commodities manufactured for use on Microchip deliverables shall be in accordance with

Class 3 products shall conform to the flux requirements of J-STD-001.

Class 2 products shall conform to flux requirements as follows,

Products that require cleaning shall use a flux activity level of no greater than M0 per J-STD-004

Products that do not require cleaning shall use No Clean Flux.

## Component Shelf Life

### Components with no shelf life defined by manufacturer, with Date Codes in excess of seven years, shall have Solderability test performed per J-STD-002 prior to being used on any Microchip assemblies.

### Components with a shelf life that exceeds 7 yrs shall be approved by Microchip prior to being used on all assemblies via a Temporary Deviation Authorization (TDA).

### Components, with manufacturing specifications stating shelf life is less than 7 years, shall require approval authorization from Microchip prior to being used on any assemblies. These components may require testing along with Solderability test per 7.5.2 above.

## Solderability Requirements for Bare Boards

### The printed circuit board fabricator shall comply with the requirements spelled out in the procedure. A C of C shall be provided with each lot of PCB’s stating the testing was successfully performed.

### The Contract Manufacturer shall upon receipt retain the solder samples and the C of C. These shall be available for examination upon request and shall be retained for a minimum of two years or as otherwise required per contract and Microchip Quality Record Procedure 899-02003-74. Solder samples may be retained by PCB Fabrication house and must be available for a minimum of two years.

### Microchip Supplier Quality shall audit this process when performing a site audit of the CM. The following tests are to be performed on 100% of all lots of Printed Circuit Board fabs in accordance with the IPC J-STD-003. There are two separate tests for both Tin/Lead & Lead Free solder alloys. For Lead Free Solder Alloys, a third Solder Float test shall be performed in accordance with GR-78 as described in 5.2.8. This applies to all Microchipboard fabs using Class 2 as the defining class unless otherwise defined on the drawings.

### Test A – Edge Dip Test for Tin/Lead Solder Alloy This test is for edge dip testing of surface conductors and attachment lands. The process to follow for performing this test is described in section 4.2.1 of the J-STD-003.

### Test C- Solder Float Test for Tin/Lead Solder Alloy For plated through holes, surface conductors and attachment lands, (solder source side only). The process to follow for performing this test is described in section 4.2.3 of the J-STD-003.

### Test A1- Edge Dip Test for Lead Free Solder Alloy This test is for edge dip testing of surface conductors and attachment lands. The process to follow for performing this test is described in section 4.2.6 of the J-STD-003.

### Test C1- Solder Float Test for Lead Free Solder Alloy For plated through holes, surface conductors and attachment lands, (solder source side only). The process to follow for performing this test is described in section 4.2.8 of the J-STD-003.

### GR-78 Thermal Stress (Solder Float) For plated through holes. The process to follow for performing this test is described in section 14.3.2 of GR-78-CORE, Issue 2.

### Test Failures Any failure of the above test samples shall be grounds for rejecting the entire lot. Should there be any question surrounding the acceptability Microchip Supplier Quality shall be contacted for resolution.

## Printed Circuit Boards.

### Date Code Requirements – PCB’s

### Date Codes: Fab boards having date codes exceeding shelf life listed below shall be baked in accordance with IPC-HDBK-001 Table 7-1 to eliminate the risk of delamination. Recommended maximum storage times after bakeout are detailed in table 7-2 of the IPC-HDBK-001.

6month = Finish type OSP, immersion Silver, immersion Tin  
 12month = Finish type ENIG, Electro-plated Ni/Au, HASL, Lead Free HASL

Boards exceeding these shelf life requirements shall also have solderability test performed on first piece per paragraph 5.1 prior to manufacturing production lots.

### Material of a different date code within a lot must be wrapped and identified separately.

## Solder Sample Requirements – PCB’s

### One solder sample is to be shipped with each production lot, wrapped separately and identified as “solder sample”. The sample board may be a rejected board for any other defect, except solderability.

### If shipping two (2) different date codes, ship one or retain (1) solder sample with each date code lot.

### The solder samples must be over and above the purchase order quantity. The purchase order shall not be considered complete unless the full order quantity and the solder samples are received.

## Solder Joint Shear Strength Requirements – PCB’s

### Shear Strength of solder joints on chip components using lead-free solder shall be evaluated with the test method described in JIS Z3198-7.

### The Contract Manufacturer shall produce a report stating the testing was successfully performed. Reports shall be available for examination upon request and shall be retained for a minimum of two years or as otherwise required per contract and Microchip Quality Record Procedure 899-02003-74.

## Gerber Data and Fab Drawing – PCB’s

### The Supplier is responsible for inspecting all media and reporting any discrepancy (minor or major) to the Buyer prior to fabrication.

### If the Supplier is able to correct a minor discrepancy in the artwork (those not involving a revision change), the Supplier is to communicate his/her intent to do so in writing prior to fabrication. Major discrepancies (those involving a possible revision change) are to be handled by the Engineer at Microchip

## PCBs – Approved Vendor List (AVL)

PCB’s must be manufactured by the vendor specified on the AVL, if one is designated, except upon written or electronic approval of Microchip All PCB’s whether on the AVL or not must be manufactured by a UL recognized vendor and appropriately marked as such except upon written approval of Microchip.

### PWB – Shall meet workmanship requirements per IPC-A-600 Class 2 unless otherwise noted in the P.O., or product specific documentation. PWB’s shall be fabricated per IPC-A-6012 Class 2 unless otherwise noted in the P.O., or product specific documentation.

### PCBA’s Workmanship – Microchip FTD workmanship is per IPC-A-610 Class 2 unless otherwise noted in the P.O., or product specific documentation.

**All operators and Inspectors shall be trained to IPC-A-610. Objective evidence of required training shall be maintained and available for review.**

**CM’s manufacturing commodities with ESD (Electro Static Devices) shall have an internal ESD procedure that is designed IAW ESD ANSI S20.20 to ensure the facility, workstations are ESD compliant and personnel have been properly trained. The procedure and associated training records shall be available for review upon Microchip request.**

### Unused Holes on PCBAs – Holes marked for components (silk screen identifying U8 etc.) must be masked prior to wave soldering, and should not be filled with solder. Vias and non-marked holes may be filled with solder.

### Lead Length On PCBAs – Lead lengths are to be per IPC-A-610 Class 2 unless otherwise specified.

### Socketed Components on PCBAs – Socketed components are not to be installed into the sockets until the socket is soldered, and the PCA is cleaned and dried.

### Serial Numbers on PCBAs - Serial numbers must be located at least .250" from any edge of the board as space allows. Serial numbers on PCBAs are required for all board-type products that are sold as separate items to customers.

### Assembly Number and Revision on PCBAs - All PCBAs must be marked with the current assembly number and revision. Top assemblies that are made from sub-assemblies (such as the 87-610 that is made using an 86-600) must also be identified.

### Acceptable Flux Levels- On PCBA’s numbered 86-357, -600, -732, -8000, no flux residues are allowed, all other criteria shall conform to IPC-A-610 Class 2. All other PCBA’s shall meet IPC-A-610 Class 2 for workmanship and cleanliness unless otherwise specified.

#### Fluxes used in the assembly of Microchip products must pass Electromigration resistance test per GR-78. Test results must be provided to Microchip upon request.

## PCBA Bag and Tag / Labeling Requirement

### All circuit board assemblies built at Microchip’s Contract Manufacturers (CM’s) shall have a label attached to the ESD bag that contains the following information. The size of the label, the font size and style is the CM’s choice. Labels should be white in color. Label adhesive material shall have a Tg (glass transition) temperature of 95°C or greater as described in GR-1221.

* Microchip Part Number.
* Revision of the assembly.
* Vendor name and location.
* Date of production
* Country of Origin

### “MADE IN XXX” markings on PCB Boards and Assemblies: All Printed Circuit Boards and Assemblies built at CM’s shall be marked with the Country of Origin (XXX). This may require modifying markings on the PCB to comply with Country of Origin regulations.

**PCB Fabricated Boards:**

The Country of Origin marking “Made in XXX” is usually part of the Silkscreen Artwork defined by the Gerber Files.

**Released and Controlled Gerber Files:**

* May have “Made in USA” pre-defined.
* May have other Incorrect markings defining the Country, Manufacturer, or Point of Origin
* May have an Empty Rectangular Box defining the location for the Country of Origin Markings.
* May not have any information defining the Country of Origin.

The Country of Origin can be added using either Option #1 or Option #2 as defined below.

**PCB Fabricated Boards Option #1:**

* Change the Gerber File.
* Only Change the Top Level Silkscreen that defines the Country of Origin.
* Delete the “Made in USA” or other incorrect markings.
* Add “MADE IN XXX” where XXX defines the Country of Origin’s Full Name or Abbreviation.

Location of the Markings shall be in the same area as the markings that were replaced, inside the pre-defined rectangular area, or where approved by Microchip Engineering.

**PCB Fabricated Boards Option #2:**

* Do Not Change the Gerber File.
* Manufacture the PCB with the incorrect markings on the Silkscreen Artwork.
* Cover the Incorrect markings with White or Black Non-Conductive Ink.
* Mark with “MADE IN XXX”
* Use Black or White Permanent Non-Conductive Ink
* Silkscreen, Ink Stamp, or other methods are acceptable.

**PCB Assemblies:**

The Country of Origin marking “Made in XXX” defined on the Fabricated Board may have to be changed for the PCB Assembly Country of Origin.

* If the PCB marking on the Board is the same as required for the Assembly, then No Changes are required.
* If the PCB marking is not correct or is not defined on the Board, then the correct Country of Origin markings much be added.
* Create a Label with “MADE IN XXX”.
* XXX defines the Country of Origin’s Full Name or Abbreviation.
* Cover the existing marking with the New Label.
* If No Markings are present, locate label where approved by Microchip Engineering.

# Backplane Assemblies: Reference Appendix A

Backplane assemblies are to be manufactured and tested per the following instructions:

## General Requirements:

### Only approved suppliers may be considered as sources to fabricate, assemble or test Microchip backplanes.

### None of the conditions or tests stated in this procedure may be waived without written approval from the Microchip Quality Team.

### The supplier shall develop the tests and procedures to cover the requirements specified in this document.

### All documentation relating to the assembly and testing of all backplanes shall be retained for a minimum of 10 years post shipment.

### All tests and procedures are to be approved by Microchip Engineering and Quality Originations prior to implementation.

### Where IPC-A-600 & IPC-A-610 are called out in this procedure class 2 is required unless otherwise specified on the assembly drawings.

## Phase I, Bare Board Testing:

These tests are to be performed by the PCB Manufacturer. It must be performed on 100% of the PCB’s in every lot. PCB’s at this step with inner layer faults cannot be repaired without written approval from the Microchip Quality Team.

## Continuity and Isolation:

### Test will cover 100% of all accessible nets.

#### High Frequency Impedance Characteristic Test:

#### Results to test coupon per PCB panel. Microchip to supply information on which traces are to be controlled and tolerance criteria. The PCB designer must identify traces with controlled impedance requirements. The may be in the form of a netlist. The Assembly drawing does include notes regarding this topic (see Note 7 in 065-50301-01 for example). The supplier may define the coupon for impedance testing.

6.3.1.1.1 Test results of coupon testing shall be provided to Microchip upon request.

6.3.1.1.2 Test coupons shall be retained for retesting for a minimum of 2 years post shipment.

### DC HiPot (Dielectric Breakdown) Test: @ 1500v (min.) for a duration of 15 sec (min.). Test will include all power and grounds. Microchip will specify any other signal traces to be tested. Dielectric test to be applied to all traces noted in the PCB fabrication drawing. PCB designer identifies traces and signals (including power) to be tested. Passing criteria is <5ma current leakage.

### Verification of all silkscreen and PCB markings.

## Phase II, Final Assembly Test

The following tests are to be performed by the backplane’s assembly manufacturer. They must be performed on 100% of the backplanes assembled and can be accomplished by any combination of the following test methods: : ICT (In circuit Test), AOI (Automated Optical Inspection). Flying Probe, Pico Capacitance or X-ray:

### The test will cover 100% of the nets for Continuity (typically less than 20ohms) and Isolation (typically greater than 5Mohms). Systems that use Pico-capacitance measurements will typically use a plus/minus 30% pass/fail window of the nominal value for each net measured from a known good (gold standard) PCB. Gold standard board(s) to be selected from Limited Availability/Pilot build after full testing cycle. Microchip Engineering supports approving gold standard units during Stage 4.

### The test will include checking the continuity through all connectors. Provide test coverage reports stating exceptions.

### The test will include checking for bent or broken pins, missing or incorrectly installed polarity or alignment keys on all connectors and through hole parts per IPC-A-610. This test will also include verification of all components on the backplane.

### DC HiPot (Dielectric Breakdown) Test: @ 1500v (min.) for a duration of 15 sec (min.). Microchip to specify signal traces to be tested. This DC test, Pass criteria is < 5ma leakage current.

## Phase III, Final Inspection

This test is to be performed by the backplane’s assembly manufacturer and must be performed on 100% of the backplanes assembled and can be accomplished by any combination of the following inspection methods: AOI or Manual. The inspection will cover the following:

### Overall Manufacturing Quality of the backplane to IPC-A-600, Workmanship for Bare Boards and IPC-A-610 Workmanship for Finished Backplanes.

### Verify that all labels are correctly and neatly placed.

### Verify that the solder mask is correct and that all components are of the correct footprint for its pads and solder mask. This visual or AOI inspection is intended to identify footprint mismatch problems (eg. Mis-installed components).

### After Microchip approval, all test software and controlling assembly/testing documentation will become controlled documents and can only be changed through the Microchip EC process.

### When possible the test printouts should be included with each backplane shipped.

### When a printout is not possible a certificate of conformance stating that all units in the lot shipped have passed all tests that individual printouts are not available for.

### All backplanes will be stamped with permanent ink indicating that the backplane has passed all tests. It will also include the identifier of the person that tested the backplane and the location of the facility (labels with non-smearing ink may be used in place of a stamp). Stamp or label must be located in a consistent position.

## See Appendix A for Backplane Testing Flow Chart.

# Cosmetic Specification

## Definitions

### **Anodize -** Coating result of treating aluminum electrolytically in a bath of acid to produce a uniform anodic coating on the metal surface. Anodize is electrically non-conductive. Base metal damage is not acceptable.

### **Bend Deformation -** The increase in width of a part at a bend as compared to the width on either side of a bend. The increase is due to metal flow parallel to the bend line. There shall be no fracturing of the metal at the bend radius.

### **Bleed Out -** Usually causedwhen colors run or become diffused during a paint or silk-screening operation.

### **Blister -** Hollow raised spot on the surface caused by lack of adhesion of the coating material to the base material. This can also occur on painted, plated or silkscreened surfaces.



### **Chem film -** A chromate conversion coating used to passivate aluminum, zinc, magnesium, and other non-ferrous metals. It is a chemical process applied nonelectrolytically by immersion, spray or brush.

### **Burrs -** Raised, sharp edges inherent in the cutting operations such as shearing, blanking, punching and drilling.

****

### **Cavity-** Depressions caused by improperly seated hardware such as rivets, inserts, etc.

### **Corrosion -** Also known as oxidation or rust. The visible deterioration of a material, due to a chemical reaction (ref. section 3.19)



### **Crack -** A line along which something has split without breaking into separate parts

### **Dent/Ding -** Also known as sink. A depression on the surface.

****

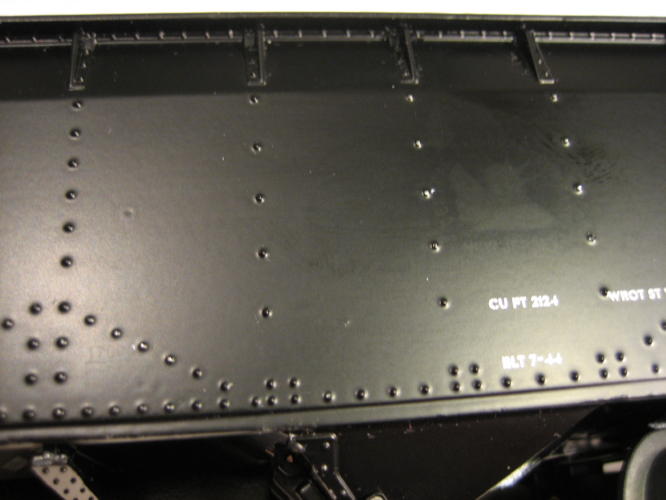
### **Discoloration -** Any change from original color or unintended inconsistent color.

****

### **Fish Eye -** Larger depressions is the surface finish caused by contamination.



### **Fingerprint -** A noticeable fingerprint image in plating or paint finish.



### **Foreign Material -** An attached particle that is not part of the base material or finish. Adherence means that the particle cannot be removed by an air blast.

****

### **Glossiness** - (refers to paint or silkscreen application only.) An area of excessive or deficient gloss.

### **Graining -** Cosmetic abrasive finishing of sheet metal. Graining helps remove burrs and can improve plating cosmetics as well by removing small scratches and oils.

****

### **Indentation -** A surface dent other than the spherical depression caused by spot welding or dimpling.

****

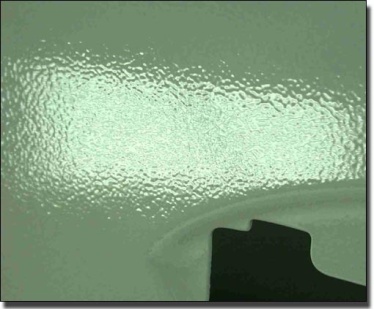
### **Lint -** Any unintended foreign substance in the coating or on the surface.

### **Masking -** Aprocess typically using tape to cover a surface not intended to be painted.

### **Non-uniform coverage -** Areas that have insufficient (bare spots) or excessive coating.



### **Orange Peel -** A certain kind of finish that may develop on painted and cast surfaces. The texture resembles the bumpy surface of the skin of an orange



### **Over spray -** Paint or other material on unintended areas or mist on previously finished areas.



### **Oxidation** - Has a rough feel or appearance. A dull gray, dark gray, black, brown, dark cinnamon or possibly white colored substance. (ref. section 3.7)



### **Plating Burn -** A noticeable discoloration is the plating finish.

## burnt plating.jpg

### **Peeling -** Also known as Flaking; Detachment of finish material due to loss of adhesion.

****

### **Pin Hole -** Small pits or depressions usually caused by incomplete fillings of a porous surface, or breakage of air bubbles when top coat was being sprayed.

****

### **Pitting -** A cluster of holes pores, or pits in the base material.

****

### **Plating Stain -** Astained appearance in the plating finish

## plating-stains.jpg

### **Protrusion -** Something that protrudes beyond the usual limits, or above a plane surface.

### **Runs -** (refers to paint application only) Excessive coating that causes drips or non-uniform coverage.



### **Scratches -** Grooves or grinding marks.

### **Light Scratch -** Can be seen at normal viewing, but cannot be felt with the finger.

### **Scuff Marks -** A difference in the tone or shade of the paint or powder coat or plating caused by abrasion.

### **Smeared/blurred -** indistinct or hazy in outline



### **Seams and Gaps** **-** Any breaks in the continuity of the coated surface created by countersunk hardware, butt joint, etc.

### **Specks -** Small particles visible in the finish.

### **Texture -** A visible variation/pattern of the surface finish.

### **Tool Marks -** Marks that are made directly from the punching or secondary operations.



### **Touch up -** The correcting of a flaw in the original finish.

### **Void -** Where there are empty spaces commonly caused during the painting, plating, or welding processes.

## General

### No deviation from the specification is allowed, without an Engineering Change Order (ECO) or Temporary Deviation Authorization (TDA).

### Fabricated parts “must” be “identified” with Microchip’s part number, revision letter, and supplier logo/name on the non-appearance side of the part. Permanent ink (not removed with common cleaners Windex or Isopropyl alcohol) or metal stamping is acceptable for part marking. If the part is too small to be “marked”, bag and tag can be used.

### All plated parts with silkscreen shall comply with Class B requirements.

### Alternate supplier substitution for commercial hardware is acceptable where form, fit and function are unaltered unless specifically prohibited on the drawing.

### Assembled parts, riveted, welded, ect., shown in the same plane are assumed to be coplanar within .015 inch at any point along the line that they meet.

### The head of countersunk rivets shall not extend beyond the plane of the surface that they are installed in.

### Unless otherwise specified, tolerances for all open holes are to be +/-0.005 [0.13 mm] before painting and +/- 0.01 [2.54 mm] **after painting**.

### Reference Dimensions: Dimensions locating cosmetic areas designated by phantom lines, dimensions in parenthesis or marked as "REF", are for "REFERENCE" only and should not be measured.

### Repetitive Inspection: A flaw that occurs repeatedly in the same surface location becomes more easily noticed. If the same cosmetic flaw was judged to be acceptable at the beginning of the inspection or run, it shall be judged acceptable at the end.

### Gloves shall be used during handling of finished metal parts, to prevent fingerprints or smudging of finished surfaces.

### For First Article requirements, reference Work Instructions 899-02003-01/1.27 (production) and 899-02003-01/1.30 (prototype).

## Cosmetic Class Codes

Cosmetic surface class codes in this procedure are used as alpha letters “A through C”.

### **Class A** - Highly decorative surface in constant view of the customer. Front panel, 19” rack mount device.

### **Class B** – Moderately decorative surface in occasional view of the customer without the unit *being removed. Examples include but are not limited to the top and sides of rack-mounted* chassis, rearfaceplates.

### **Class C** – Interior surface of the unit.

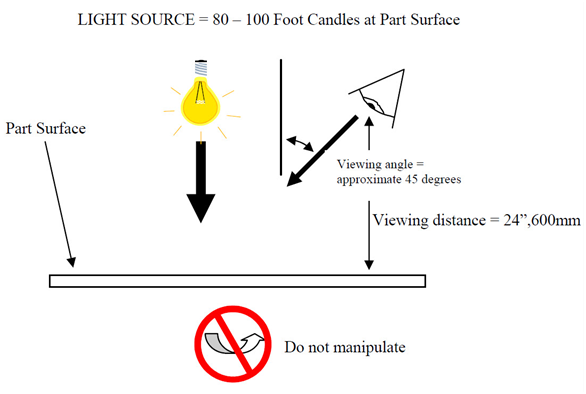
## Viewing Conditions

**(Class A and B)** Parts and products to be inspected under the following conditions:



Light source shall be cool white fluorescent (CWF 2) light

**(CLASS C)** Parts and products shall be inspected under the following conditions:



Light source shall be cool white fluorescent (CWF 2) light

### Uniform, non-directional lighting between 80 and 100 foot candle. At levels greater than 100 foot candles, caution should be taken not to over inspect.

### Viewing angle should be 45 degrees in direction to the part being inspected.

### Class A and B surfaces shall be manipulated during inspection to achieve maximum reflection of a light source. Class C surfaces shall **NOT** be manipulated during inspection.

## Time and Distance Inspection

**“Viewing time”** indicates the duration of the observation. The more critical the cosmetic surface, the longer the inspection period. “Viewing distance” indicates how far the inspector will be from the parts.

The more critical the surface, the closer the inspector will be to the parts. Parts will be inspected in accordance with instructions on the part drawing, if available. If the drawing references this procedure, the codes will reference **Table 1**.

**Table 1**

|  |  |  |  |
| --- | --- | --- | --- |
| **Class** | **A** | **B** | **C** |
| Viewing Distance | 450 mm (18”) | 450 mm (18”) | 600 mm (24 in.) |
| Viewing Time | 10 seconds | 5 seconds | 3 seconds |
| Viewing Area | 50 sq. inches | 50 sq. inches | 50 sq. inches |

Discernable variation from the guidelines specified within this document shall be grounds for rejection.

Note: Class “A” & “B” surfaces shall be manipulated during inspection to achieve maximum reflection of a light source. Class “C” surfaces shall **NOT** be manipulated during inspection. Refer to Class A, Class B and Class C viewing condition figures below

**Acceptance criteria is defined within Table 2**

Table 2 Acceptance criteria using surface class, lighting and viewing distance requirements in sections 5.0, 6.0 and 7.0.

|  |  |  |  |
| --- | --- | --- | --- |
| **Flaw** | **Class A** | **Class B** | **Class C** |
| Bleed Out | Unacceptable | Gradual color change is acceptable | Gradual color change is acceptable |
| Blister | Unacceptable | < 1% of surface area and 1” diameter. No corrosion potential. Acceptable adhesion tape test per IPC-TM-650 | < 1% of surface area and 1” diameter. No corrosion potential Acceptable adhesion tape test per IPC-TM-650 |
| Burrs | Unacceptable | Unacceptable | Unless otherwise specified, burr height not to exceed 10% of material thickness. |
| Cavity | Unacceptable | Unacceptable | Acceptable |
| Corrosion | Unacceptable | Unacceptable | Unacceptable |
| Crack | Unacceptable | < 1/8” no base material exposed | < 1/8” no base material exposed |
| Ding/Dent | Unacceptable | Not acceptable except on edge of part qty. 1 Max length .125 depth .030 No base material exposed | 1 max per 50 sq. ft area Max depth .030 Max dia.030  Cannot affect class A or B side of part. No base material exposed |
| Discoloration | Unacceptable | Gradual discoloration or texture change | Gradual discoloration or texture change |
| Fish Eye | Unacceptable | Unacceptable | Unacceptable |
| Fingerprints | Unacceptable | Unacceptable | Acceptable |
| Foreign Material | Unacceptable | Unacceptable | Acceptable |
| Glossiness issue (discernible change in glossiness i.e. uniformity ) | Unacceptable | Acceptable | Acceptable |
| Indentation | Unacceptable | Unacceptable | Acceptable |
| Lint | Unacceptable | Unacceptable | Acceptable |
| Masking | Acceptable as part of normal paint process | Acceptable as part of normal paint process | Acceptable as part of normal paint process |
| Non-uniform Coverage | Unacceptable | Unacceptable | Unacceptable |
| Orange Peel | Unacceptable | Acceptable | Acceptable |
| Overspray | Unacceptable | Unacceptable | Acceptable as normal part of paint process |
| Oxidation | Unacceptable | Unacceptable | Acceptable  no corrosion potential |
| Plating Burn | Unacceptable | Unacceptable | Unacceptable |
| Peeling | Unacceptable | Unacceptable | Unacceptable |
| Pin Hole | Unacceptable | Unacceptable | Unacceptable |
| Pitting | Unacceptable | Unacceptable | Unacceptable |
| Plating Stain | Unacceptable | Qty. 2 per 50 sq.” area. Max dim: .06W x 0.5L | Acceptable |
| Protrusion | Unacceptable | Unacceptable | Unacceptable |
| Run | Unacceptable | Unacceptable | Does not exceed .25”W x .25L |
| Scuff Marks | Unacceptable | Unacceptable | Acceptable as part of normal mfg. process |
| Smeared/Blurred | Unacceptable | Unacceptable | Does not exceed .25”W x .25L |
| Seams/Gaps | Unacceptable | Unacceptable | Acceptable as part of normal mfg. process |
| Specks | Unacceptable | Unacceptable | Acceptable |
| Surface Finish (visible variation in texture) | Unacceptable | Unacceptable. | Acceptable |
| Tooling Marks | Unacceptable | Unacceptable | Acceptable |
| Touch Up | Unacceptable | Acceptable | Acceptable |
| Void | Unacceptable | Unacceptable | Does not exceed .125 dia. No corrosion potential |

**Scratches**

Scratches which are within 0.25”L x 0.015” W

|  |  |  |  |
| --- | --- | --- | --- |
| **Surface Area** | **A** | **B** | **C** |
| Up to 20 sq. inches  Up to 50 sq. inches  Up to 200 sq. inches  200+ sq. inches | 0  0  0  0 | 3  6  10  20  No corrosion potential | Acceptable ( no corrosion potential) |

Scratches which are within 1.0” L x 0.015: W

|  |  |  |  |
| --- | --- | --- | --- |
| **Surface Area** | **A** | **B** | **C** |
| 10-20 sq. inches  21-50 sq. inches  51-200 sq. inches  200+ sq. inches | 0  0  0  0 | 1  2  3  7  No corrosion potential | Acceptable (no corrosion potential) |

Scratches which are within 1.5”L x 0.015”W **Class B only**

|  |  |
| --- | --- |
| Surface Area | Number of scratches allowed |
| 200+ sq, inches | 1  No corrosion potential |

Accumulation of scratches along a continuous line, where no segments violate the tables above should not exceed 2.5” in length.

A continuous line where portions are phantom is still considered a scratch.

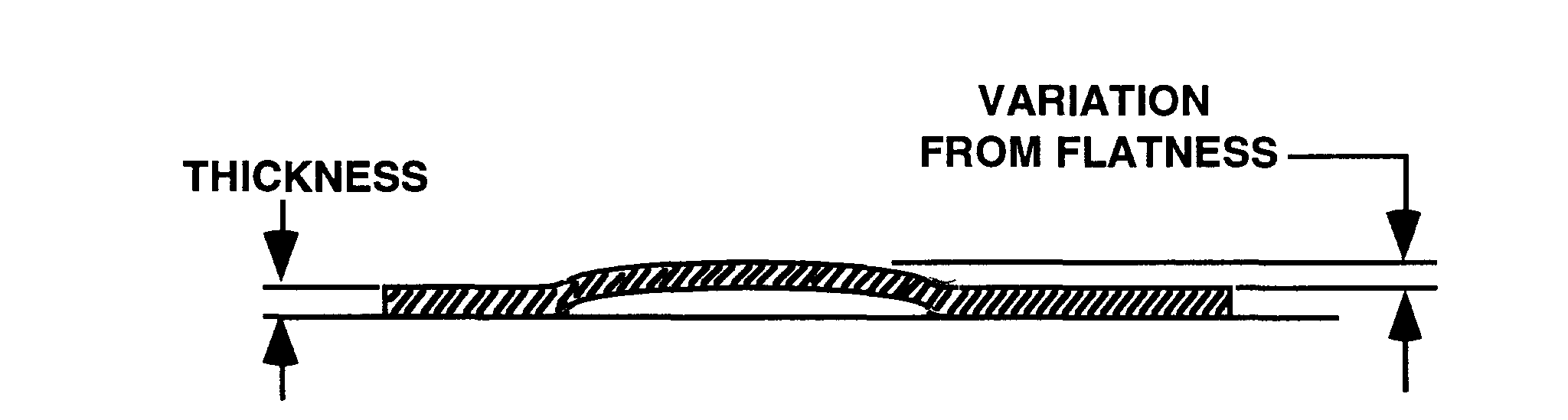
**Accept/Reject** When flaws are observed within the specified time and distance, and the accept/reject decision is difficult to make the part should be deemed acceptable.

## Flatness

### Variation from flatness will be measured by laying the parts on a surface plate with the convex side up, and measuring from the maximum rise. Clamps and weights will not be used during the measurement.

### Table 3 below defines acceptable variation from flatness.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Thickness** | **3”** | **3” TO 10”** | **10” TO 24”** | **24” to 48”** | **Over 48”** |
| .016 to .040 | 0.015 | 0.040 | 0.080 | 0.160 | 0.160 |
| .041 to .093 | 0.010 | 0.030 | 0.055 | 0.110 | 0.130 |
| .094 to .189 | 0.008 | 0.025 | 0.040 | 0.080 | 0.130 |



## Burrs

Raised, sharp edges inherent in the cutting operations such as shearing, blanking, punching and drilling.

### **Burr direction** - Unless otherwise noted on the drawing, we assume that all burrs are face up, when viewing a plane view print of the part. In a form (formed feature), burr direction is assumed to be the inside of the form.

### **Burr height** - Is related to material thickness. The expected burr prior to tumbling and deburring is typically less than 10% of the material thickness.

### **Burr Free** - Is generally used to describe sheet metal parts that have been deburred resulting in a 0.002 to 0.003 rounded edge. This should only be inspected if noted on the print.

## Graining

Cosmetic abrasive finishing of sheet metal. Graining helps remove burrs and can improve plating cosmetics as well by removing small scratches and oils.

### Minimum part size for graining is 6 inches (150mm). Part sizes smaller than 6 inches (150mm) will require fixturing to hold the part in place.

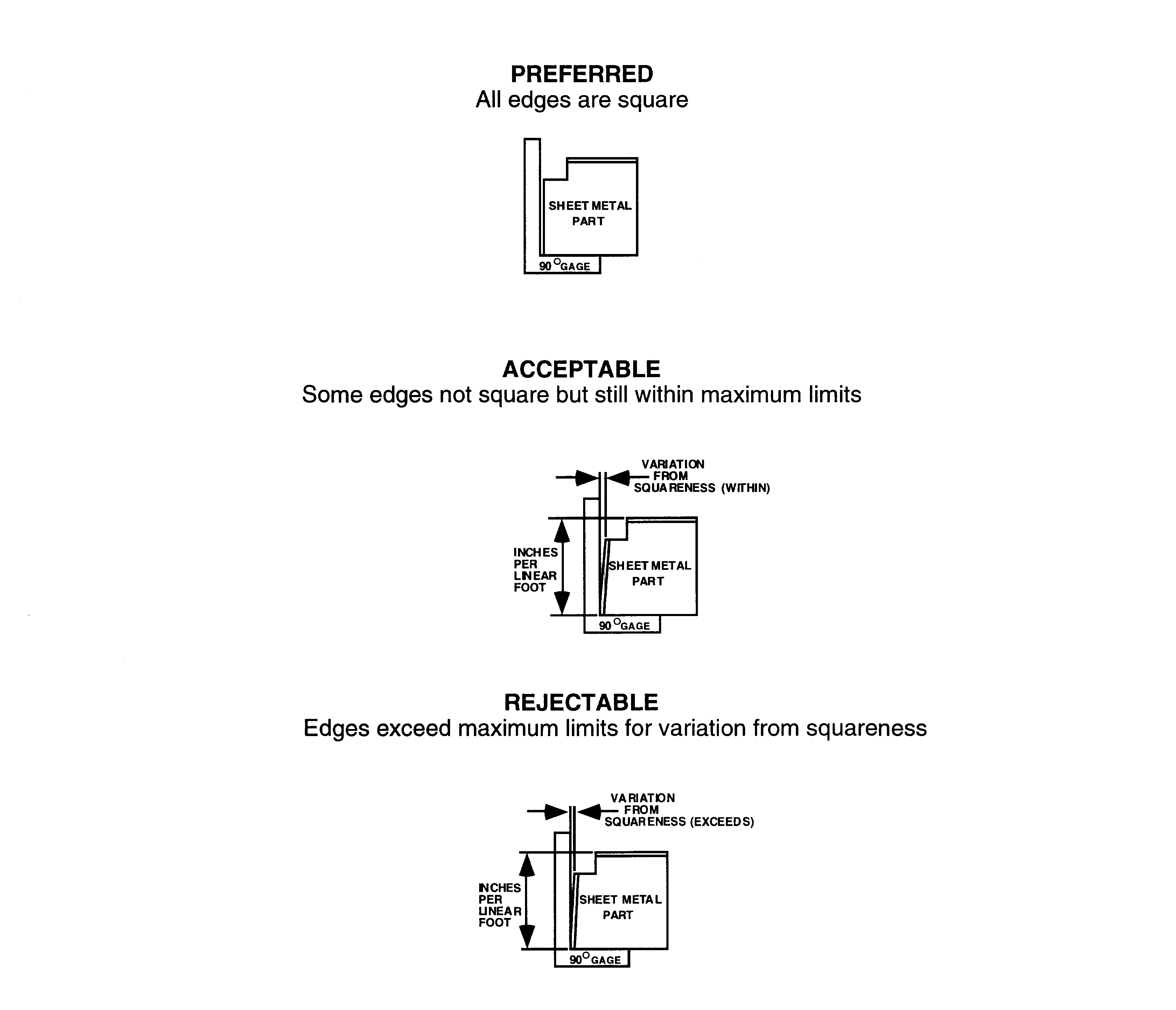
### Grain direction should be called out on the drawing. The graining specification should also be noted on the drawing, noting the grit of the abrasive belt and the type of abrasive. If the direction of the graining is not specified, the grain will run in the longest direction of the part.

## Squareness

### Edges

The variation between sheared or cut edges shall be square within the shown (inches per linear foot)

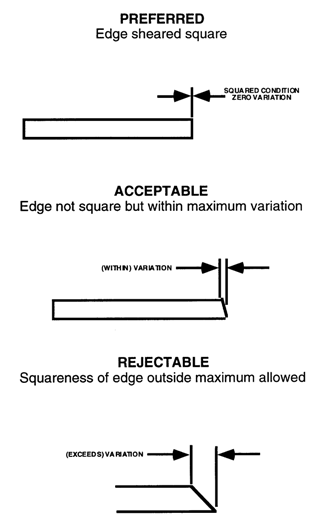
|  |  |  |
| --- | --- | --- |
| **Between** | **Sheared Edge** | **Formed Edge** |
| Sheared Edge | 0.003 | 0.010 |
| Formed Edge | 0.010 | 0.008 |

****

## Shearing

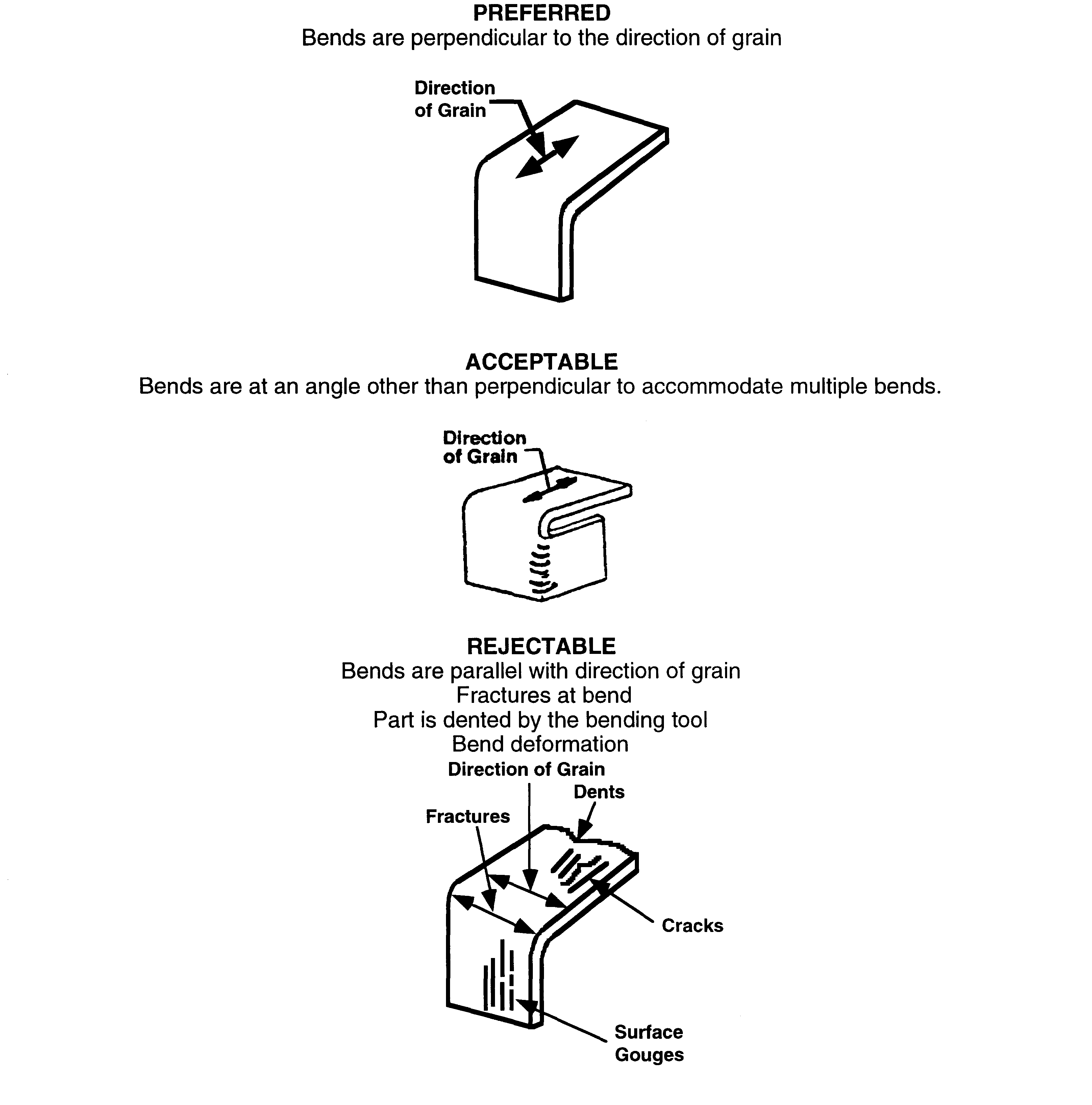
Variation from square of sheared edge

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Material thickness | To .015 | .016 to .032 | .033 to .083 | .084 to .125 | .126 to .187 | .188 to .250 |
| Maximum variation | .004 | .006 | .008 | .012 | .020 | .030 |



## Bending

### Bending shall be made at right angles to the grain whenever possible. No fracturing of the metal at the bend radius is allowed.

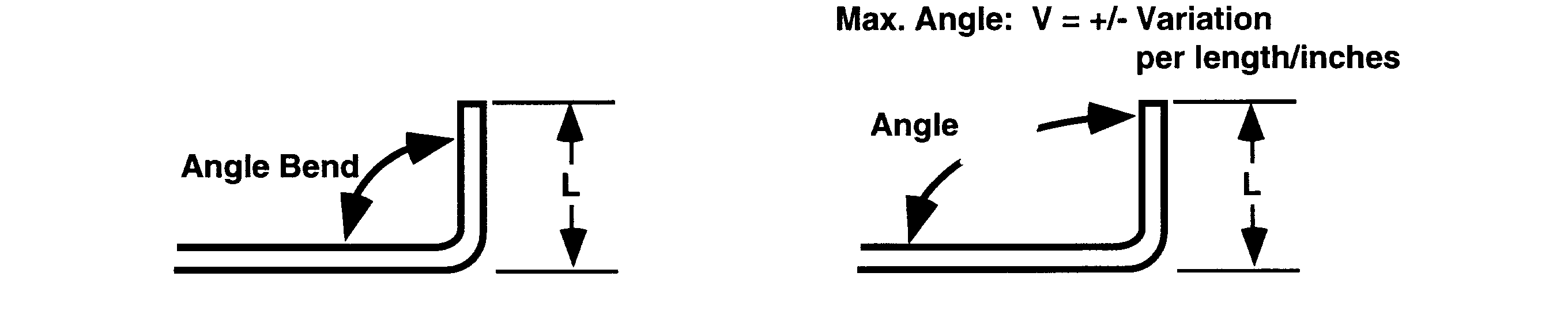


### Angle variation

Maximum variation (inches) at length

|  |  |
| --- | --- |
| Length L | Maximum V +/- |
| To .50”  .51” to 1.50”  1.51”- 6.00”  Over 6.00” | .010”  .020”  .031”  Add .031 per foot |

Any part that has specified angle bends exceeding the maximum variation will be rejectable.



## Self Clinching Fasteners

### Self-clinching fasteners should always be installed per the manufacturer’s recommendation.

### Self-clinching fasteners should be installed after plating but before paint.

### Hardware witness lines from fastener heads are unacceptable on painted surfaces with silkscreen. Lightly sand and dress installed fastener heads so they are not visible after paint.

### Commercial swaged and/or press fit hardware shall meet the manufacturers torque out and push out requirements.

## Corner and Edge Burrs

### Burrs and sharp edges are unacceptable if they can cause injury to personnel and or damage to equipment.

### All corners are required to be rounded or chamfered. If the drawing does not otherwise specify, all corners will have a .010 radius rounding.

## Paint

### Paint chips corresponding to the color specified on the drawing will be used for matching and inspection. Color matching will be done using a spectrophotometer. The spectrophotometer reading from the color chip will be compared against a reading from a known good sample to judge acceptance.

### Parts with a color and/or texture other than specified will be rejected.

### Paint chips or paints from a non approved paint supplier will be rejected

### Parts with scratches or pits that expose base metal will be rejected.

## Powder Coat

### Powder coated parts are to be inspected to the criteria defined within this procedure.

## Plating (Causes for Rejection)

### Scratches that expose base metal will be rejected.

### Any plating defect that adversely affects mechanical requirements or corrosion resistant properties.

### Over arching or finish breaches.

### Plating finish other than specified on drawing.

## Silkscreening

### Inspection will be performed under normal lighting conditions as defined in sections 6.0 of this procedure.

### Cosmetic defects will be inspected per sections 6.0 and 7.0

### Text, lines logo, symbols are to be free of voids, scratches, smudges, cracking blurring and paint runs.

### All letters, numbers and symbols must be legible, clearly distinguishable and not filled with ink. Ink distribution is uniform with no smearing or double images.

### Adhesion tests will be performed based on a sampling plan. The test will be conducted per IPC-TM-650 by applying a four inch piece of 3M 600 or equivalent tape against the marked surface. Once the tape is adhered to the surface, it will be remove with one quick pull. There should not be any evidence of marking ink adhering to the tape.

# Cable and Wire Harness Assemblies

**NOTE: All operators and Inspectors shall be trained to IPC-A-620. Objective evidence of required training shall be maintained and available for review.**

* This section describes the process by which all cables (discrete and non-discrete) shall be assembled and tested by Microchip’s suppliers and subcontractors.
* All Microchip designed cable assemblies must have Microchip’s manufacturing part number, revision letter, supplier’s date of manufacture, lot number and logo/name on the part as space allows. In lieu of marking the part cable, assemblies shall be marked for identification in a bag and tag process. As applicable and directed per manufacturing drawing refer to the Source Control Drawing (SCD), for specific instructions and/or locations for marking the part.
* All completed assemblies must be routed through the suppliers’ and subcontractors’ Final Test and Inspection functions. Inspection shall conform to IPC-A-620 requirements Class 2 unless otherwise noted on the assembly drawing.
* All cable assemblies shall be electrically tested 100% for shorts and opens using automated test equipment when available, refer to IPC-A-620 chapter 19.
* Testing shall demonstrate that connections have been made only between the termination points shown on the engineering drawings and/or specifications (checks for continuity and crimp damage required).
* Evidence of electrical test shall accompany all shipments to Microchip, and be traceable to manufacturing lot or date code at the supplier or subcontractor. This shall be documented in a Certificate of Conformance which is provided to Microchip with shipments.
* Test stamps shall appear on each assembly as space allows, in lieu of actual test stamps a C of C shall be provided indentifying cables have been tested.
* All Cable and Wire Harness Assemblies shall be certified as a UL Recognized (ULr) assembly and ULr marked/labeled accordingly in accordance with UL's wiring harnesses traceability program (UL Category ZPFW2 and ZPFW8).

# Packaging Requirements

* Suppliers shall at all times exercise measures that will ensure and maintain the quality of their product. Suppliers will be solely responsible for product packaging that will guarantee receipt of the highest quality products. Suppliers are responsible for adhering to packaging requirements as flowed down via drawing and/or BOM (Bill of Materials) documentation.
* All non-hermetic Moisture Sensitive Devices that will be subjected to bulk solder reflow process; including plastic encapsulated packages made with moisture-permeable polymeric materials (epoxies, silicones, etc.) that will be exposed to ambient air within Microchip or CM’s premises shall comply with IPC/JEDEC J-STD-033A.
* Failure to comply with these guidelines could result in delaying shipments, rejecting and returning received material.

**PART I – GENERAL REQUIREMENTS**

## Packaging Criteria

### Once a package configuration has been adopted for a particular part or assembly, continue using it for succeeding shipments unless specifically requested by Microchip to change it. The quantity per container of given part must remain constant. If multiple containers are used on the same shipment, the quantity of parts in each container must be the same, except for the last box, which may be the remaining quantity of the lot.

### The packaging is expected to provide protection during shipment to Microchip’s facilities, and during storage and handling up to the first production operation after receipt.

### For strength and function, smaller containers are superior to large, half, or full pallet size containers and are preferred.

### All boxes/containers must be securely closed with reinforced tape.

#### 8.14.2.2 Mechanical Cables, Wires, and Cable Assemblies:  Cable assemblies may be arranged in straight lengths or coiled and tied to maintain the coiled configuration without entanglement.  Cable terminations shall be capped or wrapped to maintain cleanliness and prevent damage.  Branched cable assemblies may also be coiled, but twist or alter the original design configuration is not acceptable.  Critical assemblies must be placed in bags or separated with flexible or rigid pads.

### 

### Deviations to these requirements will be considered on an individual part basis and must be requested in advance of shipment to allow time for investigation.

#### Conductive or anti-static materials will be used as indicated. All PCBA’s are to be shipped in ESD protective bags.

#### Moisture Sensitive Devices (MSD) will be packaged as established in IPC/JEDEC J-STD-033A.

## Shipping Containers

### Full pallet size containers (48” x 40” W) are not acceptable, unless part size demands a large container. In general, container height should not exceed its length.

* All shipments over 45kgs/100lbs shall ship by means of Microchip’s freight carrier if Microchip is paying the freight.
* All shipments under 45kgs/100lbs shall be shipped my means of a small parcel carrier.

### Small containers likely to be handled individually must be limited to 30 gross pounds each whenever possible.

### Corrugated fiberboard is preferred rather than wood. Except for packages customer designed for a specific part/assembly, boxes are desired instead of trays.

### For bagged parts placed within shipping containers, the bags must be of sufficient strength to permit transfer to other containers without rupturing.

### Connectors / Sheet Metal parts, susceptible to environmental contamination, shall be protected by use of clean, sulfur-free neutral packaging material.

### Container sizes, presuming part size permits, must be selected such that when arranged upright (corrugations vertical) on a standard 48” X 40” pallet they do not overhang the edges of the pallet deck by more than 1” per side.

## Identification

### Individual parts must be identified with their designated part number per print. Parts too small or otherwise difficult to mark can be placed in an appropriate container with the Microchip part number, manufacturer’s part number, and quantity marked on the container.

### Moisture Sensitive Devices (MSD) shall be identified as established in IPC/JEDEC J-STD-033A.

### Each shipping container must be identified with the Microchip part number and quantity. All boxes from suppliers/vendors shall have a barcode label on the outside of the box which indicates Microchip part numbers, description and quantity within each box.

### Products being from a CM being shipped to a 3PL site (ex. Sanmina, Manchester NH) shall have a color dot affixed to the container representing the month of manufacturer for FIFO purposes.

## Packing List

### A packing list for each purchase order is to be affixed on the outside of one container in a packing list envelope.

### Packing list must include supplier name, Microchip P.O. number, number of boxes in shipment, Microchip part number, manufacturers’ part number, and total quantity of parts.

## Bill of Lading

### The Bill of Lading must provide an accurate description of the contents and must contain the number of cartons per shipment. Reference Purchase Order(s) and Part Number(s) on each Bill of Lading.

### When the Purchase Order specifies a carrier, any deviation without prior approval by Microchip’s Buyer will subject invoice to debit for freight premiums.

## Palletization

### Palletization is not a preferred method, but is acceptable when circumstances demand.

### If pallets are used, the load is to be securely strapped to the pallet. Edge protectors must be used under straps. Strapping must provide load stability. Shrink or stretch wrap plastic may be applied as an alternative to strapping. If stretch or shrink wrap plastic is used, it must be tightly wrapped to achieve load stability.

### Pallet loads must be uniform and are not to exceed 60” overall height, including pallet. Recommended pallet size is 48 x 40 x 60 high. The top of the load must be flat for safe stacking. Gross weight per pallet must not exceed 2000 lbs.

### Depending on part size, avoid using boxes any larger than ¼ pallet size. It is acceptable to use a common cover or cap over the top of the boxes of one layer on a pallet.

### If in the same shipment, the quantities of individual items are less than a full pallet load, more than one part number may be placed on a pallet.

### Where stacking capability of the palletized load is critical due to weight or part configuration, the maximum safe stacking height should be specified on the containers (ex.: “DO NOT STACK OVER 3 HIGH”).

## Pallets – shipping should be done on a consolidated basis and on pallets when possible.

### Pallet construction should be heavy-duty warehouse grade and structurally sound with all boards in place. No cargo shall over lips the pallet size at all. Where possible strapping is recommended.

## Special Instructions

### Additional packaging instructions appear as “Special Instructions” on the Purchase Order.

**PART II - COMMODITY TYPE**

## Metal Enclosures, Covers, Faceplates, Shelf Plates, Metal Ground Strips, Bars, Rods, Rack Accessories

### Specific Requirements

#### Parts or assemblies with protrusions or critical surfaces must be individually wrapped to protect from damage.

### Interior Packaging

#### Parts that are powder coated, plated, silk-screened, polished or otherwise have finished surfaces must be wrapped with foam, bagged, separated or otherwise protected from scratching and abrasion. Interlocking separators are preferred.

#### Parts must be snug in the package to prevent movement that can cause damage to the parts or lead to package failure.

#### Moisture Sensitive Devices (MSD) shall be packaged as established in IPC/JEDEC J-STD-033A.

### Intermediate Container

#### Thin profile parts often must be packed on edge to prevent warping and to provide ease of unpacking. A tight pack is recommended.

## Screws, Nuts, Bolts, Rivets, Eyelets, Studs, Clinch Nuts, O-Rings, Washers and other Mechanical Fasteners; Hardware Spacers and Standoffs; Ties, Cable Clamps, Transistor Pads, Buttons, Knobs

### Specific Requirements

#### When possible, pack in even quantities. Cartons or other interior containers shall be uniform in size.

#### Do not use antistatic/conductive plastic bags (coating on bags can cause corrosion on some types of hardware).

### Interior Packaging

#### Interior packaging must be sufficient to fully protect the parts. Plastic bags, when used, shall be securely closed to prevent spillage and shall be of sufficient length to permit opening and resealing. Bags must always be packed in shipping containers.

#### Parts subject to corrosion deterioration shall be enclosed in appropriate corrosion inhibitor or barrier material.

#### BULK IN BAG: Non-critical parts may be bulk packed in plastic bags in uniform quantities. Bags shall be of sufficient strength to hold the quantities contained without bursting. The weight of bagged parts must not exceed five (5) pounds. No bulk in box allowed.

## Jack, Terminals, Pins & Plugs, Coax Connectors, Fuse Holders, Switches, Heatsinks

### Specific Requirements

#### Protect all soldered and protruding components using pack material.

### Interior Packaging

#### One of the following interior packaging methods shall be acceptable as applicable, or as specified:

##### Uniform Layers: Connecting devices without leads must be uniformly arranged in plastic trays within corrugated box with padded sleeve, provided sleeve can be removed without spillage of parts. The quantity packed per layer must be uniform and readily visible without further unpacking.

##### Bulk In Bag: When specified, small non-leaded items and accessories such as fuse clips, contacts, adapters, plugs, etc. may be packed bulk in plastic bags in uniform quantities of 25 or 50.

## Printed Circuit Boards/Backplane/Wire Wrap

NOTE: PCBs shall be packaged with desiccants to support longer storage shelf life.

### Specific Requirements

#### Backplane/Wirewrap shall be shipped individually packaged in conductive/anti-static bags/boxes, with anti-static or conductive protective cushioning.

### Interior Packaging

#### Pack Backplane/Wirewrap per section 9.12.1.1 above. Then place groups of boxed assemblies inside larger interior container. Even quantities are preferred. The individual backplane packaging must maintain the original design configuration, and prevent damage to circuitry, components, leads, and any other protruding portions.

#### Packaging must be designed so that boards may be easily and individually removed and replaced without damage to part, package, or operator.

#### All printed circuit boards will be either individually bagged or (if bubble packed) physically separated with plastic or paper sheets. If paper is used, it must be free of sulfur.

#### Limit each bundle to 25 to 30 pounds (lbs), depending on the size of the board. **Change bubble wrap to AMINE-Free coating material.**

#### Bundles or multiple bundles can then be packed in a container.

## Mechanical Cables, Wires, Cable Assemblies

### Specific Requirements

#### Sharp bends and kinks shall not be permitted.

#### When used, spools or reels shall accommodate the bulk of the wire or cable, and the flanges of any spool or reel shall extend beyond the coiled assembly.

## Bulk Wire

### Continuous Lengths: Wire furnished in continuous lengths shall be coiled on reels, spools, or in drums, specifically designed for this purpose. The length of wire shall be as specified on purchase order or specification.

### Interior Packaging

#### Cut or Specified Lengths: Wire cut to specified lengths shall be tied in bundles, in quantities of 50, 100, 200, etc. short lengths (6” or less) may be packaged in plastic bags. Long lengths (bundles) may be loosely coiled to fit within minimum size shipping containers.

#### Mechanical Cables, Wires, and Cable Assemblies: Cable assemblies may be arranged in straight lengths or coiled and tied to maintain the coiled configuration without entanglement. Critical cable terminations shall be capped or wrapped as required to maintain cleanliness and prevent damage. Branched cable assemblies may also be coiled, but twist or alter the original design configuration is not acceptable. Critical assemblies must be placed in bags or separated with flexible or rigid pads.

#### Flat Cable Assemblies: Flat conductor cable assemblies must be packaged flat in straight lengths. When necessary to coil or fan, bending or kinking of the ribbon-like configuration is not acceptable.

## Shock Sensitive Devices:

### Piece parts and assemblies that are shipped to CM’s or Microchip with labels identifying them as Shock Sensitive Devices shall be inspected to insure the Shock Sensor labels have not been triggered. If triggered as described on the label then parts are to be routed to MRB for disposition by Quality and Engineering teams.

### If determined that the parts are to be returned to manufacturer they are to be shipped in identical shipping containers, original if available, with new Shock Sensor labels attached to the outer container.

# Packaging Finished Goods:

## Packaging Materials:

* At the time of shipment, all packaging must be compliant to the latest revision of the European Union RoHS Directive and the China RoHS Regulation.
* Suppliers must be prepared for REACH EC1907/2006 requirements.
* Eliminate the use of adhesives to commingle materials (e.g., foam cushions glued to a corrugated pad).
* Minimize the use of bleached white corrugated board or oyster white board.
* Use water/soy-based inks when printing packaging materials. Ink components that have been FDA/USDA approved are the only acceptable alternatives.
* Use only functional coatings or impregnating that does not adversely affect material recycling. Some coatings that aid resistance to water, grease, or scuffing may be used with no adverse effect on material recycling. Avoid wax based coatings.
* Avoid the use of film laminations and/or cross-linked resins such as urea formaldehyde or polyethylene coated paperboard or solid bleached sulfate (SBS). Exceptions may apply for packaging designed for reuse.
* Unless specifically instructed otherwise, use paper or plastic tape or starch glues in place of staples and hot-melt adhesives on the container's manufacturer joint and/or closures.
* All materials used in packaging shall be marked to facilitate separation and recycling. Where ever possible stamping or marking with material already used in the manufacturing is encouraged. Marking material type with labels made of another material is not allowed. Use of hot stamping, inclusion of marking in mold or marking with a RoHS compliant ink is preferred.

Marking for plastics;



Marking for corrugated boxes;



***The plastic type marking and CB marking are the only markings required by regulation.***

## Inner/Outer Packaging Testing:

* All product packaging must pass ISTA 2A testing using the user defined cycle shown below;

|  |  |  |  |
| --- | --- | --- | --- |
| **Anticipated Condition** | **Time in Hours** | **Temperature in oC ±2oC(oF ±4oF)** | **Humidity %** |
| Tropical (Wet)  then Desert (Dry) | 72  then 6 | 38oC (100oF)  then 60oC (140oF) | 85% RH ±5%  then 30% RH ±5% |

* Mullen Test will be the standard for certifying box strength
* Outer packaging does not need to be ISTA 2A tested.

## Labeling requirements:

* Bar coding is required for Part Number, Sales Order Number, and Serial Number.
* All boxes on a pallet are to be individually labeled.
* All consolidation boxes are to have either a consolidation part number or a label showing all part numbers being consolidated.
* All pallets shall have a label showing what is on the pallet by part number, quantity and serial number.

## Over Pack Dunnage:

* Over packs are to be selected to minimize unused space.
* Use inflatable air bags or bubble wrap as fill wherever possible. Paper is acceptable but not preferred.

## Palletizing:

* Overhang of finished goods over pallet is not allowed.
* Placing a single layer of product packaging on its side on a pallet is allowable but;
  + Must be approved by the customer.
  + Nothing can be stacked upon it and it is to be labeled Do Not Stack.
  + If product packaging marking includes This Side Up not point up it is to be covered.
  + The product(s) must be tightly bound together to prevent damage.
* Edge protectors are required.
* Strapping or shrink wrap must be used to provide stability

## Marking on Packaging:

* Markings below should only be used on products which require their use.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **This Side Up** | **Fragile** | **Protect From Moisture** | **Handle With Care** | **Do Not Stack** |
|  |  |  |  |  |

* Use of Microchip logo on all product packaging is required.
* Microchip logo on over pack boxes is not required.

## Wrapping/Bagging used within Inner packaging:

* ESD compliant bags must be used to wrap product; pink on chassis and silver on PCBA.
* Use of Non-ESD bags may be used on non-ESD sensitive items within the product package.
* Heat Sealing can be used to close bags
* If using desiccant it must be DFM free
* Use Moisture/Shock Indicators only as specified on BOM

# Appendix A: Backplane Testing Flow Chart

Backplane PCB Fabrication   
To IPC-A-6012

Ship To Microsemi

**Phase II:**   
Incoming Inspection of the bareboard fab to IPC-A-600

Final Assembly Test  
(Continuity and Isolation, Components & Connectors)  
(Min. lot sample size 100%)

Backplane

Assembly

**Phase I:**   
Bare Board Test

(1. Continuity and Isolation)  
(2.High Freq. Imp. Char. Test.)   
(3. DC HiPot Test)  
(Min. lot sample size 100%)

Diagnose & Repair

Correct Failure

**Phase III:**

Final Inspection

To IPC-A-610

Limited Repair  
(See section 6.2.1)