Chip Planner User Guide

For Libero SoC v11.7 SP1

Microsemi

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Introduction

The Chip Planner is a Graphical Interface Tool that allows you to create regions, edit regions and make logic assignments to these regions. It is a floorplanning tool used to improve the timing performance and routability of your design by providing maximum control over your design placement.

You may also cross-probe from SmartTime into Chip Planner to browse your design and look into timing problems.

Use Chip Planner to:

- View macro assignments made during layout.
- Assign, unassign, or move macros.
- Lock macro assignments.
- View net connections using a ratsnest view.
- View architectural boundaries.
- View and edit silicon features, such as I/O banks.
- Create Regions and assign macros or nets to regions (floorplanning).
- View logic placement and net connections to investigate timing problems together with SmartTime's Cross-Probing feature

You must first run Synthesis and Compile Netlist on your design before invoking the Chip Planner. If you don't, Libero runs Synthesis and Compile Netlist first before opening Chip Planner. You may invoke the Chip Planner for floorplanning after running Place and Route to improve routability and remove congestion.

When floorplanning, you analyze your design to see if certain logic can be grouped within regions. Placement regions are especially useful for hierarchical designs with plenty of local connectivity within a block. If your timing analysis indicates several paths with negative slack, try grouping the logic included in these paths into their own regions. This forces the placement of logic within the path closer together and may improve timing performance of the design.

Chip Planner and PDC Commands

The Chip Planner is an interactive tool for floorplanning. The floorplanning changes you make in the Chip Planner are saved as PDC (Physical Design Constraints) commands in PDC file(s). Any interactive floorplanning actions in Chip Planner have corresponding PDC commands which can be made part of a constraint file for Place and Route. For details of PDC commands, please refer to the PDC command UG (LiberoSoC > Help > Reference Manual > PDC Commands User Guide).

Supported Families and Platforms

The Chip Planner supports the SmartFusion2, IGLOO2 and RTG4 devices and run on Windows and Linux.

Invoking Chip Planner

When you first create a Libero SoC project, the design flow option you select for the project determines the way Chip Planner is accessed. There are two design flows available in Libero SoC:

- Classic Constraint Flow Option
- Enhanced Constraint Flow Option, which has a single centralized Constraint Manager to manage all design constraints for the design.

Invoking Chip Planner (Classic Constraint Flow)

If you have selected the Classic Design Flow when you first create the Libero SoC project, invoke Chip Planner from the Design Flow Window (**Design Flow Window** > **Edit Constraints** > **Chip Planner** > **Open Interactively**) or double-click Chip Planner in the Design Flow window.

Note: AYou must have first completed successfully the Synthesis step and Compile step before Chip Planner can be opened. If you don't, Libero SoC executes these steps for you before it opens Chip Planner.

PDC files in Classic Constraint Flow

When Chip Planner opens, only the PDC constraint file(s) marked "Use For Compile" are loaded into the Chip Planner for reading. PDC constraint files in the project not marked as such are ignored by Chip Planner.

When you make an I/O or floorplanning change in the Chip Planner, commit and save, PDC files are created: a <root>_io.pdc for I/O changes and a <root>_fp.pdc for floorplanning changes.

The <root>_io.pdc files is located in the <proj>\constraints\io folder.

The <root>_fp.pdc files is located in the <proj>\constraints\fp folder.

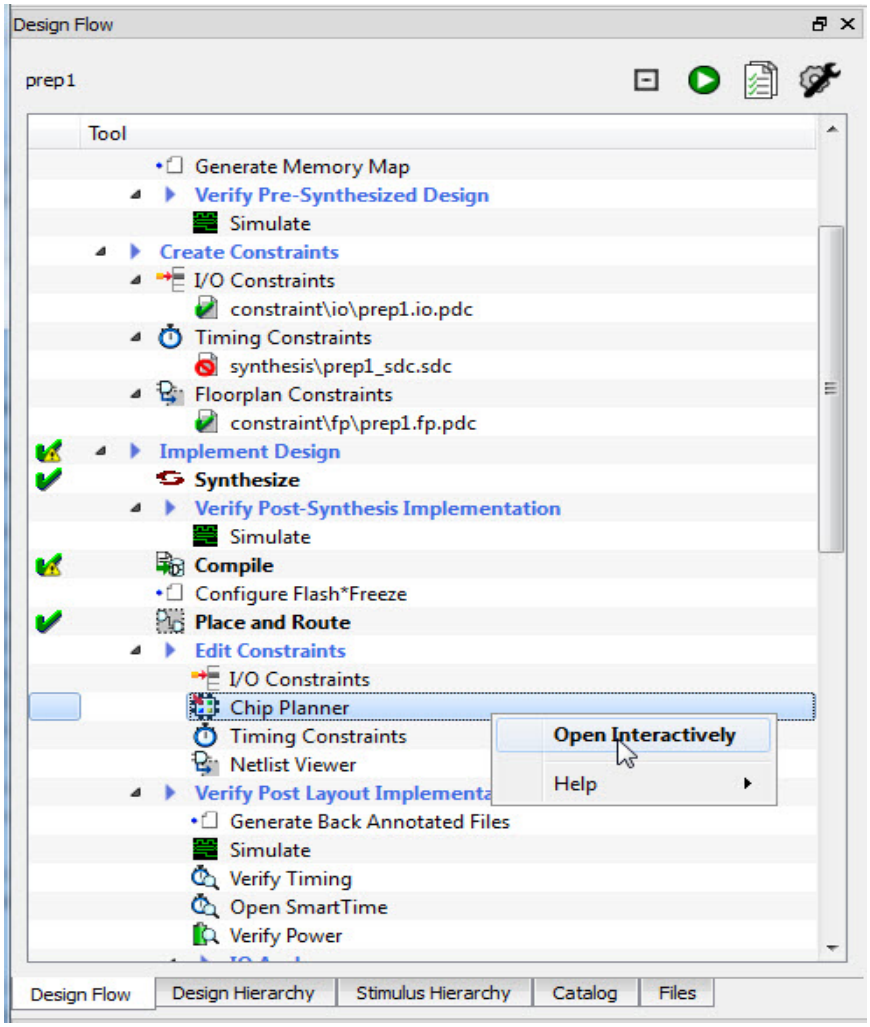

***Figure 1* • Chip Planner Invoked from Design Flow Window (Classic Constraint Flow)**

Invoking Chip Planner (Enhanced Constraint Flow)

If you have selected the Enhanced Constraint Flow option when your first create the project, invoke Chip Planner from the Constraint Manager (**Design Flow window** > **Manage Constraints** > **Open Manage Constraints View** > **Constraint Manager** > **Floor Planner > Edit with Chip Planner)** or double-click **Chip Planner** under Edit Constraints in the Design Flow window**.**

Note: You must have completed the Synthesis or Compile step before invoking Chip Planner from the Constraint Manager. If you don't, a pop-up message appears to remind you the need to run these steps first.

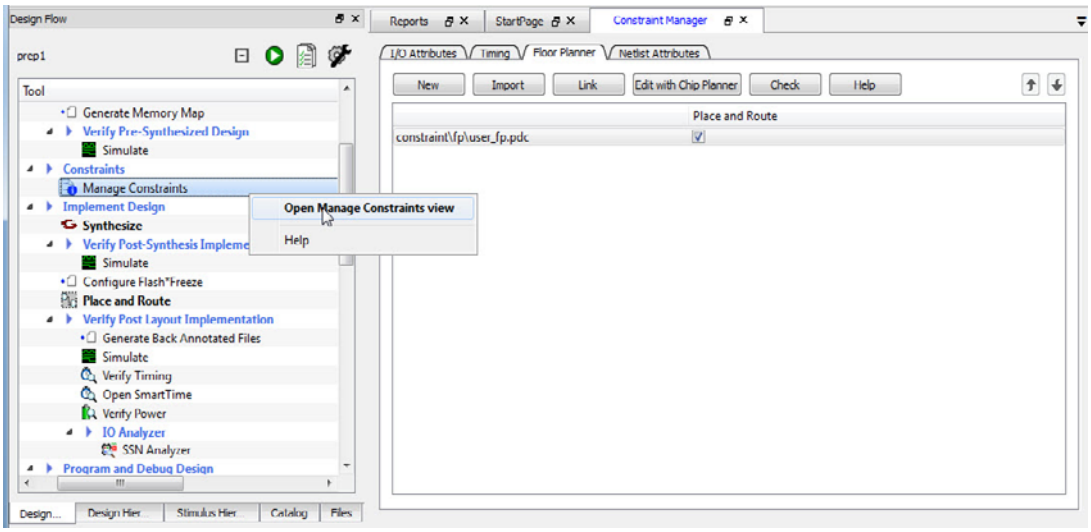

***Figure 2* • Chip Planner Invoked from Constraint Manager (Enhanced Constraint Flow)**

PDC Files in Enhanced Constraint Flow

When Chip Planner opens, only the PDC file(s) associated with Place and Route are loaded into the Chip Planner for reading. PDC files in your project not associated with Place and Route are ignored.

When you make an I/O or floorplanning change in the Chip Planner, commit and save, the change is saved to a *.pdc file that you have set as target in the Constraint Manager. If no PDC constraint file is set as target, the change is written to a new user.pdc file. When the change is related to floorplanning, the user.pdc file is displayed in the Floor Planner tab. When the change is related to I/Os, the user.pdc file is displayed in the I/O Attributes tab.

The I/O PDC files are located in the <proj>\constraints\io folder.

The Floorplanning PDC files are located in the <proj>\constraints\fp folder.

Chip Planner Splash Screen

The Chip Planner Splash Screen appears when it is invoked.

***Figure 3* • Chip Planner Splash Screen**

Chip Planner, I/O Editor and Multiview Navigator

The Chip Planner, I/O Editor and MultiView Navigator (MVN) have access to and write to the same PDC file(s). When two or more of the three tools are opened, making and saving changes (from any one tool) is not allowed. This is to prevent the user from inadvertently overwriting the constraints in the PDC file(s). A message pops up to alert you to the modification conflict and tells you what tool are opened that needs to be closed.

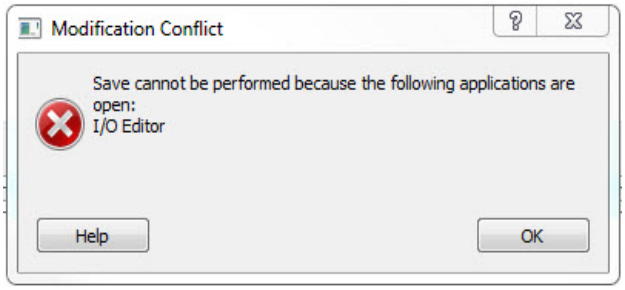

***Figure 4* • Modifications Conflict Message**

To fix the modification conflict, you need to:

1. Close the tools and leave only one open.
2. Make and save the changes in the tool.

1 – Chip Planner Views

When the ChipPanner Graphical Interface launches, it opens with the following windows:

- Design View Window
- Canvas Window
- Log Window
- Display Options Window
- Properties Window
- World Window

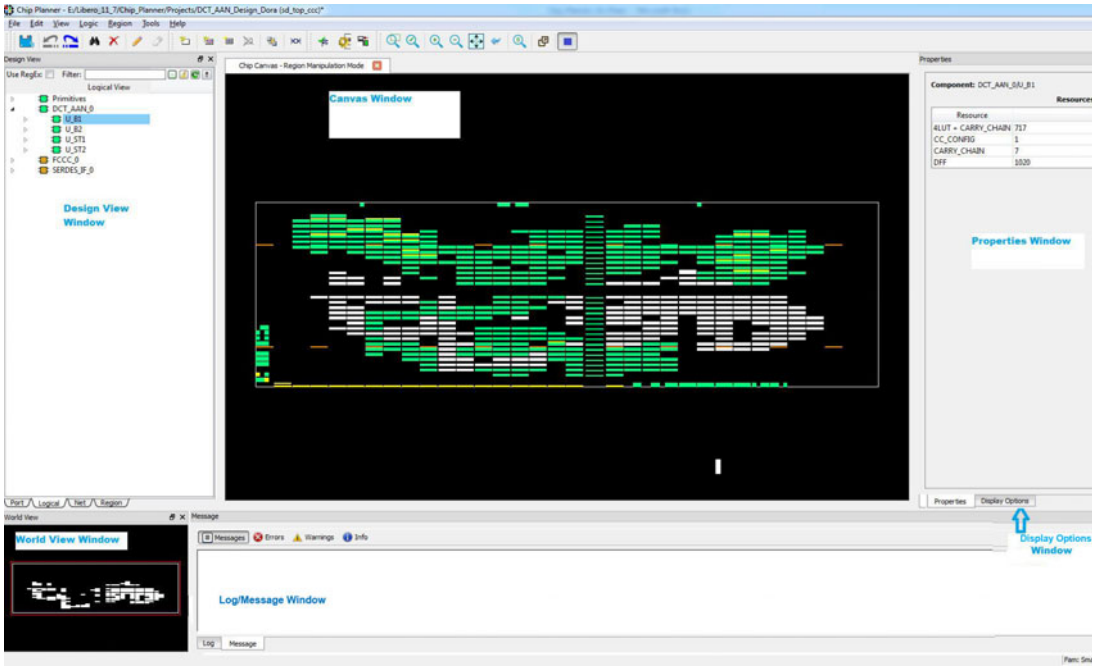

***Figure 1-1* • Chip Planner**

The Design View Window provides the following view tabs for the design:

- Port
- Logical
- Net
- Region
- Block (only when the design instantiates a design block)

All windows, except the Chip Canvas, are docking windows, which can be docked or undocked (floating), turned on or off, moved to the right, left, top, or bottom of the Chip Planner application.

Table 1-1 lists the icons in the toolbar. Hover the mouse on the icon shown on Chip Canvas to see the tooltip.

***Table 1-1* • Chip Planner Toolbar Icons**

Icon	Name	Function
	Commit	Commit and Save will: • Run Chip Planner DRC before saving the changes. • Write/Update the PDC files.
	Undo	Reverse your last action
	Redo	Reverses the action of your last Undo Command
	Find /CNTL F	Clone a Find Window for a specific view (Logical/ Port/ Net,/Region/Block) depending on the view you are in when you click this icon or CNTRL F. Multiple Find windows may be cloned, each with a different set of filtering criteria to give you multiple filtered views of design elements.
	Clear	Clear All Find Trees
	Highlight	Highlight a net, macro or a port
	Unhighlight All	Unhighlights all highlighted selections (macro, net or port)
	Check Design Rules	Runs the Prelayout Checker, a preliminary check of the netlist for possible Place and Route issues.
	I/O Bank Settings	Sets the I/O bank to specific I/O Technology
	Auto Assign I/O Bank	Runs the Auto I/O Bank and Globals Assigner. Assigns a voltage to every I/O Bank that does not have a voltage assigned to it and if required, a VREF pin.

***Table 1-1* • Chip Planner Toolbar Icons (continued)**

Icon	Name	Function
	Create Empty	Create an empty user region
	Create Inclusive	Create an inclusive user region
	Create Exclusive	Create an Exclusive user region
	Delete Region	Delete user-created region you have selected
	Region/Macro Toggle Switch	Toggle this switch to select the Macro or the Region in the Chip Canvas. Use this switch when you are switching back and forth between Macro Manipulation Mode and Region Manipulation Mode.
	Show Nets For Macros	Show all nets connected to the Macro. There are usually too many nets attached to the macro. It is off by default.
	Rubber Band Zoom	Rubber Band Zoom - Drag out an area to enlarge/ zoom into
	Rubber Band Select	Rubber Band Select an area to Zoom into. Click in the Chip Canvas and drag the mouse to delineate an area. Release the mouse and all macros inside the delineated area are selected. Works in the Macro Manipulation Mode.
	Zoom In	Zoom In to Chip Canvas
	Zoom Out	Zoom Out of Chip Canvas
	Zoom to Fit	Zoom to fit the Canvas Size

***Table 1-1* • Chip Planner Toolbar Icons (continued)**

Icon	Name	Function
	Zoom to Location	Zoom to a Location Specified by X-Y co-ordinates
	Zoom to fit Selection	Zoom to fit selected macros and ports. When enabled, the view attempts to center the view on the selected and placed ports.
	View Full Screen	View Full Screen. Click to display the full-screen view of the Chip Canvas.

In addition, there are special icons common to all the five views: Port, Logical, Net, Region and Block. A tooltip is available for each icon.

Table 1-2 shows a list of special icons common to all the five views.

***Table 1-2* • Special Icons in the Design View Window**

Icon	Name	Function
	Rename Tree	Rename a Find tree from the default name to a name you specify. Appears in the Find Window only
	Delete Tree	Delete the Find tree Appears in the Find Window only.
	Filter	Select the Type of Filter: Regular Match, Regular Expression or Wildcard Filter
	Collapse	Collapse everything in the hierarchical tree
	Expand Selected	Expand the hierarchical display recursively from the currently selected item. *Note: On large designs when the top is selected, clicking Expand Selected incurs some runtime overheads before the hierarchical tree is expanded recursively.*

***Table 1-2* • Special Icons in the Design View Window (continued)**

Icon	Name	Function
	Clear	Clear the Filter and refresh the tree reflecting no filters applied
	Reapply the Filter	Reapply the Filter and Sort (if any)
	Change Sort Order and Additional Filtering	Change Sort Order (Ascending/ Descending) or Apply Additional Filtering Sort and Filter criteria vary with the view.

The Chip Planner provides the following special keys and hot keys:

***Table 1-3* • Special Keys/Hot Keys**

Hot Keys/Special Keys	Function
CNTL + F	Find/Search function.
CNTL + Z	Undo the last action/command
CNTL + S	Save all Changes
CNTL + Y	Redo last action/command
Home	Scroll to the first selected item in the view
End	Scroll to the last selected item in the view
Tab	scroll to the next selected item in the view
Shift + Tab	Scroll to the previous selected item
CNTL + Q	Exit Chip Planner
CTRL + ++	Zoom In
CTRL + --	Zoom Out
CTRL + 0	Zoom to Fit
CTRL + H	Lock All Macros
SHIFT + CTRL + H	Unlock All Macros
Hold SHIFT + Left_Mouse Click	Select multiple elements in Design View Windows
Hold CTRL + Left Mouse click	Select multiple elements in Design View Windows

***Table 1-3* • Special Keys/Hot Keys (continued)**

Hot Keys/Special Keys	Function
ESC	Unselects all selected items. Removes any pop-up windows
<Right Arrow key>	Selects Element at next level of hierarchy in design flow window
<Left Arrow key>	Selects element at previous level of hierarchy in design flow window.
<Down Arrow key>	Select next element at the same level of hierarchy in design flow window
<Up Arrow key>	Selects previous element at the same level of hierarchy in the design flow window.

Design View Window and View Tabs

When Chip Planner opens, it presents a Design View Window with five view tabs:

- Port
- Logical
- Net
- Region
- Block - only if user blocks (*.cxz files) exist in the design

Each of the view tabs displays a design view. A selection of a design element in one view is reflected in other views. Take for example, when in the Port view you click and select a bus port, the Logical view shows the OUTBUF/INBUF primitives (for the bus) selected and the Net view shows the net (connected to the INBUF/OUTBUF of the port) selected.

Similarly, when a user region is selected in the Region view, the selection is reflected in the Chip Canvas as well.

The Design View Window can be docked and undocked.

Find Window

The Chip Planner provides a Find window for each of the five design views to search for design elements. To open the Find Window, click the **Edit** menu and choose **Clone for Find**. You may also use the **CNTL + F** Hot Key. Multiple Find windows may be created for the same design view (Port/Logical/Net/Region).

When the Find Window opens, it is associated with a specific design view. Only design elements specific to the particular view are displayed. The view name is appended in parenthesis in the window name when it opens.

The Cloned Find Window has the title “Find (<view_name>)” across the top of the window. A cloned Find window has the same features and functionalities as the main view window. You may create multiple cloned Find Windows for each view. Cloned Find windows are floating when they first open and may be resized, moved and docked.

Take for example, when the Find window is invoked in the Logical view, the find window opens with the name Find (Logical View) across the top of the window and the name Find # (Logical View) when there are multiple cloned Find windows for the same View.

You may find multiple find windows useful in floorplanning. Take for example, If you design has both a RAM and a MACC block and you want to filter and select both and display them in the Chip Canvas, you

need to have two Find windows for the logical view, one with the filter based on Macro type > RAM and the other with the filter based on Macro type > MACC.

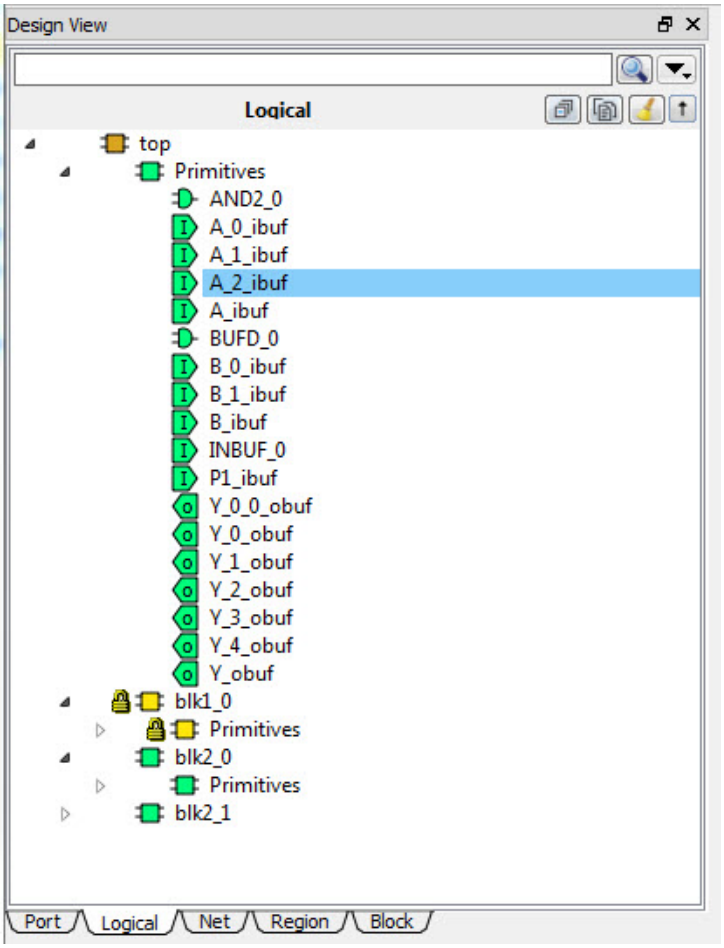

***Figure 1-2* • Find (Logical View)**

Search and Filter

For each of the five views (Port, Logical, Net, Region, and Block) the Search and Filter operations are available. Opens first the Find windows and use the filter field to search for specific design elements. Three different filter options are available from the pull-down list:

- Wildcard filter
- Regular match filter
- Extended posix case insensitive regular expression

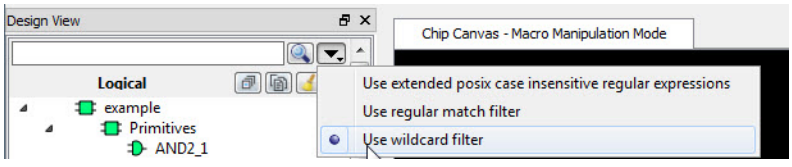

***Figure 1-3* • Filter Options in Search**

Regular Match Filter

The wildcard filter is the default filter. You may use the wildcard character “*” to match any number of characters, the “\” character which makes the following (special) character look like any regular character, or “?” to match any single character. Take for example, when you enter FDDR* in the filter, the FDDR component and all its lower level primitives are displayed.

Wildcard Filter

You may use the “*” character to match any number of characters.

Regular Expression

For details on regular expression syntax please refer to http://www.boost.org/doc/libs/1_43_0/libs/regex/doc/html/boost_regex/syntax/basic_extended.html

Note: All Filtering is case-insensitive.

Port View

The Port View displays a hierarchical view all the Inputs, Outputs and Inouts ports of the design. Both Regular I/Os and Dedicated I/Os are displayed:

- Regular I/O ports - Input/Output/Inout ports that can be changed or re-assigned by the user. These are shown under **I/O Ports** tree.

- Dedicated I/Os - Special-purpose I/Os that cannot be changed or reassigned by the user. These are shown under **Dedicated Ports** tree. Examples are SERDES I/Os or UJTAG dedicated ports

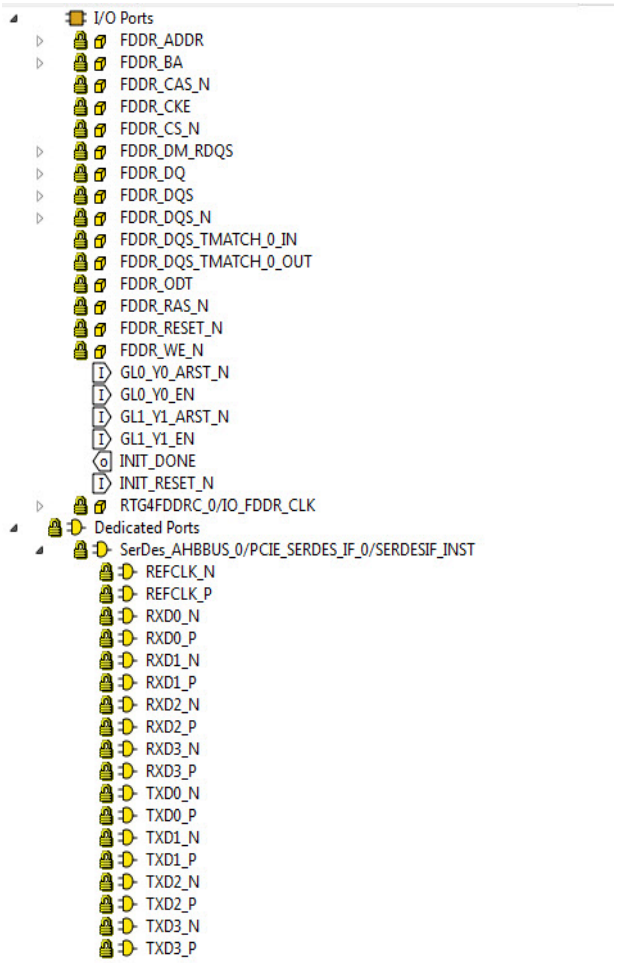

***Figure 1-4* • Port View**

Port Buses

Scalar members of a bus port are grouped under the bus. All bus ports can be collapsed or expanded.

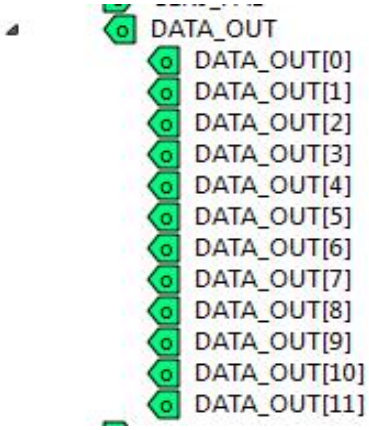

***Figure 1-5* • Bus Port DATA_OUT and its scalar members**

Port Properties

To find out the properties of the port, click to select the port. The property of the port you selected is displayed in the "Properties Window". The selected port is also highlighted in Chip Canvas and the World View.

User Actions in Port View

In the Port View, you can:

- Assign ports to locations - Select a port and drag and drop the port onto Chip Canvas at valid resource location to assign the element to that location. All valid port locations are highlighted once you drag the selected element onto the Chip Canvas.
- Unassign ports from locations - Right-click the port and select **Unassign From Location** to unassign a port.
- Lock Port to location - Right-click the port and select **Lock Placement** to lock selected port to the assigned location. This option is enabled only when the port is already placed in a location.
- Unlock Port from location - Right-click the port and select **Unlock Placement** to unassign the port. This option is enabled only when the port is already locked to a location.
- Assign Port to Region - Right-click the port and select **Assign Macro to Region** to assign a port macro to a region. This option is enabled only if there is a valid region (inclusive or exclusive) created over the I/O port location.
- Unassign Port from Region - Right-click the port and select **Unassign Macro to Region** to un-assign a port macro from a region. This option is enabled only if the port is already assigned to a region.

Sorting

Click the sort icon  to sort the Ports according to ascending or descending order, the type and state of the ports.

Port Filtering

Select Wildcard Filter, Regular Filter, or Regular Expression Filter from the pull-down list. Enter a port name in the Filter Text Box to filter Ports.

Filter According to Port Types

The Port Filter list varies with the family and die. See "Appendix A - Family-specific Macros/ Nets/Ports" for details.

Filter According to Port States

Port States filtering includes:

- Placeable - All I/O which can be placed by user.
- Unplaceable - All I/O which can't be placed by user, example: dedicated I/O.
- Assigned to location- All I/O which can be assigned to location.
- Not assigned to location - All I/O which can't be assigned to location.
- Assigned to region - All I/O which can be assigned to region.
- Not assigned to region - All I/O which can't be assigned to region.
- Locked - All I/O which are locked.
- Unlocked - All I/O which are not locked

Table 1-4 lists the icons and the functions of the ports in the Port View.

***Table 1-4* • Ports and Icons**

Icon	Name	Function
	Input Port	Represents an Input Port
	Output Port	Represents an Output port
	Bidirectional Port	Represents a Bi-Directional port
	White Background	Represents a port that is not placed
	Green Background	Represents a port that is placed
	Blue Tick Mark	Represents an I/O that has been assigned to a region
	Lock Icon	Represent an I/O that is fixed / locked to location

Logical View

The logical view is accessible from the Logical tab of the Design View Window.

It displays a hierarchical view of all the logic inside the chip. The displayed Logic levels are:

- Component - Displays the logic at the component level such as FDDR/CCC/Soft IP cores/ SERDES, etc. This represents the hierarchy in the design.
- Primitives - Displays the lowest level of the hierarchy (hard macro level).You may expand the hierarchy tree to see the lower level logic

Logic Element Properties

Click the component/primitive to find out the properties of the logic element you have selected. The property of the component/primitive is displayed in the "Properties Window". The selected design element is also highlighted in Chip canvas and in World view

User Action in Logical View

Select a design element to:

- Assign elements to locations - Right-click a design element and select **Assign to Location** to assign the element to that location. All valid resource locations are highlighted in Chip Canvas once you drag the selected element onto Chip Canvas. Only a single element can be assigned at a time.
- Unassign element from location - Right-click a design element and select **Unassign from Location.** You can do multiple selections of design elements / components and unassign them.
- Lock element to location - Right-click a design element and select **Lock Placement** to lock selected element to assigned location. This option is enabled only when the element is already placed in a location. You can do multiple selections of design elements / components and lock them.
- Unlock element from location - Right-click a design element and select **Unlock Placement** to unlock or unfix a design element which is already locked to a location. This option is enabled when the element is already locked to a location. You can do multiple selections of design elements / components and unlock them.
- Assign element to Region - Right-click a design element and select **Assign Macro to Region** to assign a macro to a region. This option is enabled only if there is a valid Region created over the required resource location. You can do multiple selections of design elements / components and assign them to a region.
- You can also drag and drop the selected elements directly onto a region in Chip Canvas. If the selected elements are not compatible or over-booked for the desired region, the selection is not assigned to the region and invalid elements are shown in red in the Properties window.
- Unassign element from Region - Right-click a design element and select **Unassign Macro from Region** to unassign a design element/macro from a region. This option is enabled only if the element is already assigned to a region. You can do multiple selections of design elements / components and unassign them from a region.

Filtering

From the pull-down list, select Regular Expression, Wildcard Filter, or Regular Match. Enter a macro name in the Filter text box to filter the design elements.

Sorting

Click the Sort Icon  to sort according to ascending or descending order, the type (Filter by Macro Type) and state (Filter by State) of the logic element.

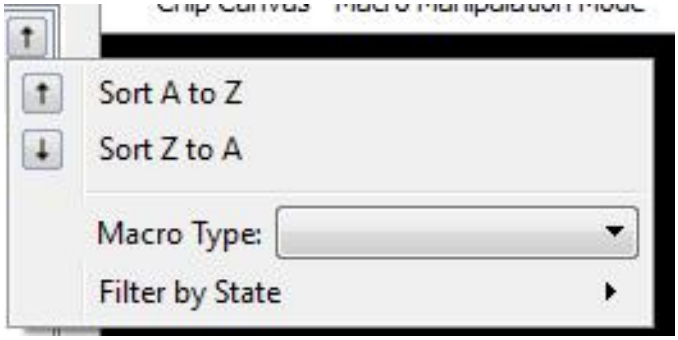

***Figure 1-6* • Macro Filter**

Filtering

From the pull-down list, select Regular Expression, Wildcard Filter, or Regular Match. Enter a macro name in the Filter text box to filter the design elements.

According to Macro Types

Available Macro types are family/die-dependent. See "Appendix A - Family-specific Macros/Nets/Ports" for the list of Macro filters specific to the family/technology of your project.

According to Macro State

The Logical View displays the filter results based on the state of the Logical elements:

- Placeable - All Macro which can placed by user. This option is mutually exclusive with Unplaceable option.
- Unplaceable - All Macro which can't be placed by user. This option is mutually exclusive with Placeable option.
- Assigned to Location - All Macro which can be assigned to location. This option is mutually exclusive with Not assigned to Location option.
- Not assigned to Location - All Macro which can't be assigned to location. This option is mutually exclusive with Assigned to Location option.
- Assigned to Region - All Macro which can be assigned to region. This option is mutually exclusive with Not assigned to Region option.
- Not assigned to Region - All Macro which can't be assigned to region. This option is mutually exclusive with Assigned to Region option.
- Locked - All Macro which are locked. This option is mutually exclusive with Unlocked option.

- Unlocked - All Macro which are not locked. This option is mutually exclusive with Locked option.

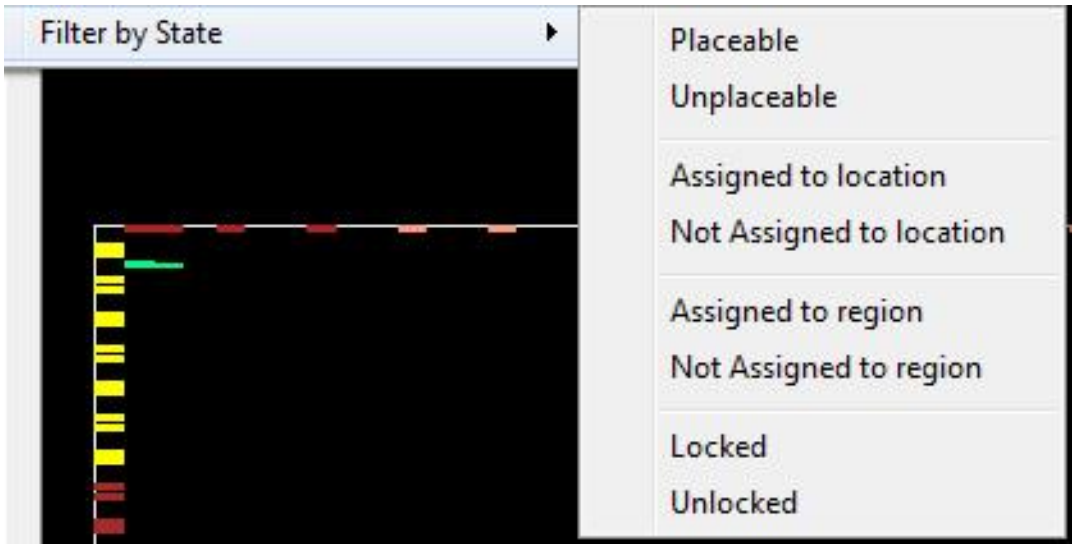

***Figure 1-7* • Macro State Filter**

Table 1-5 lists the Macros as displayed in the Logical View.

***Table 1-5* • Macros in Logical View**

Icon	Name	Function
	Component / Top Level Macro	Represents a Design Component or Top level macro which has a lower level macro.
	Comb / Seq Element	Represents the lowest level element associated with a fabric resource.
	Input Port Macro	Represents a macro associated with an Input port
	Output port macro	Represents a macro associated with an output port.
	Bi-Directional port	Represents a macro associated with a Bi-Directional port
	Global Resource	Represents a macro assigned to Global Resources / Row Global Resources
	Block Element	Represents a design element associated with a block or an IP interface

***Table 1-5* • Macros in Logical View (continued)**

Icon	Name	Function
	White background	Represents a design element which is not placed
	Green background	Represents a design element which is placed
	Blue tick mark	Represents a design element which has been assigned to a region
	Lock Icon	Represents a design element which is fixed / locked to location

Net View

The Net View displays a flattened net view of the design displaying all the nets associated with the design. Shown with each net are the pins connected to the net.

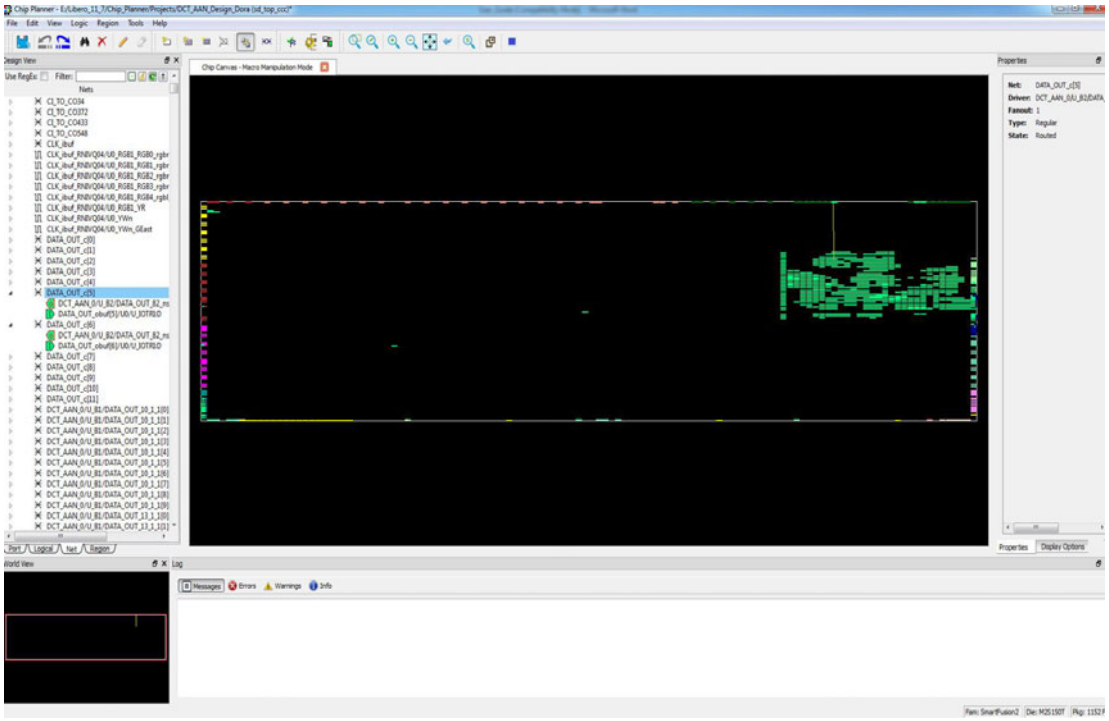

***Figure 1-8* • Net View**

Net Properties

Click to select the net and the net properties are displayed in the "Properties Window". The selected net is also highlighted in Chip Canvas and the World View.

User Actions in Net View

From the Net view, you can:

- Change Net Color - Right-click a net and select **Net Color** to change the net color. This will open a color palette from which you can assign the desired color to the selected net.
- Assign net to Region - Right-click a net and select **Assign net to Region** to assign the driven macros associated to the net to the desired region. This option is enabled only if there is a valid Region created over the required resources. You can do multiple selections of nets and assign them to a region.
- Assign net (with driver) to Region - Right-click a net and select **Assign net (with Driver) to Region** to assign all net macros including driver macros to a region. This option is enabled if there is a valid Region created over the required resources. You can select multiple nets and assign them to a region.
- Unassign net from Region - Right-click a net and select **Unassign net from Region** to unassign net macros from a region. This option is enabled only if the net is already assigned to a region. You may select multiple nets to unassign from a region.

Sorting

Sort the nets in ascending or descending order.

Filtering

Enter a net name in the Filter text box to filter net names. From the pull-down list, select Regular Expression, Wildcard Filter, or Regular Match. You may also filter with criteria specific to nets, such as fanout values, net types, routing status (routed or unrouted).

Filter Criteria based on fanout value

- Max Fanout - Enter a value to display nets with a maximum fanout value.
- Min Fanout - Enter a value to display nets with a minimum fanout value.

Note: Max Fanout and Min Fanout are logical ANDed together. If the Max Fanout has a value of 10 and the Min Fanout has a value of 2, the Net view displays only nets which meet both conditions. In this case, only nets with a fanout range of 2 to 10 are displayed.

Filter Criteria based on net Type

The net type and the filter list is family/die-specific. See "Appendix A - Family-specific Macros/Nets/Ports" for the list of net filters specific to the family/technology of your project.

Filter Criteria based on routing status

- Routed - Displays all routed nets
- Unrouted - Displays all unrouted nets

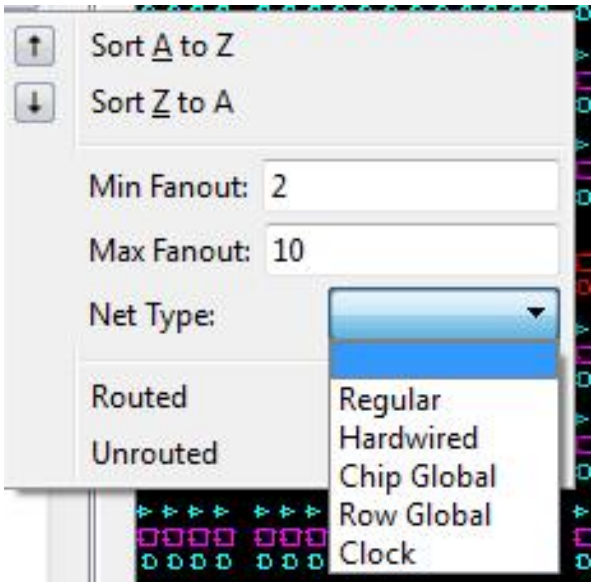

Figure 1-9 • **Net Filter Options**

Table 1-6 lists the icons specific to the net view.

Table 1-6 • **List of Net Icons**

Icon	Name	Function
	Regular/Hardwired Net	Represents a regular or hardwired net
	Global Net	Represents a net that is routed through Chip Global / Row global resources
	Driven Macros	Represents a list of macros which are driven by this net
	Driver macros	Represents a macro which is driving this net
	Blue tick mark	Represents a net which has been assigned to a region

Global Nets

A global net is a net which uses Global routing resources for routing a signal from source to destination logic clusters. These include Chip Globals Resources / Global Buffers (GB), Row global resources /row global buffers (RGB), Half-Chip Globals (HGB in case of RTG4). Clocks, Async Reset and nets with high-fanout are typically routed through these global routing resources. Global signals (G[n:0]) reach the logic clusters through row global signals (RG[7:0]) generated by an associated row global buffer (RGB). RGBs

do not exist in the user netlist. They are inferred and inserted by the layout tool. Depending on the placement of the design elements, it distributes the fanout of the global nets across multiple RGBs. Net View shows this break-up for such global nets.

An example of a Global Net routed through GB[0] with a fanout of 2968 is shown in the Properties Window below.

Global Nets Information

	From	GB Location	Net Name	Fanout
1	GB[0]	(290, 72)	CLK_ibuf_RNIVQ04/U0_YWn	2968
2	GB[12]	(306, 72)	RST_ibuf_RNIUR47/U0_YWn	512

***Figure 1-10* • Global Net Information in Properties Window**

The Chip Canvas View of the Global Net is shown in Figure 1-11. The nets are shown directly connected to the Chip Global GB[0].The Properties Window shows the Chip Global GB[0] to have a fanout of over 1,300 (to the clusters). Note this view is displayed only when the option "Consolidate Globals" in the window is enabled.

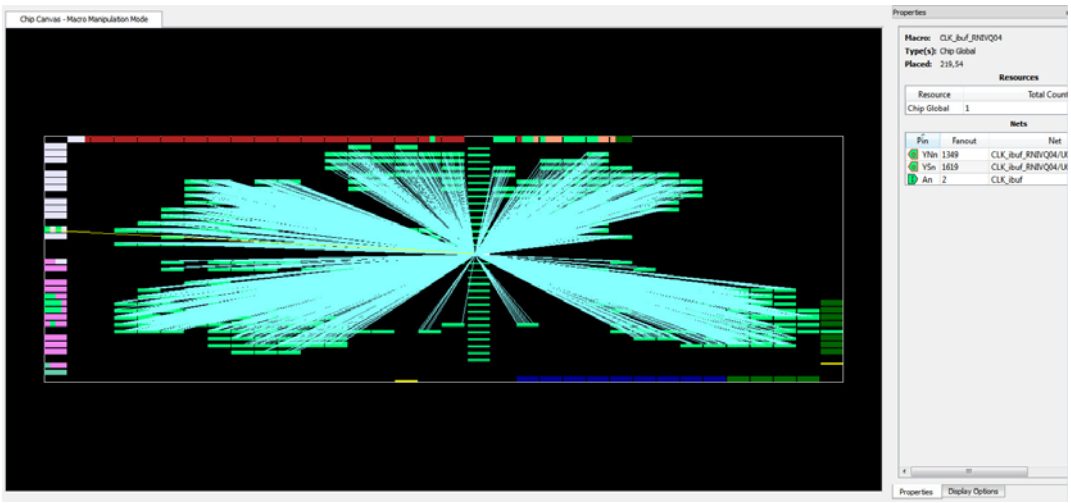

***Figure 1-11* • Chip Canvas View with Consolidated Globals Turned On**

When the Consolidate Global button is turned off, the Chip Global is shown to connect to Row Globals which drive the clusters (Figure 1-12). The Properties Window shows the Chip Global GB[0] to have a fanout of 15 (to the Row Globals RGBs).

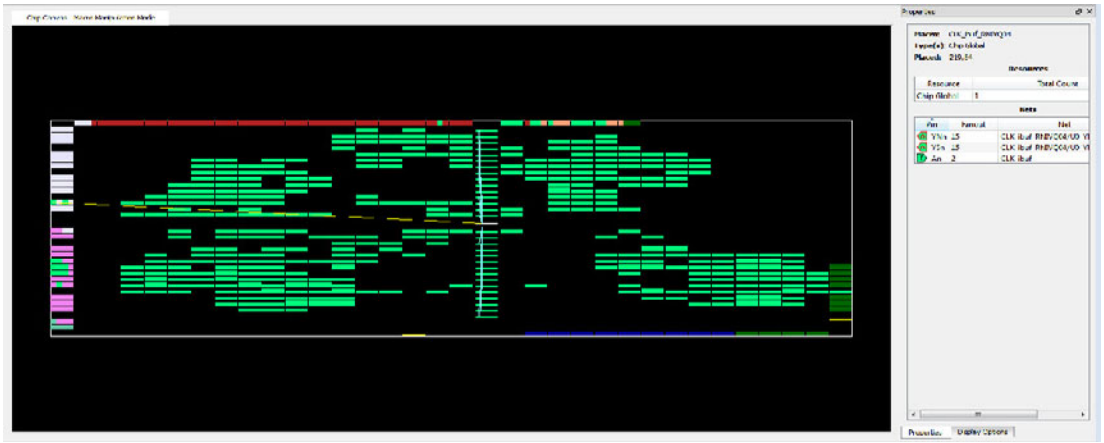

***Figure 1-12* • Chip Canvas View with Consolidate Globals Turned Off**

Region View

The Region View displays the regions you have created and all the Components, Macros and Nets assigned to the region. When you create a region, by default the region is named UserRegion1, UserRegion2 and so on. When you make a selection in the Region View, the property of the Region you select is displayed in the "Properties Window". When you select an item in the hierarchical tree display, all sub-items are selected.

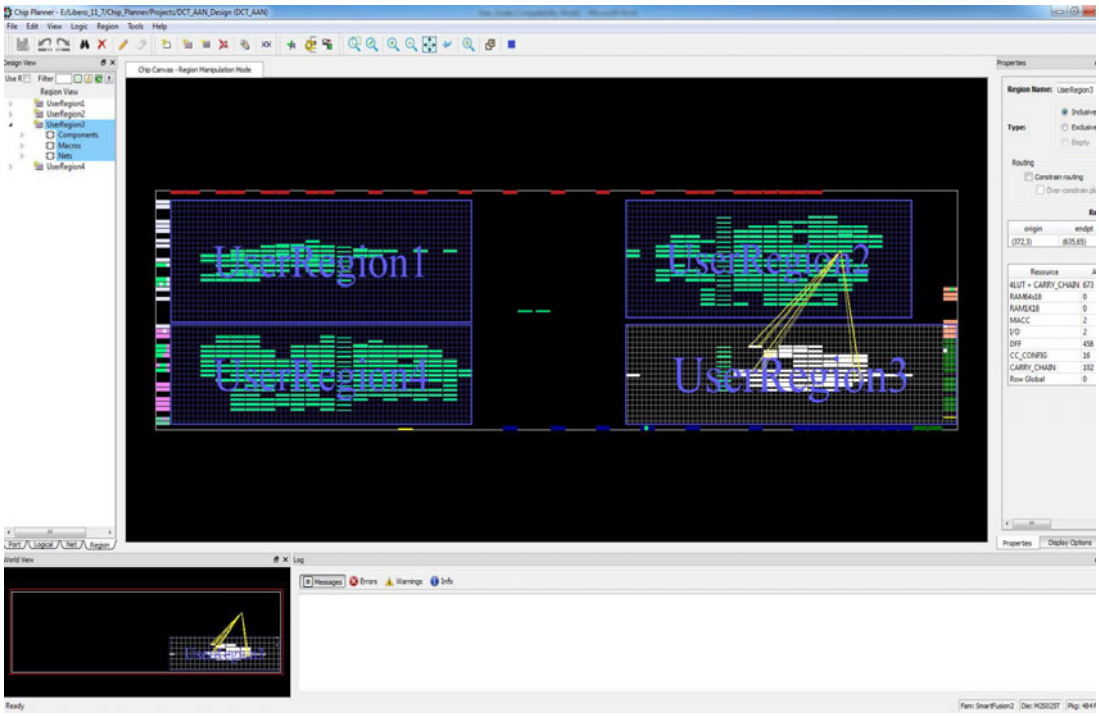

***Figure 1-13* • Region View**

User Regions and Region Types

Three different types of regions are available for creation:

- "Inclusive Region"
- "Exclusive Region"
- "Empty Region"

User Actions on Regions in Chip Canvas

You may select a region in the Regions View to:

- Delete - Deletes a selected region.
- Clone - Clones a selected region.
- Rename - Renames a selected region.
- Merge - Merges two or more regions. This option is enabled if there are more than two regions selected.
- Assign macros inside Region - Assigns macros which are part of region area assigned to selected region.
- Unassign From location - Unassign all design elements that are part of selected region from their placed locations.
- Lock Placement - Locks all macros that are part of selected region.
- Unlock Placement - Unlocks all macros that are part of selected region.
- Unassign macros from Region - Unassigns assigned macros from selected region.
- Unassign Component from Region - Unassigns assigned components from selected region.
- Unassign Net from Region - Unassigns assigned nets from selected region.

Region Properties

Click the region in the Region View and the property of the region you have selected is displayed in the "Properties Window". The selected region is also highlighted in the Chip canvas and the World View.

Region Filtering

Enter a region name in the Filter text box. From the pull-down list, select Regular Expression, Wildcard Filter, or Regular Match filter.

Region Sorting

In addition to ascending or descending order display, a filter is available for the Region View to display user regions based on region types:

- Inclusive - shows all inclusive regions
- Exclusive - shows all exclusive regions
- Empty - shows all empty regions

***Figure 1-14* • Region Filter**

Table 1-7 lists Region View icons.

***Table 1-7* • Region View Icons**

Icon	Name	Function
	Inclusive	Represents an inclusive region
	Exclusive Region	Represents an exclusive region
	Empty Region	Represents an Empty region
	Nets	Represents a net associated with a region.
	Component / Top Level Macro	Represents a Design Component or Top level macro which have lower level macro.
	Comb / Seq Element	Represents the lowest level element associated with a fabric resource.
	Output port macro	Represents a macro associated with an output port.
	Input Port Macro	Represents a macro associated with an Input port

***Table 1-7* • Region View Icons (continued)**

Icon	Name	Function
	Green background	Represents a design element which is placed
	Blue tick mark	Represents a design element which has been assigned to a region
	Lock Icon	Represents a design element which is fixed / locked to location

Block View

The block view displays the low-level design blocks (*.cxz files) you have imported into the Libero SoC project. This tab appears only if and when design blocks exist in the project. These low-level design blocks may have completed the place-and-route step and have met the timing and power requirements of the design block. For details, refer to the SmartFusion2, IGLOO2, and RTG4 Block Flow User's Guide (**Help > Reference Manuals**).

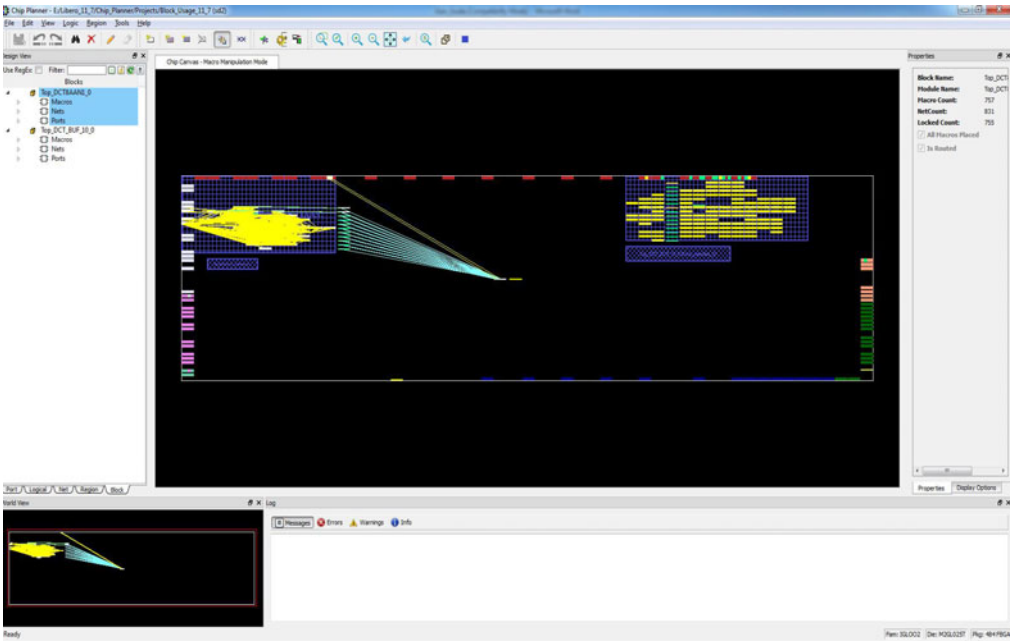

***Figure 1-15* • Block View**

The Block view displays all the design blocks in the project and for each design block the following design elements:

- Macros
- Nets
- Ports

Block Properties

Click to select the block in the Block View and the property of the block is displayed in the "Properties Window". The selected block is also highlighted in Chip Canvas and the World View.

Block Filtering

Enter a block name in the Filter text box to filter blocks. From the pull-down list, select Regular Expression, Wildcard Filter, or Regular Match filter.

You can sort the blocks in ascending or descending order.

Properties Window

The Properties Window displays the properties of the design elements. What is displayed in the Properties Window is dependent on what is selected in the design view.

Properties of Logical View Elements

The Properties Window displays the properties of Component and Macro when they are selected in the Logical View. Properties displayed may include the following depending on the type of design elements:

- Macro/Component Name - Full Macro or component name based on selection in logical view.
- Cell Type - Resource type based on design element selection.
- Placed (Location)- X-Y coordinates where device element is placed.
- Resource Usage Table - A Table showing resources based on component and macro selection.
- Region Attached Table - A Table showing region to which selected macro / component is assigned.
- User region (if any) it is attached to.
- Nets Table - A Table showing Pins and nets which is associated with selected macro along with fanout value.
- Locked/Unlocked (Placement) - Selected port is locked or not.
- Port - Port name to which I/O macro is assigned (only shown for I/O port macros).
- I/O Technology Standard - I/O Technology which is associated with selected I/O macro (only shown for I/O port macros).
- I/O Bank- I/O bank to which selected I/O macro is assigned (only shown for I/O port macros).
- Pin (Package Pin) - Pin to which macro is assigned (only shown for I/O port macros).

Note: Not all properties in the list are displayed. The list of displayed properties varies with the type of design element selected in the Logical View.

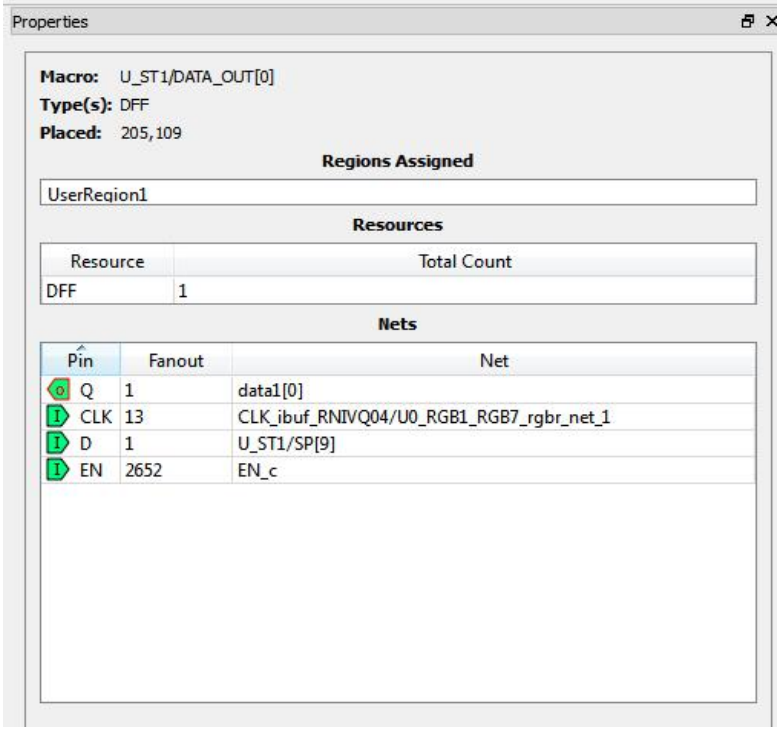

***Figure 1-16* • Properties Window of Logical View**

Properties of Port View Elements

When a design element (I/O Bus or Scalar I/O) is selected in the Port View, the Properties Window displays the properties of a Bus (for I/O bus) or a Macro (for scalar I/Os)

For I/O bus, the Properties Window displays:

- Resource Usage Table - Shows all resources associated with selection.
- Ports Table: Displays a table with I/O Bank, I/O Technology Standard, Package Pin and Port Names of each individual member of the bus.

For scalar I/O ports, the Properties window displays the Macro information:

- Port Name - Full Name of the selected port.
- Macro - Name of the macro associated with selected port.
- Port Type of selected I/O.
- Locked/Unlocked (Placement) - Selected port is locked or not.
- Pin (Package Pin name) - Pin name to which selected port is assigned.
- I/O Technology Standard - I/O standard which is associated with the port.
- I/O Bank - I/O Bank associated with selected port.
- Resource Usage table.
- Nets Table - A Table showing Pins and Nets associated with selected port along with fanout value.

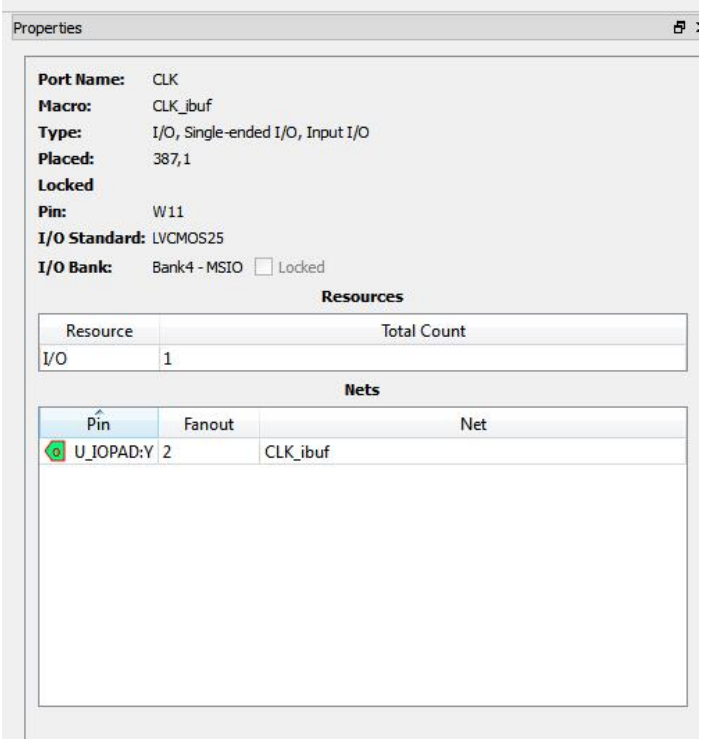

Figure 1-17 • **Properties Window of Ports View**

Properties of Nets

For Nets selected in the Net view, the Properties Window displays the following:

- Net Name - Full name of selected net
- Driver Name - Macro which is driving selected net
- Fanout - Fanout value of selected net
- Type of Net: Regular/Hardwired/Global for selected net
- State: Routed or Unrouted net

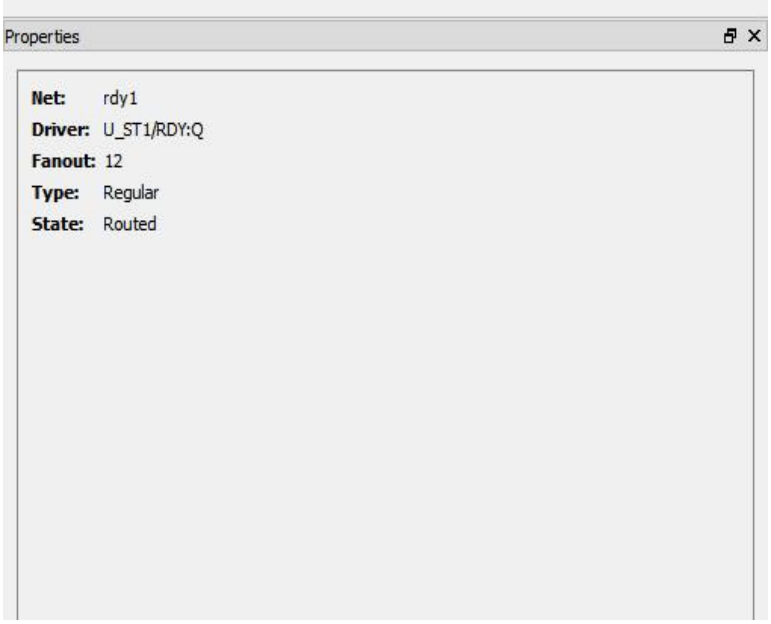

***Figure 1-18* • Properties of Net**

Properties of Region

Region properties are displayed in the Properties window when a user region is selected in the Chip Canvas or in the Region View.

The properties window for a region displays the following:

- Region Name - By default, the regions are named UserRegion1, UserRegion2 and so on when first created. You can change the region name by editing the Region name text box from properties window.
- Type of Region (Inclusive/Exclusive/Empty)
- Routing Requirements
  - Constrain routing - Instructs the Place and Route tool to apply routing restrictions (in addition to Placement restrictions) to the user regions. Refer to Figure 1-19 • Properties of Region for details.
- Region Extents - displays the X-Y co-ordinates of the origin (lower left corner) and the endpoint (upper right corner) and the width and height of the region.
- Resources in the Region - displays the logic resources in the region, including used resources and total available resources and a percentage of used resources relative to the total resources.

A percentage of over 100 means overbooking, which is not allowed. The overbooked resource is highlighted in red.

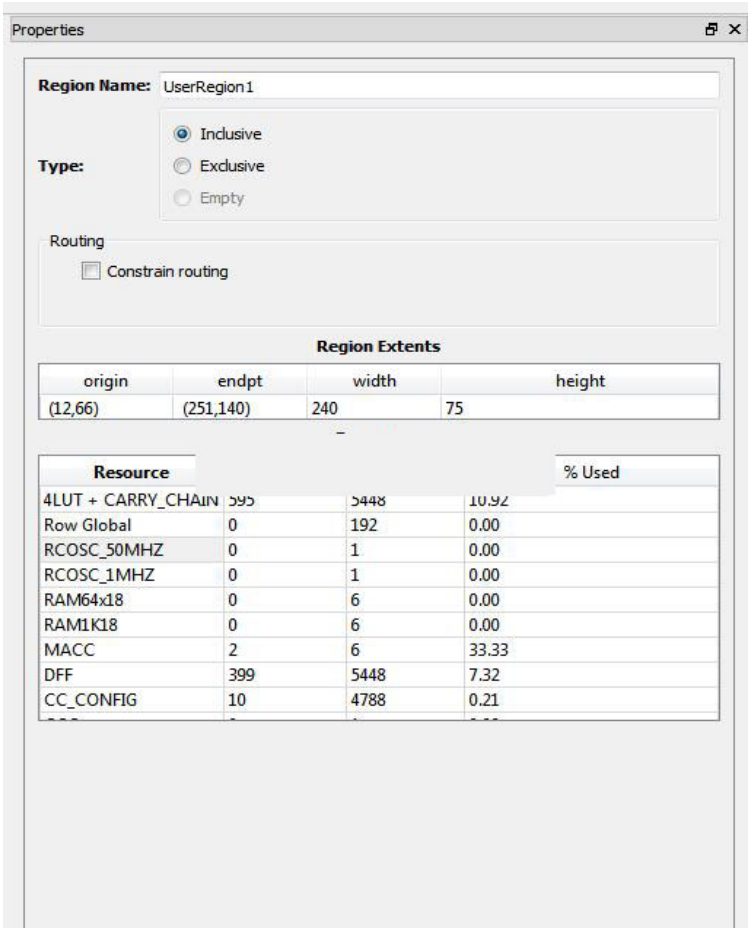

***Figure 1-19* • Properties of Region**

Properties of Blocks

When a block is selected in the Block View, the Properties window displays:

- Block Name - Name of the selected block
- Module Name - Name of the block module
- Macro Count - Total number of macros in the block
- Net Count - Total number of nets in the block
- Locked Count - Total number of Locked macros

In addition, it specifies whether all the macros are placed and/or routed.

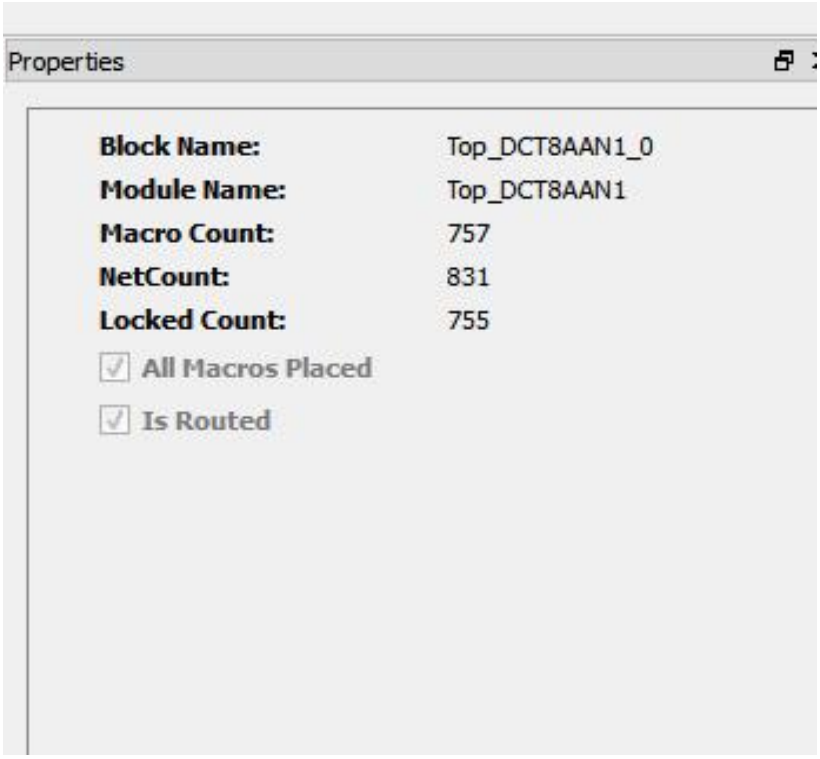

Figure 1-20 **• Properties of Block**

2 – Display Options Window

The Display Options Window allows you to customize the layout and the color settings for design elements on the Chip Canvas to meet your personal preferences.

There are two default layers and colors settings group that are provided with Chip Planner:

- System
- Gray_Scale

By default, Chip Planner launches with “System” layers and colors settings group for the Device (Silicon feature) and the Design Elements. These are the System Default Settings.

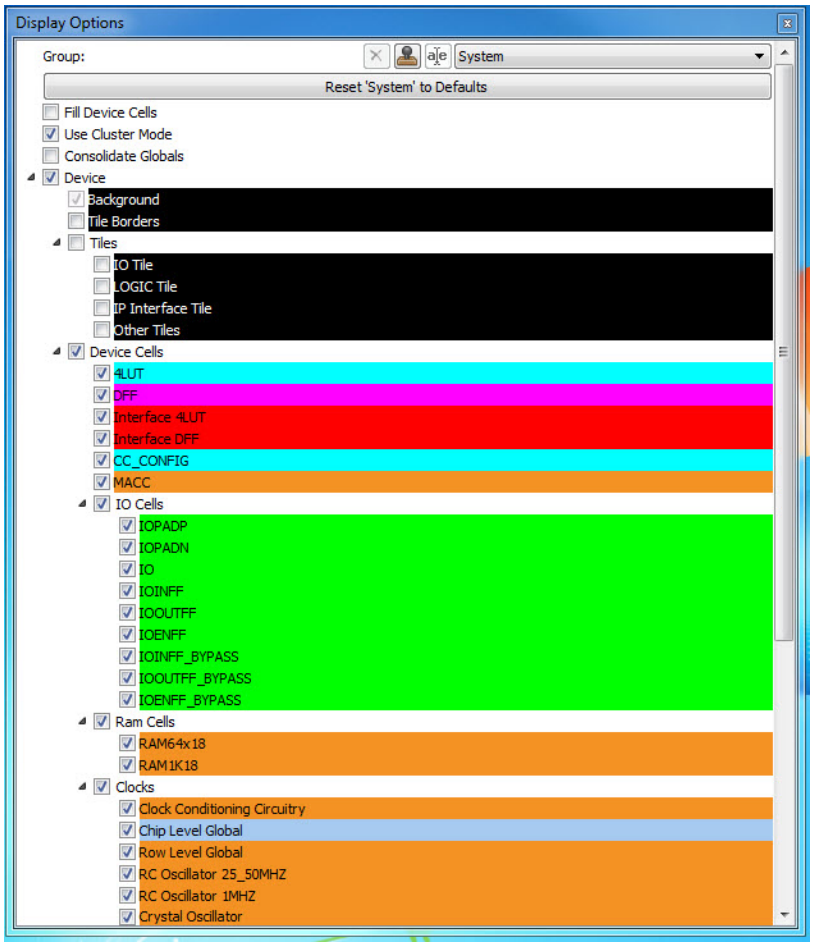

***Figure 2-1* • Default Color Setting for Device (Silicon Hardware) - Settings shown are for M2S090TS die**

The device color setting is a hierarchical view. You may expand each group to see the lower level items and see the default color setting for each. The device cell types, IO banks are die-dependent and reflects the available hardware components for the selected die.

Similarly the color setting for the Design Elements are displayed in a hierarchical view. Expand the group to see the default color setting for each lower level design element.

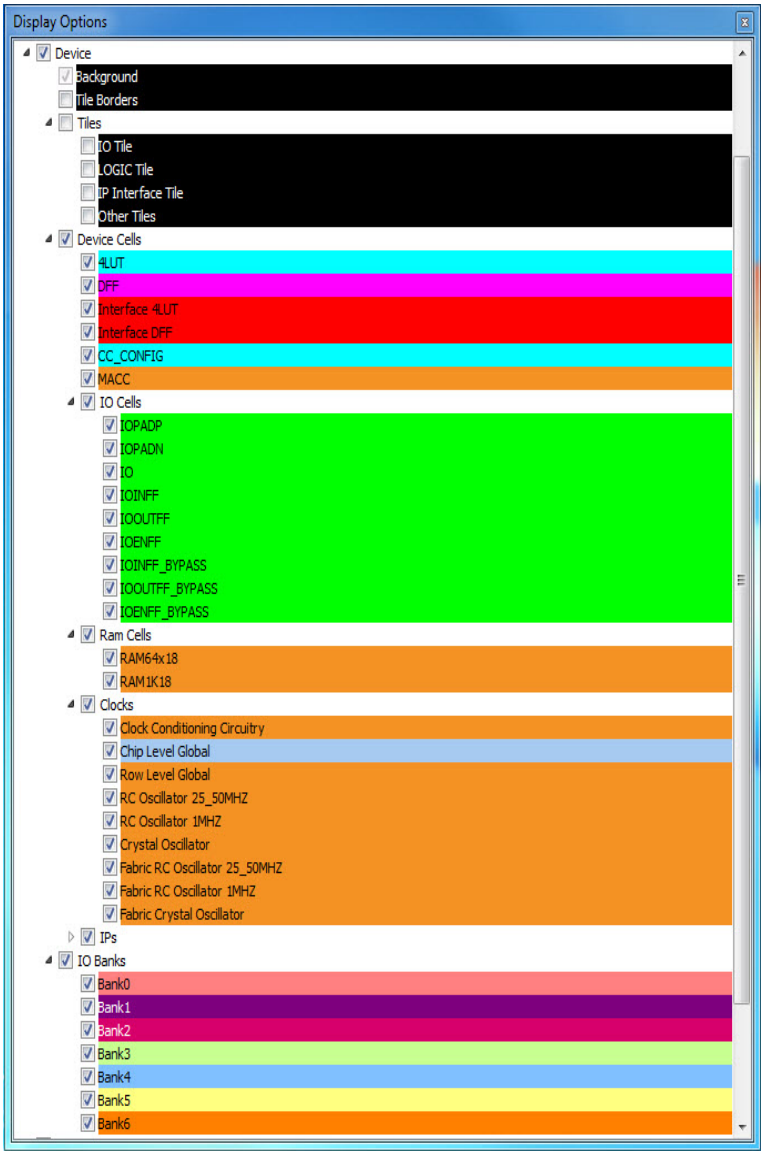

***Figure 2-2* • Default Color Settings for Design Elements- Settings shown are for design implemented on M2S090TS die**

Changing Color Settings

To change the color setting for a device or design element from the default setting:

1. Right-click the color for the element.
2. In the Set Color Dialog Box, move the Cross across the color spectrum to the color you prefer.

3. Click **OK**.

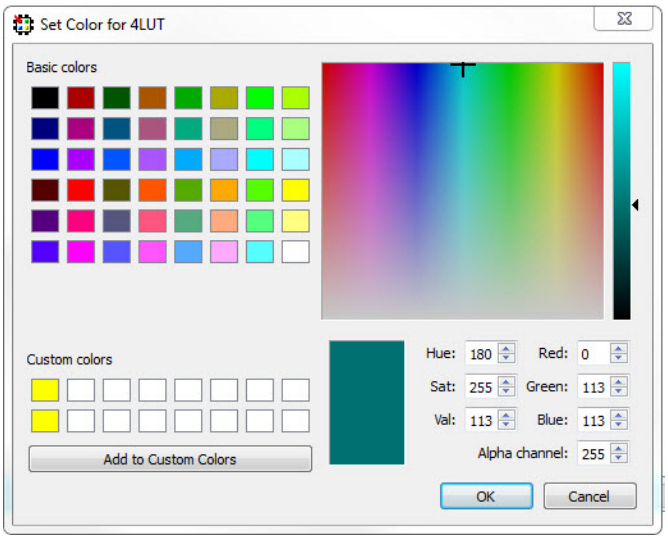

***Figure 2-3* • Set Color Dialog Box to Change Color**

Displaying an instance on Chip Canvas using Display Options Window

You can use the checkbox provided against each menu item.to select the elements you want to see in Chip Canvas.

For example if you want to view all MACC cells available on the M2S010T die, enable **Device -> Device Cells -> MACC** and disable everything else. All MACC elements that are part of the Device are now shown on Chip Canvas.

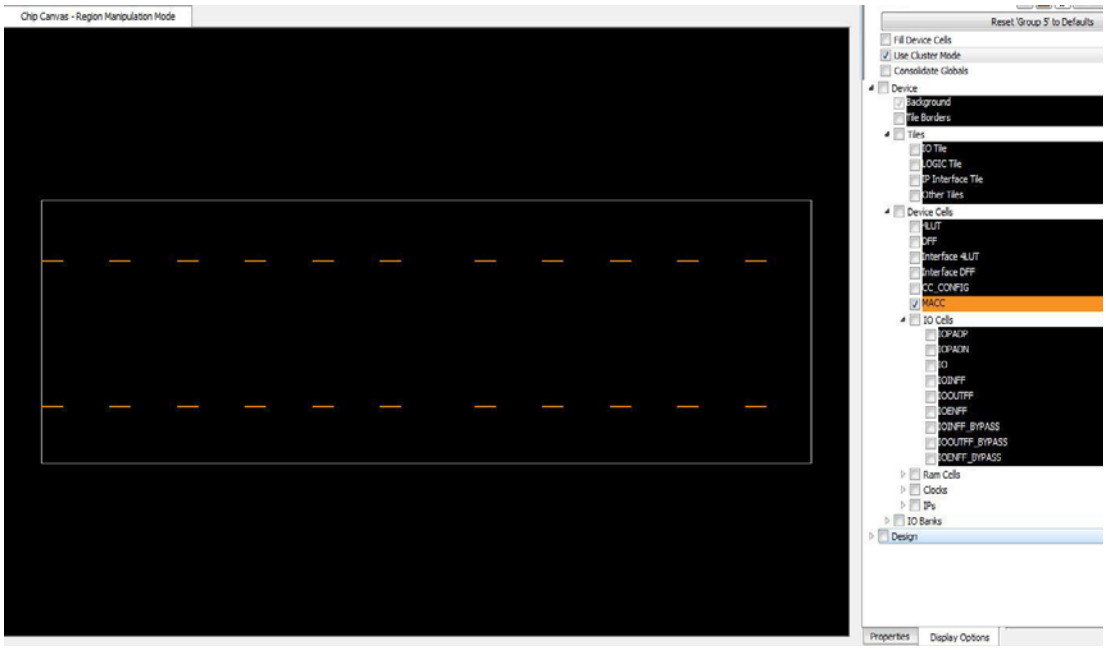

***Figure 2-4* • MACC Resources Displayed in Chip Canvas**

Some of the options in Display Options window cannot be unchecked as these options are fixed for any design. Such options (shown below) have checkboxes grayed-out and are always enabled. However you can still change the colors settings of these options.

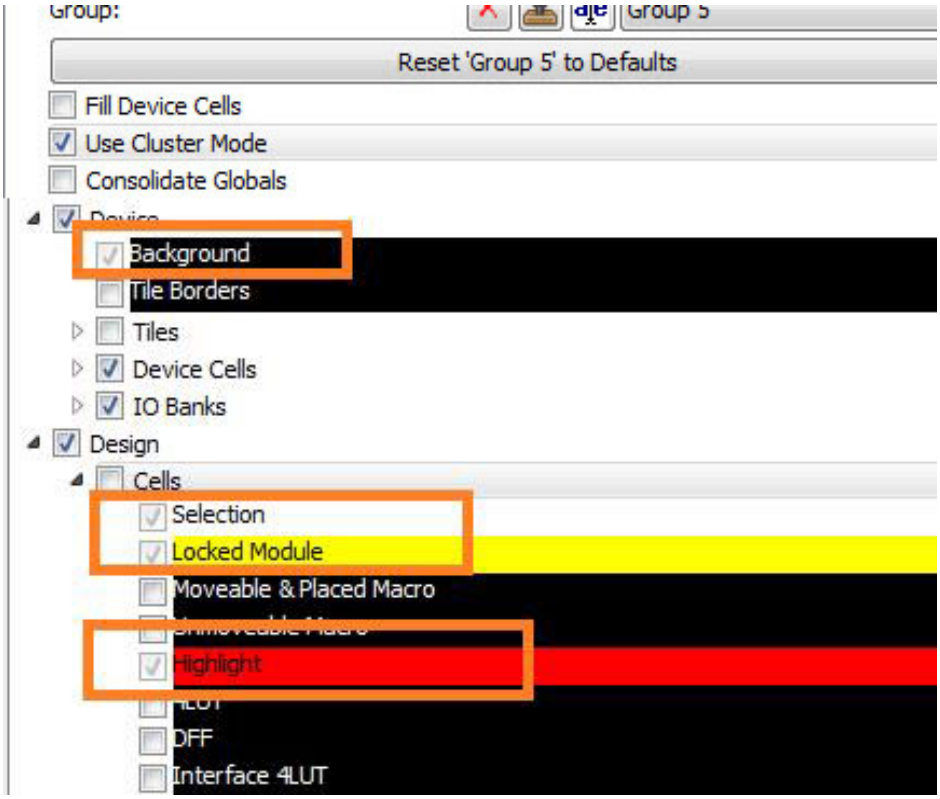

***Figure 2-5* • Options that Cannot Be Unchecked**

Design Option in Display Options Windows can be grouped according to Macro Type and State of Macro. The display of design elements in Chip Canvas depends on both conditions met: the Macro Type and the State of macro. For example if you want to see 4LUT elements of your design, then you need to select both Movable & Placed Macro and 4LUT options as shown below.

***Figure 2-6* • Macro State and Macro Types**

The Movable and Placed 4LUT macro is displayed in Chip Canvas.

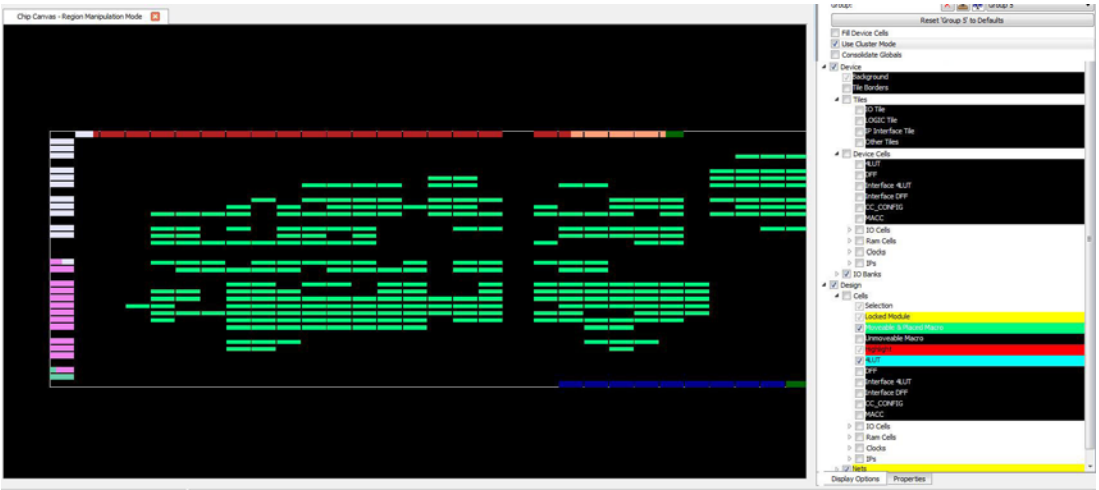

***Figure 2-7* • Chip Canvas display of Movable and Placed 4LUT macro**

Refer to Appendix A, "Family-specific Macros/Nets/Ports" for the list of Macros available in Display Options Window.

Creating Personal Settings

You can create your own layers and colors settings according to your preferences.

1. Create a clone from one of the selected settings using **Clone Setting** icon in Display Options window.

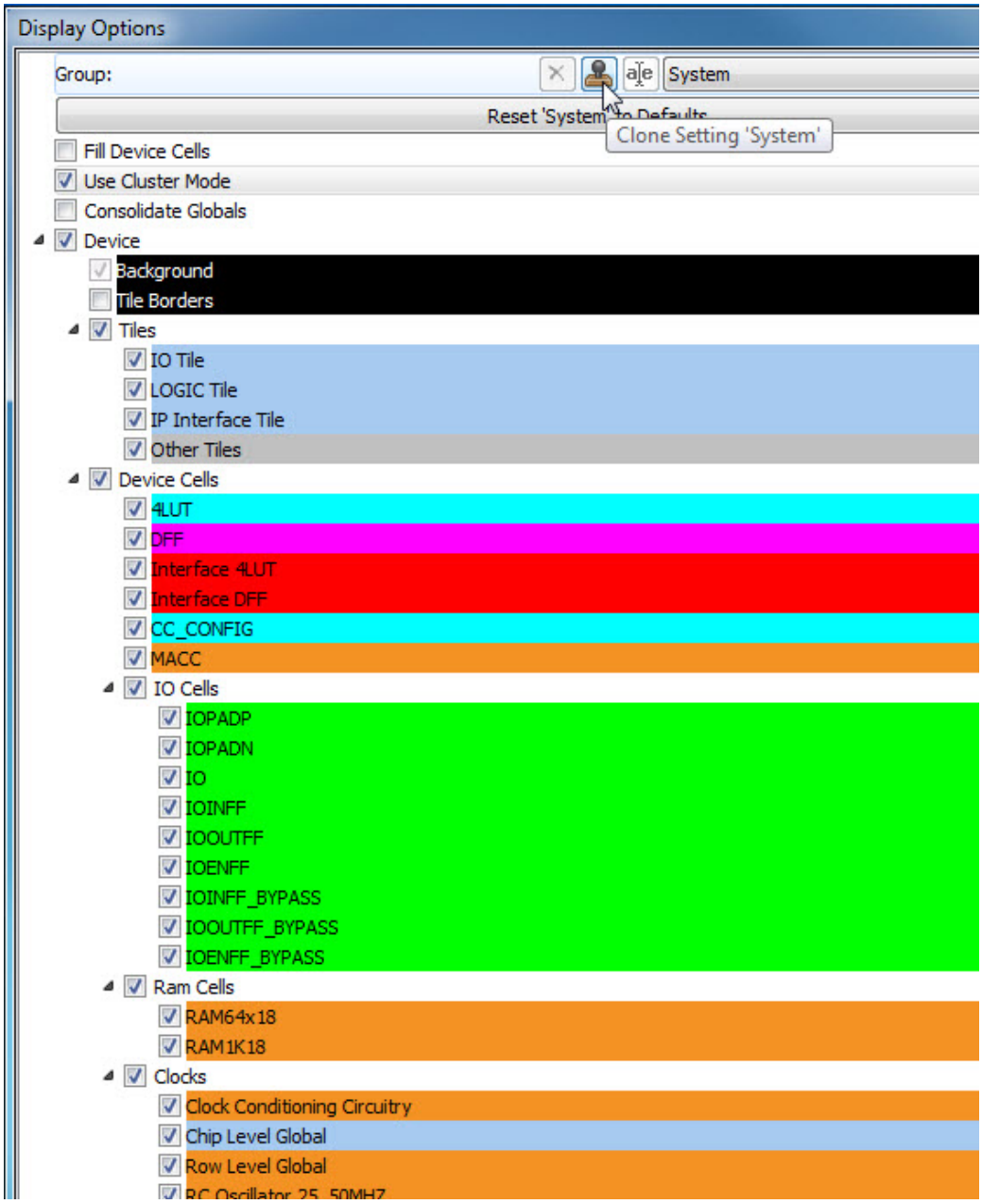

Figure 2-8 • **Clone Settings in Display Options Window**

2. Accept the default name “Group #” for the settings name or rename it from the Display Options window.
3. Change color settings and/or select items to be displayed from Display Options window.

Take for example, a new settings group from the System group has been cloned and new color settings for Device > MACC cells have been set and everything else has been disabled. This setting is renamed to MACC_ELEMENTS. The figure below shows what is displayed in Chip Canvas.

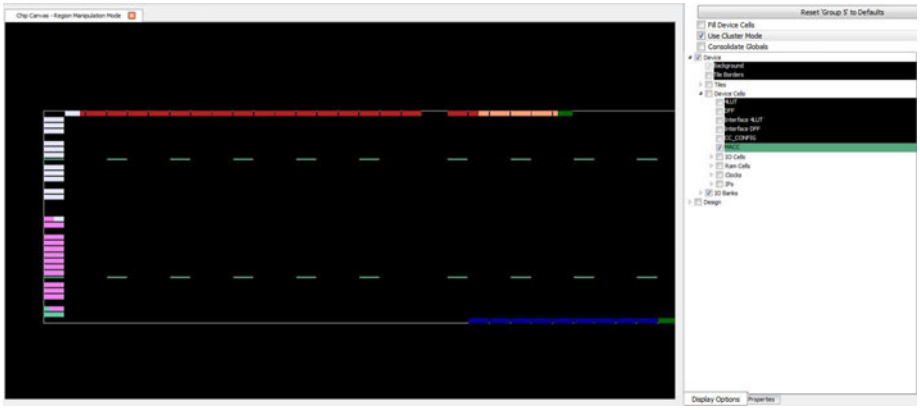

***Figure 2-9* • Chip Canvas View with Cloned Settings**

The customized settings are now created and preserved on your system and will always be available in the drop-down group list in the Display Options window. The customized settings are available to you across different projects on the same machine.

Removing Custom Setting Group

To delete the custom setting group, select the custom setting group and click **Remove Setting icon** in Display Options Window.

Note: The System setting is the default group and it cannot be removed. Only user-set custom settings can be removed.

Reset to System Default

Click **Reset <group_name> to Default** to reset the group's settings to the system default settings.

Chip Display Options

The following options are available in the Display Options Window. They control the display in the Chip Canvas window:

Fill Device Cells

When this box is checked, the entire chip canvas is filled with all device modules at all view levels. Use this mode to see the display of all device resources on the chip. When this mode is not enabled (the default), only the devices used by the design are displayed.
Device cells which are shown are dependent on the Display Options settings for Device cells.

Use Cluster Mode

When this box is checked, the clusters (rather than the modules and macros inside the clusters) of the chip are displayed. This mode is useful when the Chip Canvas is zoomed out far enough to make the modules and macros too small to be visible. This mode significantly improves runtime performance, especially when displaying large device.The cluster will be displayed as used in the Chip Canvas if any module inside it is used.
When this mode is not enabled (the default), the Chip Canvas displays down to the macro and module level. This mode may incur runtime penalty, particularly on large devices.

Consolidate Globals

When this box is checked, the Row Globals (RGB) are hidden from the Chip Canvas view. Row globals (RGB) do not exist in the user netlist. They are buffers inserted by Libero SoC after layout. When this option is turned on, the Row Globals are removed from the display and the Chip Globals are shown as directly driving the macros and cells. This view makes it easier to determine the load of the Chip Globals. To do so, there is no need to track the load from the Chip Globals to the Row Globals and then to the macros and cells.

The table below lists the icons specific to the Display Options window.

Table 2-1 • **Display Options Icons**

Icon	Name	Function
	Rename Settings	Rename user created layers and colors settings from the default name to a name you specify
	Remove Settings	Remove the user defined Layers and colors settings.
	Clone Settings	Create a clone of current Layers and Colors Settings

Design Elements in Display Options Window

The design elements displayed in the Display Options Window are family and die-dependent. See Table 6-4 • SmartFusion2/IGLOO2/RTG4 Family-specific Design Elements for Layers and Colors Settings for details.

3 – Other Chip Planner Windows

Chip Canvas Window

The Chip Canvas displays all the design elements in one window. The selections you make in the views are reflected in the Chip Canvas window. The color scheme used in the canvas is dependent on the Layers and Colors you have selected.

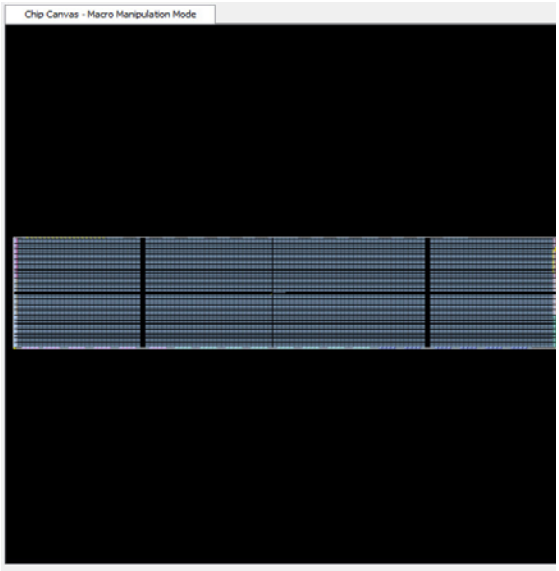

***Figure 3-1* • Chip Canvas Window**

Operation Modes

The Chip Canvas has two modes of operation. Toggle the  button in the tool bar to switch between them:

- Chip Canvas - Macro Manipulation Mode

  Use this mode to work with macros, such as assigning macros to location or un-assigning placed macros from locations. You can also view properties of selected macros in Chip Canvas from properties window. You can also select multiple macros from the Chip Canvas by pressing <CTRL> key and selecting required macros in the Chip Canvas.
  In Macro Manipulation Mode, placed but unlocked macros can be dragged and dropped from one legal location to another. To help you find a new location for the macro, as you drag the macro across the Chip Canvas, the Chip Planner displays in the lower left corner the following information:

  – Macro Name and Type
  – Current X-Y co-ordinates
  – (Current Location) Incompatible or
  – (Current Location) Legal location (Elements can be legally placed)

- Chip Canvas - Region Manipulation Mode

  Use this mode to work on regions such as resizing, renaming, deleting or renaming regions, assigning and un-assigning macros or nets to regions.

Note: When you first create a region, the Chip Planner by default enables the Region Manipulation Mode.

Display Options

The Chip Canvas has display modes controlled by enabling/disabling checkboxes in the Display Options Window. These modes determine the granularity and the level of details in the Chip Canvas display. See "Chip Display Options" on page 43 for details.

World View Window

The World View shows a red rectangle which reflects what is visible in the Chip Canvas view in the context of the Chip. Changing what is visible in the canvas also changes the red rectangle. Changing the size or position of the red rectangle changes what is seen in the Chip Canvas.

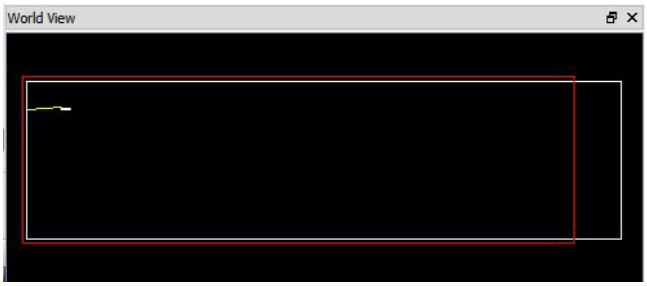

Figure 3-2 • **World View**

Log Window

The Log window displays all messages Chip Planner generates. You can filter the messages according to the type of message - Error, Warning, and Info. If you have made and saved changes in the Chip Planner, the Log Window displays the name and location of the PDC file(s) which have been edited/ updated to reflect the changes.

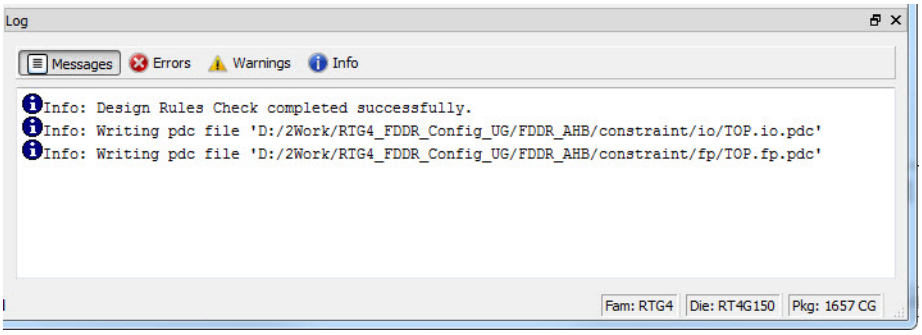

Figure 3-3 • **Log Window**

Message Window

The Message Window organizes and displays messages in two levels: parent message (first-level) and child messages (second-level).

Parent Message

A parent message is a message summary. It is the first-level primary message which can be expanded to expose more messages that fall within the summary.

An example is the creation of an exclusive region over placed macros. The parent message “Creating region UserRegion1 caused side-effects” appears in the Message Window.

***Figure 3-4* • Parent Message in Message Window**

Child Message

A child message is the second-level message that appears when the parent message it belongs to is expanded.

In this case, when the parent message is expanded, the child message displays the message “Macro: <macro_name> is being unplaced”.

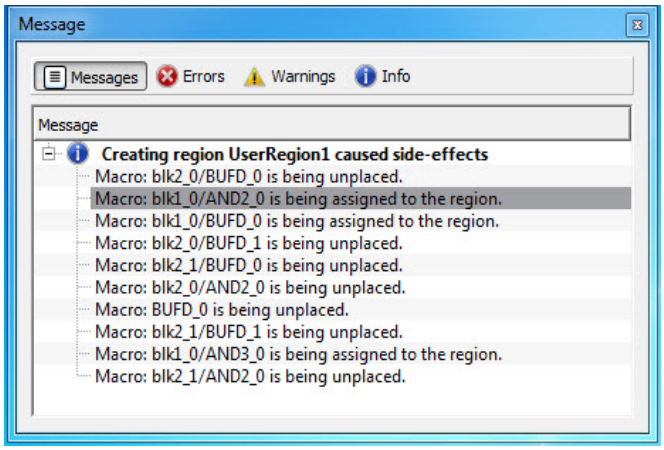

***Figure 3-5* • Parent Message Expanded to display Child Messages**

4 – Floorplanning Using Chip Planner

Floorplanning includes creating regions and making logic assignments to those regions. It is an optional methodology to improve the performance and routability of your design. The objective in floorplanning is to assign logic to specific regions on the chip to enhance performance and routability.

When floorplanning, you analyze your design to see if certain logic can be grouped within regions. Placement regions are especially useful for hierarchical designs with plenty of local connectivity within a block. If your timing analysis indicates several paths with negative slack, try grouping the logic included in these paths into their own regions. This forces the placement of logic within the path closer together and may improve timing performance of the design.

Use floorplanning to create Design Separation Regions for security-critical designs. For Microsemi's Design Separation Methodology all logic should be contained in a logic placement region with dedicated place and route resources. Refer to the Microsemi Design Separation Methodology for details.

http://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc#documents

Use Chip Planner before and after running layout to help you floorplan. You may

- Create Regions
- Move, Resize, merge or delete regions
- Assign logic to region
- Assign nets to regions

Types of Regions

Three region types can be created for floorplanning purpose:

Inclusive Region

An inclusive region is one that the user allows the Place-and-Route tool to place unassigned logic within its boundary. It can contain macros, both assigned and unassigned to region. Routing resources within an inclusive region are also not restricted. Logic already placed there before region creation are not unplaced from the region.

Use the **create Inclusive Region** icon  to create an Inclusive region.

Once a region rectangle is created you can assign logic macros / net macros / port macros to it from the design view window.

You can also draw region rectangle over placed macros and assign these macros to region using **Assign macros inside region** option by selecting region rectangle on Chip canvas

Figure 4-1 **• Inclusive Region Example**

Exclusive Region

An exclusive region is one that the user does not allow the Place-and-Route tool to place unassigned logic within its boundary. It can contain only macros already assigned to the region before the region is created. Routing resources within an exclusive region are, however, not restricted.

Use the **Create Exclusive Region** icon  to create an Exclusive region.

Once a region rectangle is created you can assign logic macros / net macros / port macros to it from design view window.

In case an exclusive region rectangle is created over placed macros, the locked macros already there inside the exclusive region will not be unplaced. They are automatically assigned to region. If the macro is placed but not locked, the macros will be unplaced from the locations and will not be assigned to the exclusive region. The message window displays a message about this side-effect. Click to expand the message to see what macros have become unplaced.

***Figure 4-2* • Exclusive Region Example**

Empty Region

An empty region is one that neither the user nor the Place-and-Route tool can place any logic within its boundary. Routing resources within an empty region may be used by Place and Route tool though.

Use the **Create Empty Region icon**  to create an Empty region.

You cannot assign logic macros / net macros / port macros to an empty region.

In case an empty region rectangle is created over placed macros which are not locked, the macros will be unplaced from the locations. The Message Window displays a message about side-effects. Expand this message summary to see the list of unplaced macros as a result of this side-effect.The creation of an Empty Region over locked macros is not allowed.

***Figure 4-3* • Empty Region Example**

Creating Rectilinear Regions

To create a rectilinear region for floorplanning:

1. Click the region icon: Empty/Inclusive/Exclusive.

2. Go to the Chip Canvas and click at the location you want to create a region.
3. Drag the mouse diagonally to draw a rectilinear shape for the size of the region you want. The region is named UserRegion1, 2, 3 and so on by default for Inclusive and Exclusive Regions and EmptyRegion1, 2, 3 and so on by default for Empty Regions.
4. (Optional) Right-click and select **Rename** to rename the region from the default name to a different name.
5. Click **Commit** to save the changes.

Note: When creating a user region and its boundary falls on top of a cluster boundary, the tool extends the region to include the cluster into the region.

Note that Log Window prints out the message that PDC files are updated/written to reflect the changes you have made in Chip Planner.

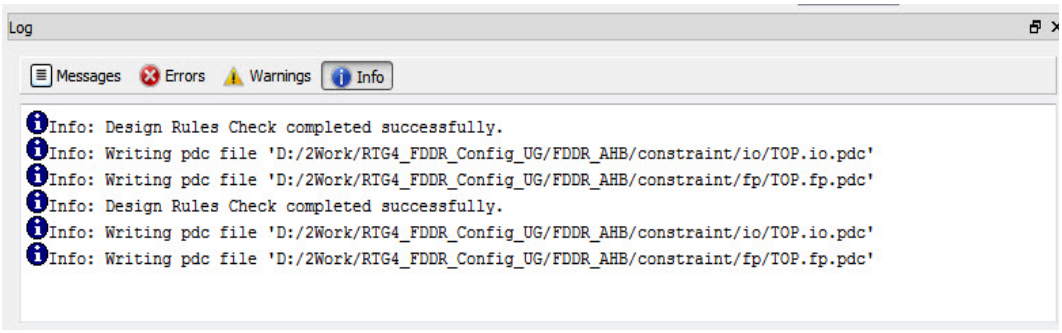

Figure 4-4 • **Log Window Messages**

Note that the <proj_location>\constraint\<root>.fp.pdc is updated with the “define_region” command to reflect the new user region you create.

```
define_region -name EmptyRegion3 -type empty -color 2143322112 648 225 659 227
define_region -name UserRegion1 -type inclusive -color 2147442270 552 300 731 311
```

For details of the PDC commands, refer to the PDC Commands User Guide (**Libero SoC Help > Reference Manual > PDC Commands User Guide**)

The "Properties Window" displays the properties of the region you have created.

Creating Non-Rectilinear Regions

By default a region is created with a rectangular area. However you can also create a non-rectilinear regions by merging two or more rectangular regions.

Note: Use inclusive or exclusive region constraints if you intend to assign logic to a region. An inclusive region constraint with no macros assigned to it has no effect. An exclusive region constraint with no macros assigned to it is equivalent to an empty region.

Note: A user region in which there are macros assigned to it is identified by vertical and horizontal checkered-board pattern

A user region without any logic assigned to it is identified by diagonal hash lines. pattern.

Assigning Components/Macros to Regions

To assign Components or Macros to a user region:

1. Right-click the Component/Macro in the Logical View and select Assign Component/Macro to a UserRegion.
2. Click **Commit** to save the changes.

Alternatively, you can drag-drop the component / macro from the logical view onto a user region on Chip Canvas.

The Component/Macro that has been assigned to the region is identified with a blue tick

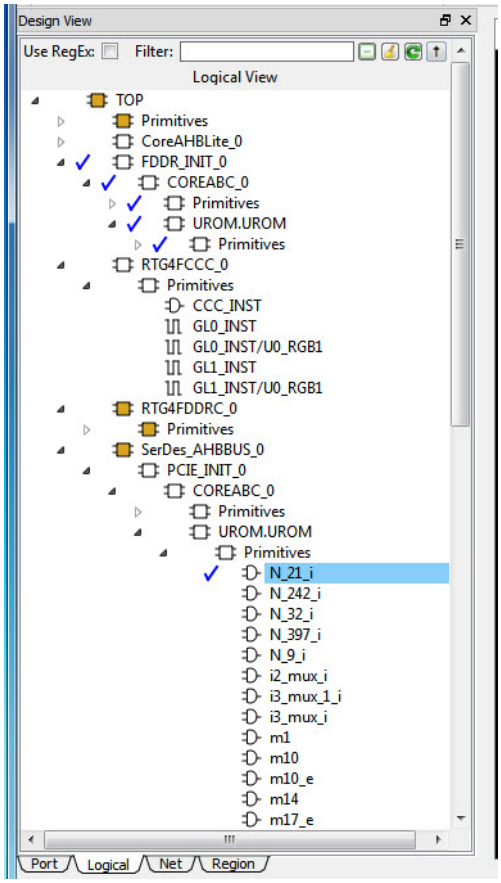

Figure 4-5 • **Macro Assigned to a User Region**

Note that Log Window prints out the message that PDC files are updated/written to reflect the changes you have made in Chip Planner.

Note that the <proj_location>\constraint\<root>.fp.pdc is updated with the assign_region PDC command:

```
define_region -name UserRegion1 -type inclusive -color 2147442270 552 300 731 311
assign_region UserRegion1 FDDR_INIT_0
```

For details on PDC commands, refer to the PDC Commands User Guide (**Libero Soc Help > Reference Manual > PDC Command User Guide**)

Routing Inside Constrained Region

By default, when a region is first created, the region properties (Inclusive/Exclusive/Empty) apply to design resources (Placement) only. The Place and Route tool is free to use the routing resources inside the region. To further constrain the Place and Route tool on routing resources usage inside the region, click the **Constrain Routing** check box in the Properties window.

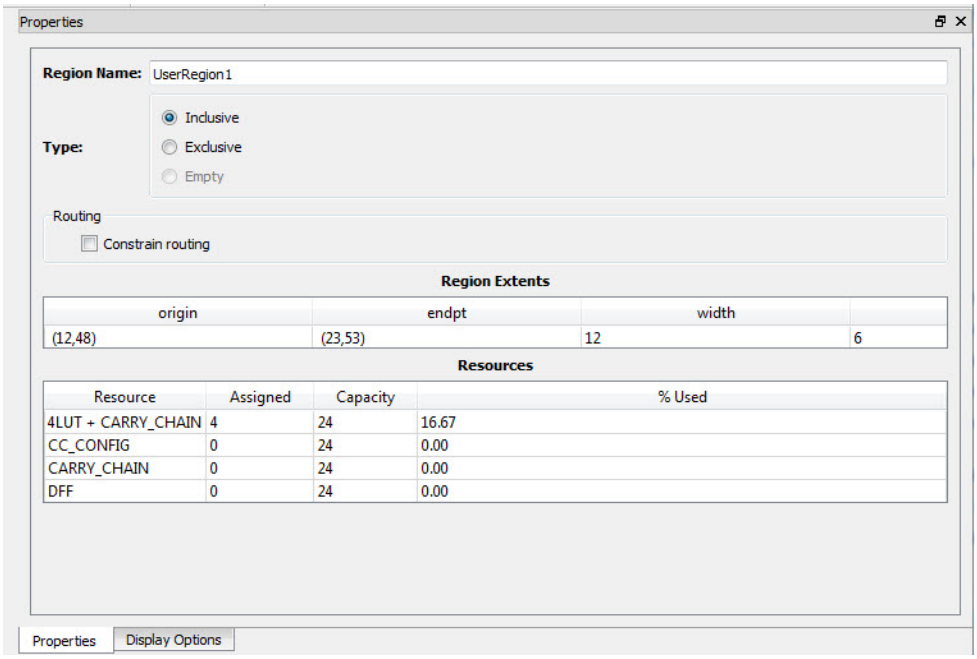

***Figure 4-6* • Constrain Routing Checkbox inside Property Window**

Constrain Routing

This option applies to all types of regions: inclusive, exclusive and empty.

When this check box is checked, the region constraints are applied to routing, in addition to placement. The routing behavior is summarized in Table 4-1 for each type of user regions

***Table 4-1* • Routing Behavior Inside User Regions with Constrain Routing Enabled**

Region Type	Routing Behavior
Inclusive	• For all nets internal to the region (the source and all destinations belong to the region), routing must be inside the region (that is, such nets cannot be assigned any routing resources which is outside the region or crosses the region boundaries). • Nets not internal to the region can use routing resources within the region.
Exclusive	• For all nets internal to the region (the source and all destinations belong to the region), routing must be inside the region (that is, such nets cannot be assigned any routing resources which is outside the region or crosses the region boundaries). • Nets without pins inside the region cannot be assigned any routing resources which is inside the region or crosses region boundaries).
Empty	• No routing is allowed inside the Empty Region. • However local clocks and globals can cross empty regions.

Empty Region General Guidelines

Empty regions allow you to create exclusive areas on the device where no logic placement can occur. Empty regions help guide the placer to pack your logic closer together and thereby use more local routing resources to connect it. You cannot create empty regions in areas that contain locked macros. Use the following guidelines for empty regions.

Use Empty Regions to Guide the Place-and-Route Process

If your design does not completely use up your target device (for example 60% utilization or lower), use empty regions to cluster your logic placement into specific subareas of the chip. This helps when you have originally placed-and-routed the design into a smaller device but want to fit it to a larger part while still preserving the performance you have achieved in the smaller device.

Use Empty Regions to Reduce Routing Congestion

Creating empty regions next to the congested area(s) of your design helps reduce congestion. When you place an empty region next to congested logic blocks or regions, the placer cannot place any logic next to your region or logic block. Logic, which would normally be placed there, is forced to be placed somewhere else. Routing resources next to the congested area are, therefore, freed up and provide the router more options to route signals into the congested block.

Before deciding to place empty region(s), analyze your design for congestion areas. Use the **Ratsnest** view in Chip Planner to see dense areas of connectivity into and out of your logic blocks or regions. Create empty regions in these congested areas and see it if improves the routability of your logic.

Use Empty Regions to Reserve Device Resources

If you want to preserve the placement of your existing design but plan additional modifications in the future, create empty regions in the areas of the chip where you plan to add additional logic. As you add new logic, remove or resize your empty regions accordingly to fit your new logic. Empty regions placed over I/O pins reserve them for future use as the I/O needs of your design changes. There are some restrictions for using empty regions in this manner.

Overbooking of Regions

Over-booking of regions (assigning resources over 100 percent utilization) is not allowed. When you try to overbook a region, Chip Planner shows the over-booked resource type in the "Properties Window"of the Region and the resources are not assigned to the region. The overbooked resource is highlighted in red in the Region Properties window.

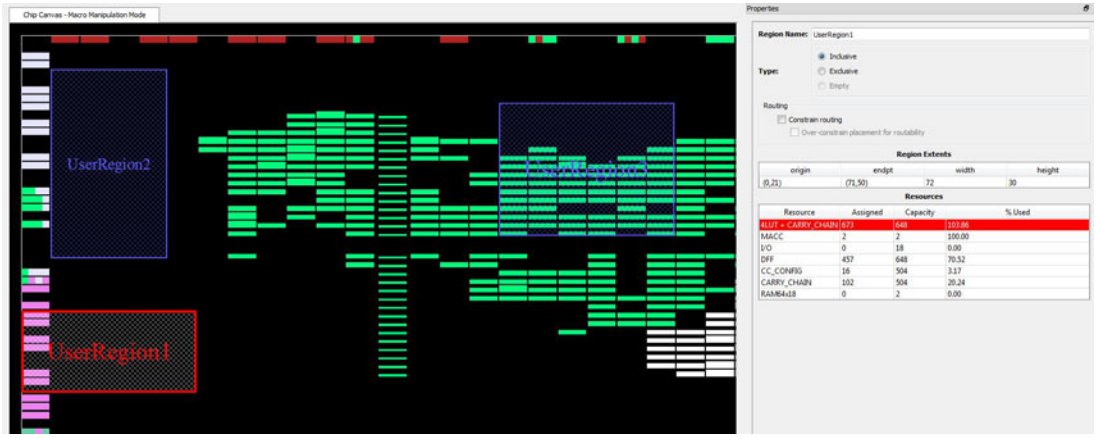

***Figure 4-7* • Overbooking of Region**

User Action on Regions in Chip Canvas

When you select a region on Chip Canvas, you may:

- Rename Regions
- Delete Regions
- Merge Regions
- Unassign macros from Regions

Note: The Chip Canvas has two modes of operation: Macro Manipulation Mode and Region Manipulation Mode. If the Chip Canvas is in the Macro Manipulation Mode, before any region operations (Resizing/Renaming/Deleting/Merging), you must first click the Region/Macro Toggle Switch icon  to enter the Region Manipulation Mode.

Note: Any side-effects such as unplacing or un-assigning of a macro due to region creation or region resizing are shown in the Message Window.

5 – Cross-Probing from SmartTime to Chip Planner

Cross-probing allows you to select a design object in one application and the selection is reflected in another application. When you cross-probe a design object from SmartTime to Chip Planner, you will understand better how the two applications interact with each other. With cross-probing, a timing path not meeting the timing requirements may be fixed with relative ease when you see the less-than-optimal placement of the design object (in terms of timing requirement) in Chip Planner. Cross-probing from SmartTime to Chip Planner is available for the following design objects:

- Macros
- Ports
- Nets/Paths

Note: Cross-probing of design objects is available from SmartTime to Chip Planner but not vice versa.

Before you can cross-probe from SmartTime to Chip Planner, you need to have:

1. Completed Place and Route on the design.
2. Opened both SmartTime and Chip Planner.

Cross-Probing Examples

To cross-probe from SmartTime to Chip Planner, a design macro in the SmartTime is used as an example.

Design Macro Example

1. Make sure that the design has successfully completed the Place and Route step.
2. Open SmartTime Maximum/Minimum Analysis
3. Open Chip Planner.
4. In the SmartTime Maximum Analysis view, right-click the instance Q[2] in the Timing Path Graph and select **Show in Chip Planner**. Note that with cross-probing the Q[2] macro is selected in Chip Planner's Logical View and highlighted (white) in the Chip Canvas. The Properties window in Chip Planner displays the properties of Q[2].

Note: Menu item **Show in Chip Planner** is grayed out if Chip Planner is not already opened.

Note: You may need to zoom in to view the highlighted Q[2] Macro in the Chip Canvas.{net

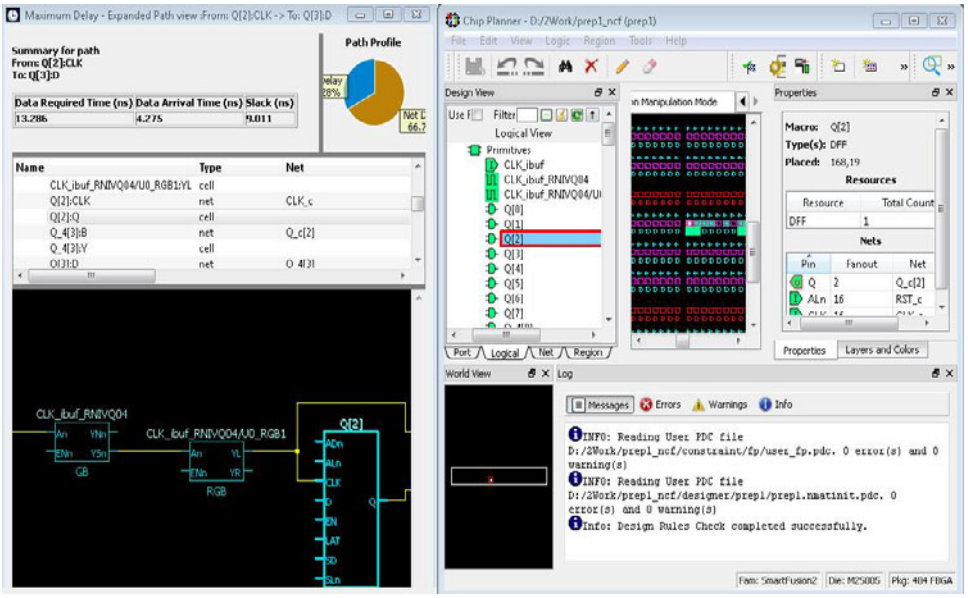

Figure 5-1 • **Cross-Probing the Q[2] Macro**

CLK_ibuf_RNIVQ04/U0_YWn_GEast}

Timing Path Example

1. Make sure that the design has successfully completed the Place and Route step.
2. Open SmartTime Maximum/Minimum Analysis view.
3. Open Chip Planner.
4. In the SmartTime Maximum/Minimum Analysis view, right-click the net Cliburn/U0/U_IOPAD:PAD in the Table and select **Show Path in Chip Planner**. Note that the net is selected (Highlighted in red) in the Chip Canvas view and the three macros connected to the net are also highlighted (white) in the Chip Canvas view.

Note: The color for highlights and cross-probed elements can be changed from the Display Options window.

Note: Menu item **Show Path in Chip Planner** is grayed out if Chip Planner is not already opened.

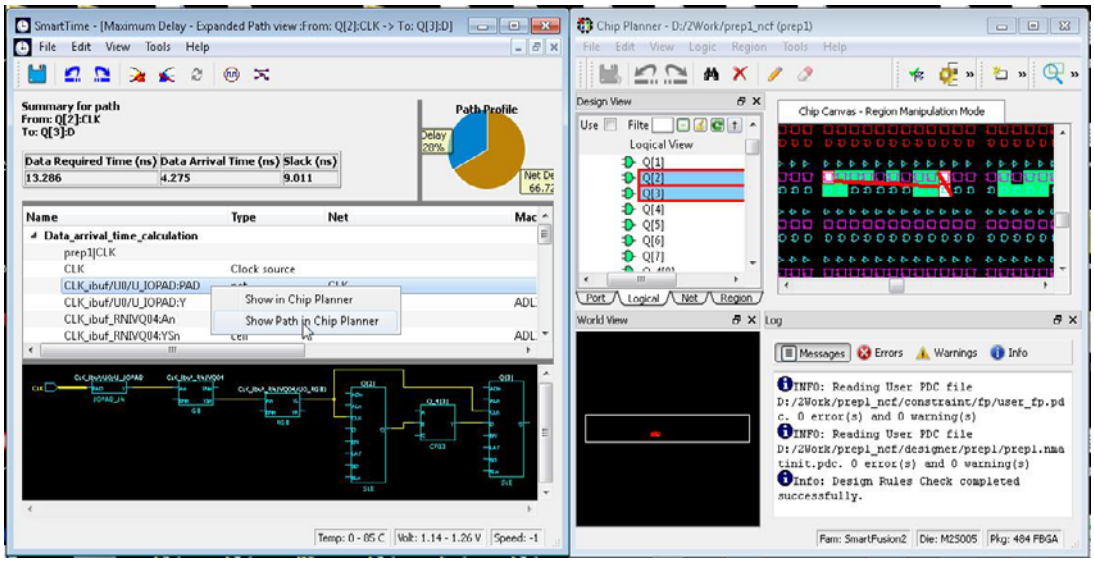

***Figure 5-2* • Cross-Probing - Timing Path**

Alternatively, right-click from SmartTime's Max/Min Delay Analysis Table view to cross-probe into Chip Planner.

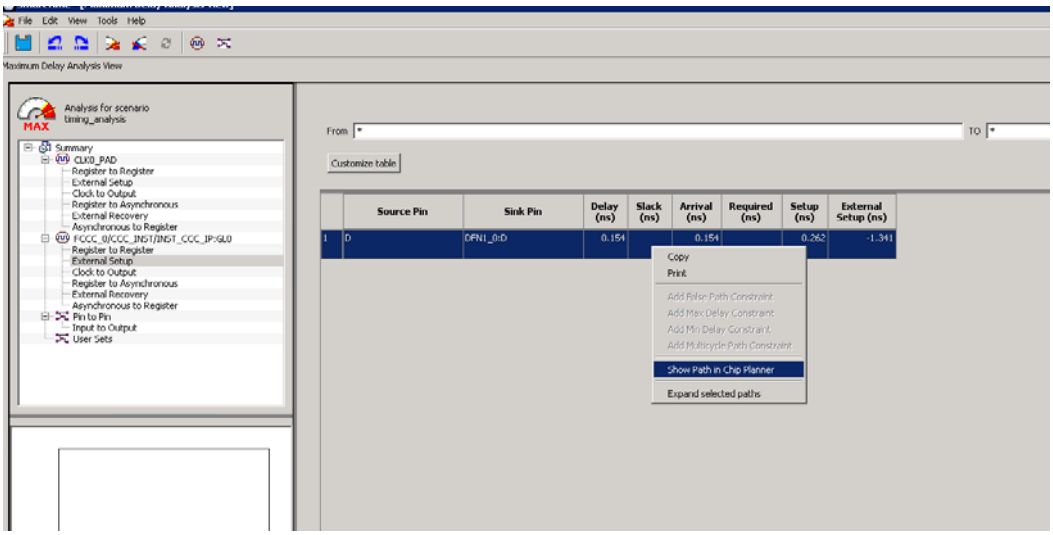

***Figure 5-3* • Cross-Probing from Max/Min Delay Analysis View Table**

Port Example

1. Make sure that the design has successfully completed the Place and Route step.
2. Open the SmartTime Maximum/Minimum Analysis View
3. Open Chip Planner.
4. In the SmartTime Maximum/Minimum Analysis view, right-click the Port "CLK" in the Path and select **Show in Chip Planner**. Note that the Port "CLK" is selected and highlighted in Chip Planner's Port View.

Note: Show in Chip Planner is grayed out if Chip Planner is not already open.

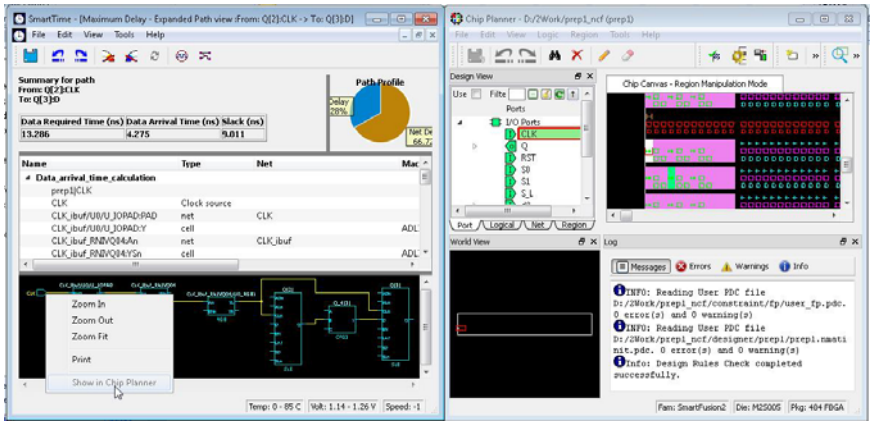

Figure 5-4 • **Cross-Probing - Port**

From the Properties View inside Chip Planner, you will find useful information about the Port “CLK” you are cross-probing:

- Port Type
- Port Placement Location (X-Y Co-ordinates)
- I/O Bank Number
- I/O Standard
- Pin Assignment

A – Family-specific Macros/Nets/Ports

The filter list for Nets, Macros and Ports are family-specific. The hardware items displayed in the Display Options Window are also family-specific.

SmartFusion2/IGLOO2/RTG4-specific Ports, Macros, Nets

***Table A-1* • SmartFusion2/IGLOO2/RTG4 Family-specific Ports Filter List**

Port Filter List	Descriptions
I/Os	All I/Os
Single-ended I/O	Single-ended I/Os
Differential I/O pair	Differential I/O pair
Input I/O	Inputs
Output I/O	Outputs
Inout I/O	Bidirections
I/O Register - DDR I/O	I/O Register (I/Os combined with registers) or DDR I/Os

***Table A-2* • SmartFusion2 Macro Filter List**

Macro	Descriptions
DFF	Represents a Sequential Element.
4LUT	Represents a Combination Element (4-input look-up table).
Carry Chain	Carry Chain macro
Carry Chain Config	Represents a carry chain configuration element which drives a carry chain.This is created by the Compile engine for internal timing modeling.
RAM1K18	Represents a LSRAM block.
RAM64x18	Represents a USRAM block.
MACC	Represents a MATH block.
CCC	Represents a Clock Conditioning Circuitry Block.
I/O Register -DDR I/O	Represents an I/O Element along with IO registers.
I/O	Displays all I/O Macro.
Input I/O	Input Macro
Output I/O	Output Macro
Inout I/O	Inout Macro
Single-ended I/O	Single-end I/O Macros
Differential I/O Pair	Differential I/O Macros
Chip Global	Chip Level Globals. Represents GB resources usually located at center of the chip.
Row Global	Row Level Globals. Represents RGB resources usually located on vertical stripes on left half and right half of the chip
SERDESIF	Represents a SerDes resource.
FDDR	Represents a FDDR resource.

***Table A-2* • SmartFusion2 Macro Filter List (continued)**

Macro	Descriptions
RCOSC_50MHZ	Represents 50MHz oscillator available in selected die.
RCOSC_1MHZ	Represents 1MHz oscillator available in selected die.
XTLOSC	Crystal Oscillator available in selected die.
MSS	Represents a Microcontroller Subsystem resource.

***Table A-3* • IGLOO2 Macro Filter List**

Macro	Descriptions
DFF	Represents a Sequential Element.
4LUT	Represents a Combination Element (4-input look-up table).
Carry Chain	Carry Chain macro
Carry Chain Config	Represents a carry chain configuration element which drives a carry chain.This is created by the Compile engine for internal timing modeling.
RAM1K18	Represents a LSRAM block.
RAM64x18	Represents a USRAM block.
MACC	Represents a MATH block.
CCC	Represents a Clock Conditioning Circuitry Block.
I/O Register -DDR I/O	Represents an I/O Element along with IO registers.
I/O	Displays all I/O Macro.
Input I/O	Input Macro
Output I/O	Output Macro
Inout I/O	Inout Macro
Single-ended I/O	Single-end I/O Macros
Differential I/O Pair	Differential I/O Macros
Chip Global	Chip Level Globals. Represents GB resources usually located at center of the chip.
Row Global	Row Level Globals. Represents RGB resources usually located on vertical stripes on left half and right half of the chip.
SERDESIF	Represents a SerDes resource.
FDDR	Represents a FDDR resource.
RCOSC_50MHZ	Represents 50MHz oscillator available in selected die.
RCOSC_1MHZ	Represents 1MHz oscillator available in selected die.

***Table A-3* • IGLOO2 Macro Filter List (continued)**

XTLOSC	Crystal Oscillator available in selected die.
HPMS	High Performance Memory Subsystem

***Table A-4* • RTG4 Macro Filter List**

Macro	Descriptions
DFF	Represents a Sequential Element.
4LUT	Represents a Combination Element (4-input look-up table).
Carry Chain	Carry Chain macro
Carry Chain Config	Represents a carry chain configuration element which drives a carry chain.This is created by the Compile engine for internal timing modeling.
RAM1K18	Represents a LSRAM block.
RAM64x18	Represents a USRAM block.
MACC	Represents a MATH block.
CCC	Represents a Clock Conditioning Circuitry Block.
I/O Register -DDR I/O	Represents an I/O Element along with IO registers.
I/O	Displays all I/O Macro.
Input I/O	Input Macro
Output I/O	Output Macro
Inout I/O	Inout Macro
Single-ended I/O	Single-end I/O Macros
Differential I/O Pair	Differential I/O Macros
H-Chip Global	Chip Level Globals. Represents GB resources usually located at center of the chip.
Row Global	Row Level Globals. Represents RGB resources usually located on vertical stripes on left half and right half of the chip.
SERDESIF	Represents a SerDes resource.
FDDR	Represents a FDDR resource.
RCOSC_50MHZ	Represents 50MHz oscillator available in selected die.
Global Async Reset	Represents instances using GRESET macro.
Local Async Reset	Represents instances using RGRESET macro.
UPROM	Micro Programmable Read-Only Memory

***Table A-5* • SmartFusion2/IGLOO2/RTG4 Family-specific Nets Filter List**

Net Filter Type	Descriptions
Clock	Nets with clock pins connected to it
Chip Global	Nets which are routed through Chip Global Resources
Row Global	Nets which are routed through Row Global Resources
Hardwired	Nets which are routed through hardwired connections
Regular	Nets which are routed through fabric routing resources

***Table A-6* • SmartFusion2/IGLOO2/RTG4 Family-specific Design Elements for Layers and Colors Settings**

Design Group	Design Element	Descriptions
Device Cells	4LUT	4-input Look-up Table
	DFF	Sequential Element
	Interface 4LUT	Interface 4LUTs used in the RAMs and Math blocks
	Interface DFF	Interface DFF used in the RAMs and Math blocks
	CC_CONFIG	Carry Chain Configuration
	MACC	Math Blocks
IO Cells	IOPADP	P side of a differential IO
	IOPADN	N side of a differential IO
	IO	Regular IO
	IOINFF	Input IOFF
	IOOUTFF	Output IOFF
	IOENFF	Enable IOFF
	IOINFF_BYPASS	Input IOFF in bypass mode
	IOOUTFF_BYPASS	Output IOFF in bypass mode
	IOENFF_BYPASS	Enable IOFF in bypass mode
RAM Cells	RAM64Kx18	RAM64Kx18 Memory Block
	RAM1K18	RAM1K18 Memory Block
Clocks	Clock Conditioning Circuitry	Clock Conditioning Circuitry
	Chip Level Global	Chip Level Global
	Row Level Global	Row Level Global
Oscillators	RC Oscillator 25_50MHz	50MHZ Oscillator
	RC Oscillator 1MHz	1MHZ Oscillator
	Crystal Oscillator	Crystal Oscillator
	Fabric RC Oscillator 25_50MHz	50MHZ Oscillator going to the fabric
	Fabric RC Oscillator 1MHz	1MHZ Oscillator going to the fabric
	Fabric Crystal Oscillator	Crystal Oscillator going to the fabric

***Table A-6* • SmartFusion2/IGLOO2/RTG4 Family-specific Design Elements for Layers and Colors Settings**

Design Group	Design Element	Descriptions
IPs	IP Interface	Interface to the IPs such as SERDES
	MSS/HPMS	MSS (SmartFusion2 Only)
	HPMS	HPMS (IGLOO2 Only)
	SYSCTRL	System Controller

B – Limitations

The Chip Planner has the following limitations:

I/O Register Support

Every I/O has several embedded registers that you can use for faster clock-to-out timing, and to meet external hold and setup timing requirements. This feature uses input, output or enable registers available in I/O block.

However a register if combined with a IO register is not shown on Logical view as a separate element and is shown as part of a port.

Figure B-1 **• Register Combined with Input Register of an I/O**

Internal Elements of External IP Macros Displayed in Single Connection

Some external IP such as SERDES and FDDR span across multiple clusters and have their own dedicated ports. However the net connected to these macro I/Os are shown to be connected from a single location. The figure below is an example of a SERDES macro which shows all the associated nets connected to a single macro.

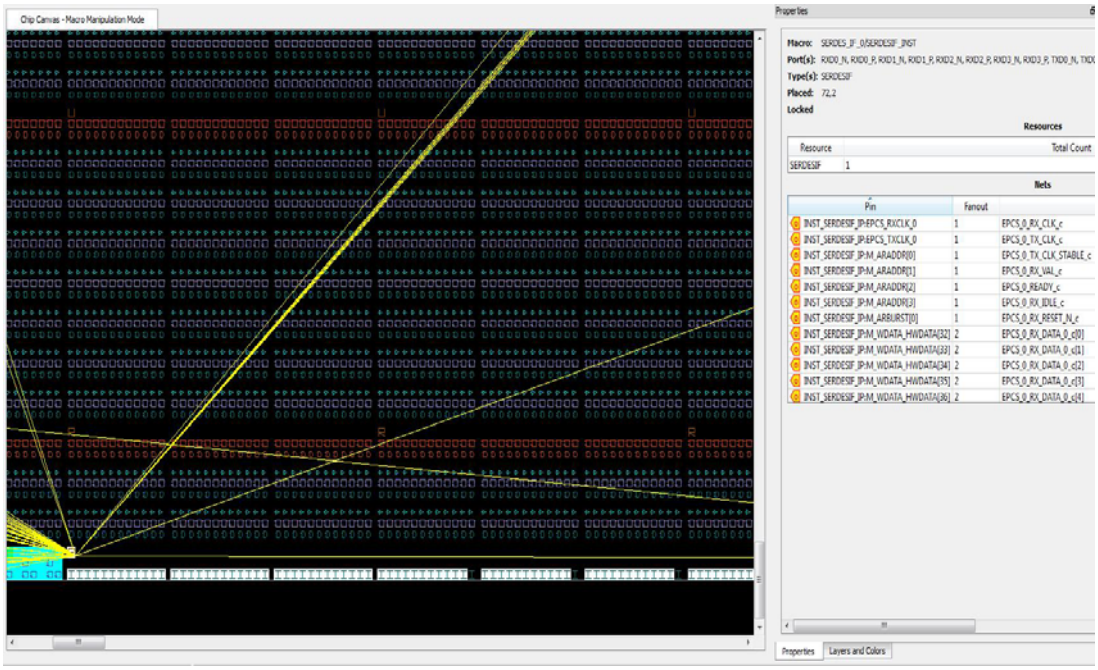

Figure B-2 **• SERDES Macro with Associated Nets in single connection**

A – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world, **650.318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

For Microsemi SoC Products Support, visit http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office.

Visit About Us for sales office listings and corporate contacts.

Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; Enterprise Storage and Communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 4,800 employees globally. Learn more at **www.microsemi.com**.