



#### 3-Output Programmable Fanout Buffer with Multi-Format I/O and Dividers

Product Brief

December 2016

# Features

- 4 Input Clocks
  - One crystal/CMOS input
  - Two differential/single-ended inputs
  - One single-ended/CMOS input
  - Any input frequency up to 1035MHz (up to 300MHz for CMOS)
  - Clock selection by pin or register control

#### • Up to 3 Differential Outputs (Up to 6 CMOS)

- Output frequencies are any integer divisor up to 2<sup>32</sup> of the input frequency (CMOS 250MHz max)
- Each output has independent dividers
- Low additive jitter <200fs RMS (12kHz-20MHz, for input frequencies ≥100MHz)
- Outputs are CML or 2xCMOS, can interface to LVDS, LVPECL, HSTL, SSTL and HCSL
- In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125MHz and 25MHz)<sup>\*</sup>
- Per-output supply pin with CMOS output voltages from 1.5V to 3.3V
- Precise output alignment circuitry and peroutput skew adjustment<sup>\*</sup>
- Per-output enable/disable and glitchless start/stop (stop high or low)<sup>\*</sup>

# **Ordering Information**

32 Pin QFN

32 Pin QFN

ZL40255LDG1 ZL40255LDF1

Trays Tape and Reel

Matte Tin

Package size: 5 x 5 mm

-40°C to +85°C

#### General Features

- Automatic self-configuration at power-up from internal EEPROM; up to four configurations, pin-selectable
- Crystal interface for frequency synthesis up to 60MHz
- Four general-purpose I/O pins, each with many status and control options
- SPI or I<sup>2</sup>C processor Interface
- Tiny 5x5mm QFN package

# Applications

- Frequency synthesis up to 60MHz
- Fanout up to 1035MHz
- Format conversion, frequency division, and skew adjustment in a wide variety of equipment types



Figure 1 - Functional Block Diagram

\* Some features require a higher-frequency input clock and enabling the output dividers.



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