Advanced Packaging for Implantable Devices
Introduction

- Market drivers and the emergence of “hidden” devices
- Technology options
- Getting access to smart phone packaging technology
- Emergence of “hidden” die technology
- Case studies and where next
Market Drivers for “Hidden” Devices

- **Miniaturization**
  - Patient comfort, aesthetics and wound healing
- **Wireless telemetry**
  - Remote monitoring and communication
- **Low power**
  - Additional functions limited by battery life
- **Lower cost**
  - Needed to increase sales
  - Simplified electronics assembly
  - Only 1 in 9 patients in emerging markets requiring pacemakers receive one
- **These drivers are very similar to mobile phones**
Packaging Technology Options

- Bare die package on package (PoP)
- Molded laser via PoP
- Embedded die in laminate
- FO wafer level package (WLP)
- Silicon interposer/substrate
- Through-silicon Vias (TSVs)

Images courtesy of STC
Getting Access to High Density Die Packaging

- Packaging needs are very similar to mobile phones
  - Mobile market is many times larger
  - Expensive tooling costs and dedicated chip designs are easily justified
- WFO
  - Dedicated designs and volume
- TSVs
  - Requires dedicated chip designs
  - May not be easy to justify in a mid-volume market
- 2.5 and 3D packaging
  - Requires high volume to get access to suppliers
  - Requires dedicated chip designs
  - Not all players want to supply the medical markets
- Getting access to right technology can be difficult
Emergence of Embedded Die Technology

- **Primary Package Platforms:**
  - DIP, PGA, PLCC, QFP
  - TQFP, TAB, QFN
  - 1ML-CSP, FC CSP, POP

- **Enabling Technologies:**
  - BGA, u"BGA, CSP, FC BGA
  - Flip Chip Interconnect, Thermal management

- **System Applications:**
  - DIP, PGA, PLCC, QFP
  - BGA, u"BGA, CSP, FC BGA
  - Stacking die, Wafer thinning
  - Embedded Si, Face-to-Face interconnect, bio-compatible Materials & packaging, ultra-thin, thru Si via, substrateless pkg

- **Sub Systems Integration:**
  - Hi-Perf BGA, HiCITE Ceramic, POP2
  - FC CSP/POP2, SIP, ML-CSP
  - FC CSP/POP, POP1, MPRK

- **F2F:** Chip-on-MEMS

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Case Study: Radio Module
Case Study: Radio Module

Typical Implantable Cardiac Defibrillator (ICD) Block Diagram

Area of focus – MICS Transceiver Circuit
Case Study: Radio Module

- SHIFT – industrial/academic pioneering collaboration for embedded die

- Demonstrated
  - Reliability of embedded die
  - Potential for miniaturization
  - Design rules

Test platform with die embedded here
Case Study: Radio Module

Die hidden in the PCB

0.50” X 0.32” X 0.06”

400% reduction in area
## Radio Module Qualification

<table>
<thead>
<tr>
<th>Test Group</th>
<th>Test Standard</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Cycling</td>
<td>-40°C to 60°C, 5 cycles</td>
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<tr>
<td>Bake</td>
<td>125°C for 24hrs</td>
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<tr>
<td>Moisture Soak</td>
<td>120hrs, 60°C/60%RH</td>
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<tr>
<td>3x Reflow</td>
<td>JESD22-A113F, 260°C</td>
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<tr>
<td>Thermal Stress:</td>
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<tr>
<td>Low Temperature Storage</td>
<td>-40°C, 72hrs</td>
<td>Pass</td>
</tr>
<tr>
<td>High Temperature Storage</td>
<td>125°C, 72 hrs</td>
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<tr>
<td>Temperature Cycling</td>
<td>MIL-STD-883 Method 1010, Condition B, -55°C to 125°C, 20 cycles</td>
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<tr>
<td>Mechanical Stress:</td>
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<tr>
<td>Mechanical Shock</td>
<td>MIL-STD-883 Method 2002, Condition B, 5 shocks, 1500g</td>
<td>Pass</td>
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<tr>
<td>Constant Acceleriation</td>
<td>MIL-STD-883 Method 2001, 10,000G</td>
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<td>Steady State Life Testing:</td>
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<tr>
<td>Low and High Temperature Testing</td>
<td>0°C, 55°C</td>
<td>Pass</td>
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<tr>
<td>HTOL</td>
<td>125°C, 1000hrs</td>
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<tr>
<td>Exposure:</td>
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<td>ESD</td>
<td>MIL-STD-883 Method 3015, 1000V HBM</td>
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<tr>
<td>Assembly:</td>
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<tr>
<td>External physical dimensions</td>
<td>MIL-STD-883 Method 2016</td>
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<tr>
<td>Ionic Cleanliness</td>
<td>IPC-TM-650</td>
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</tbody>
</table>
Case Study: Radio Module

- Evolution is towards ultra-thin embedded die
- Die (50 to 80um) enables ultra-thin Z axis lamination 0.5mm
- Module height typically 1.0mm (discrete component limit)
Case Study
Stacked Die Module
Case Study: Stacked Die Module

Typical Implantable Cardiac Defibrillator (ICD) Block Diagram

Area of focus – HVFET Circuit
Case Study: Stacked Die Module

- Stacking embedded die layers
  - To enable further miniaturization

- Working on volume rather than planar surfaces of PCB
  - Volume is becoming more critical to device companies than area
Case Study: Stacked Die Module

- Stack of pacemaker protection FETs
  - Large area consumed by the FETs – 10% of ICD PCB
  - Low-power, low-heat
  - High KGD yield
  - But challenging HV barrier requirements
Case Study: Stacked Die Module

- 60% space-saving demonstrated by stacked die module

FET area usage

module area usage

X-ray of test module
Observations for Both Technologies

- Single die single layer (SDSL) embedded die technology is established and gaining greater acceptance in products

- Stacked die technology gaining “interest” traction - currently better suited to low count I/O

- Stacked die technology typically working with stacks of 3 or 4 – some research institutes have discussed at 8 or 10

- Yields can be a limiting factor as die number and stack number increases complexity (MDML)
# Embedded Die Complexity Matrix

## Layer Count

<table>
<thead>
<tr>
<th>Layer Count</th>
<th>1</th>
<th>2(+)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Radio Module Case Study</td>
<td>1</td>
</tr>
<tr>
<td>2(+)</td>
<td>Stacked Die Case Study</td>
<td>2(+)</td>
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</tbody>
</table>

## Greatest Area and Volume Saving

<table>
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Advantages of Embedded Die Packages

- **Good scale of miniaturization**
  - Especially height
  - Die becomes a near zero area occupancy

- **More flexible package design**
  - Package design and footprint can be adapted to meet the system
  - Standard die more easily integrated into system – take a system approach for solution not an accept what is available

- **Potentially low cost for low volumes**
  - Large area mass production PCB panel process
  - Low tooling costs
  - Faster time-to-market
Where Does the Technology Fit?

Benchmark summary

- TIPS (UTCP)
- TIPS (lam.)
- PoP
- WB
- TSV

Embedded die in laminate technology
Comparison with TSV

- **TSV**
  - Lower cost and smaller size

- **However!**
  - Silicon needs to be designed for TSV
  - TSV can consume chip real estate
  - Wafer-level processing as opposed to chip processing
  - TSV insulating liner integrity/leakage – at medical standards?
  - TSV are not available yet for reasonable commercial terms
  - Embedded die in laminate technology suits the lower to medium volumes of the medical market
On the Horizon

- **Integrated Passives**
  - Simplified assembly
  - Medical grade
  - Supports the ultra thin module concepts

- **Chip Scale Modules**
  - Substrate less modules
  - Incorporating discrete devices
Conclusions

- Advanced packaging technology can deliver substantial space and volume savings for electronic medical devices

- Embedded die technology suits medical applications
  - Low tooling costs for low to mid volumes
  - Extreme miniaturization in all three axis

- Stacked embedded die is a low cost credible alternative to TSV
  - No need for dedicated chip designs, uses available bare die

- Chip scale as opposed to wafer scale
  - More accessible for medium volume applications wanting to use existing semiconductor solutions
Thank you!

For more information: [www.microsemi.com/design-support/package-miniaturization-services](http://www.microsemi.com/design-support/package-miniaturization-services)