Building High Reliability into Microsemi Designs with Synplify FPGA Tools

Microsemi Space Forum 2015, Synopsys
Agenda

- FPGA SEU mitigation industry trends and best practices
  - Market trends
  - What’s needed and when
- Current solutions
  - Overview FPGA design tools
  - Hardware debug and operation visibility
  - DO-254 support
  - SEU mitigation circuitry creation and error monitors
- New best practices → What’s next?
  - Local TMR best practices
  - Validating that TMR occurred and that it works
  - Error monitoring and access
  - Solutions for Microsemi RTG4
FPGA Military/Aerospace Solutions

- Mil/Aero market trends for FPGA systems
  - Need highest datapath performance in smallest area
  - High reliability and SEU error mitigation
  - Strict processes for circuit creation and verification
  - Reliable operation in harsh and high radiation environments
  - Support for multiple FPGA vendor suppliers

- Synplify FPGA solutions provide
  - DO-254 support and process compliance
  - Debug operating design in RTL
  - Automation of high reliability design techniques
  - Highest system performance in smallest area
  - Support for Verilog, VHDL, VHDL-2008 and System Verilog

Synplify enables high reliability, fast runtimes and deep debug
Synplify Premier offers 10x Faster Hardware Bring-up for Microsemi FPGAs

- Single-pass design debug
  - Upfront RTL and constraint checks
  - Finds all errors in a single compile
  - Diagnostic reporting
  - Fast synthesis (low QoR) mode

- Highly Reliable Automation
  - Hamming-3 error detection and correction design automation

- Quickly apply improvements
  - Hierarchical & incremental flows
  - Multi-machine synthesis

Early Bring-up | Highly Reliable Design Automation | Earlier Completion
---|---|---

Synplify Premier

Accelerated Software Development
Earlier System Testing
Why is There a High Reliability Problem?

- Radiation-induced circuit glitches (SEUs, SETs)
- Power rail glitch
- Power supply glitch or brown-out
- Meta-stability due to design flaws (failure to synchronize the circuit)
SETs and SEUs

Glitches clocked into a synchronous element can cause operation errors and ultimately system failure

- Impacts memories, registers, state machines

**SET** (Single Event Transient)
A current spike or “glitch” in a signal that occurs due to ionization or electromagnetic radiation

**SEU** (Single Event Upset)
Incorrect signal (SET) captured by a synchronous element that impacts its internal state and/or output
SEUs Cause Incorrect Behavior or FSM Failure

A flip in a register bit within an FSM can cause what was assumed to be an “unreachable” or “invalid” state to be reached.

RTL others clause that would handle state transition behavior out of an unreachable state is optimized away by default by the synthesis tool.
Synplify Premier Automates Design for High Reliability

- Monitor for Soft Errors “Bit flips”
- Restore Stable Operation

Control Logic and FSMs

- Safe FSMs w/ Hamming-3
- Local and Distributed TMR

Memories

- RAM TMR
- ECC RAM Inference

User Logic, I/O’s

- Distributed TMR
- I/O Replication and Error Monitoring

Preserve Critical Circuitry

High Reliability Reporting

Duplicate w/ Compare Triggers Scrubbing

Duplicate with Compare

*Not supported for Microsemi
## Radiation-Induced Error (SEU) Mitigation

<table>
<thead>
<tr>
<th>Device Type</th>
<th>RAD-HARD</th>
<th>Anti-Fuse/Flash</th>
<th>SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register</td>
<td>Low</td>
<td>Moderate</td>
<td>Low</td>
</tr>
<tr>
<td>Block RAM</td>
<td>Very High unless Error Detection &amp; Correction used</td>
<td>Very High unless Error Detection &amp; Correction used</td>
<td>Very High</td>
</tr>
<tr>
<td>Logic Cells</td>
<td>None</td>
<td>None</td>
<td>High</td>
</tr>
<tr>
<td>Routing Matrix</td>
<td>None</td>
<td>None</td>
<td>High</td>
</tr>
</tbody>
</table>

Current Solutions

Overview FPGA design tools
Hardware debug and operation visibility
DO-254 support
SEU mitigation circuitry creation and error monitors
Synopsys FPGA Design Suite

Algorithmic Modeling
- Synphony Model Compiler
- Identify RTL Instrumentor

RTL Synthesis and Analysis
- Logic Synthesis
  - Synplify Pro®
- Logic & High-Rel Synthesis
  - Synplify® Premier

Simulation
- VCS Simulator

FPGA Place-and-Route Tools

FPGA-Based Production Board

In-System Debug
- Identify RTL Debugger
Synphony Model Compiler Overview

Save Months in Design/Verification of Signal Processing Systems

Signal Processing IP library

High-Level Design and Verification from Simulink/MATLAB

High-performance verification for RTL and C-model system simulation

Synphony Signal Processing IP Library

High-Level Design (Simulink/MATLAB)

Synphony Model Compiler High-Level Synthesis

Synplify for Microsemi

Verification

- Multi-device
- DSP Mapping
- Timing Closure

- RTL Testbench
- C-Models
- Prototypes

- Microsemi provides “Synphony Model Compiler” software distribution for Microsemi FPGA devices
- Synopsys enables Synphony Model Compiler product enabling all FPGA devices
Synplify Debug Provides Simulator-Like Visibility into FPGA Hardware Operation

- Faster debug & higher design visibility
  - Traditional debug takes too long
  - Logic analyzers are insufficient
  - Debug at speed in system required
- Debug were you design
  - Instrument/debug directly in RTL
  - Quickly select signals for sampling/triggering
  - Capture signals at real-time speed
  - Powerful triggering for pinpointing a fault
  - Explore state spaces and conditions not easily reached by simulation
  - Integrated with Synplify Premier

- Microsemi provides “Identify” software distribution for Microsemi FPGA devices
- Synopsys enables Synplify Premier and Identify products enabling all FPGA devices
Identify Enables Requirements Traceability after Synthesis Optimizations

Synthesis performs optimizations
- Can cause debug node being absorbed or transformed
- No longer able to trace or probe these nodes
- Cannot relate their behavior in system back to your RTL

Instrument with Identify
- Nodes of interest preserved
- Relate behavior on board at nodes back to the RTL

RTL representation

Optimized Gate Level Netlist
Synplify Enables DO-254 Compliant Process

**Traceability**
- Schematics for Documentation
- Timing Reports and Log files
- Safe FSM and TMR Reports

**Repeatability**
- Reproducible synthesis results
- Lock down pre-verified blocks
- Best Practices Safety-critical design

**Equivalence**
- Simulator Integration
- Node preservation control for equivalence assurance & requirements trace
Clock Domain Synchronization Assurance
- Report alerts you to meta-stability problems due to design flaws such as failure to synchronize the circuit

Preservation of Debug Circuitry and of Custom Error Detection and Mitigation Circuitry
- Implementation during synthesis of RTL “others” clause that specifies your custom error mitigation circuitry
- Attributes to designate “preserve during synthesis nodes needed for probing and debug, or for equivalence proving purposes”

```
always @ (in1,present_state)
case (present_state)
  s0 : ...........
  s1 : ........
  s2 : ........
  s3 : ............ //no transition into S3
default : next_state <= s3;
endcase
```
Single Event Upset Mitigation Practices

- Antifuse/flash device registers can be moderately susceptible to SEUs
- FSMs contain registers

<table>
<thead>
<tr>
<th>Resource</th>
<th>Recommended solution</th>
<th>Synplify Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Registers</td>
<td>Local TMR</td>
<td>Synplify Pro</td>
</tr>
<tr>
<td>FSMs</td>
<td>Hamming-3 Automatic Error Correction</td>
<td>Synplify Premier</td>
</tr>
<tr>
<td></td>
<td>Specify how to return FSM from “unreachable state” to safe state by specifying and preserving the RTL “others” clause</td>
<td></td>
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TIP: Be sure to instruct the synthesis software to preserve error-mitigation circuitry.
New Best Practices … What’s Next?

Local TMR Best Practices
Validating that TMR occurred and that it works
Error monitoring and access
Solutions for MicroSemi RTG4
New Industry Trends and Best Practices

- TMR clock enable feedback loop in Local TMR & Distributed TMR circuitry
- Ways to determine “what best to TMR”
- Validation that TMR occurred
- Physical Separation of Triplicates

Synopsys is refining these solutions within Synplify Premier
Local TMR Best Practice

Enhances Local TMR implementation to include feedback from voter

Noncomprehensive implementation

Best practice implementation

Handles CE DFFs including feedback from voter to hold logic of DFFs

Available in Synplify Pro and Synplify Premier
Validating that TMR Occurred

Synplify Premier reports and confirms where SEU mitigation circuitry implemented:
- For Local TMR and Distributed TMR, Safe FSM
- Voter logic, sequential loops, error monitoring, comparator gates, pipestage resources
Error Monitoring & Access – FSM Example

- Synthesis Attributes specify Error Nets to be monitored
- Synthesis creates error-monitoring logic and makes Error flag signal accessible
  - set_option –safe_case 1

```
syn_create_err_net { -name {error_flag} -inst {i:state[1:3]}}
syn_connect -from {{n:error_flag} -to {t:EMIP.err_port}}
```

STATE ERROR MONITORING LOGIC
Automatically created to find errors
ECC, DTMR, RAM, TMR and Safe FSM

ERROR FLAG (EMIP)
Indicates state errors
2015.09 Release Synplify Premier
Synplify Premier MicroSemi RTG4 Solution

- Safe FSM
  - syn_encoding = safe
  - Using preserve & decode unreachable states logic

- Sequential logic and FSMs – Hamming 3 error detection and correction (EDAC)

- Support for Block RAMs
  - Inference of ECC block RAMs
  - Access to error bits similar to duplicate and compare.

- Local TMR for registers not required

RTG4 design solution available in 2015.09 Synplify Premier release
More Information on Design for High Reliability

White Paper

App Note

High Rel Webinar

http://www.synopsys.com/fpga

And visit us at our booth
Synplify Enables SEU Mitigation Methodologies

- Enhanced Local TMR and Distributed TMR for CE DFF
- TMR Reporting Trade-off Analysis and Control
- TMR and Safe FSM reporting and/or visualization
- Fault injection for Safe FSM and TMR (future technology)
- Ease of validation of error recovery
- Error Flag implementation

BEST PRACTICES
Microsemi Corporation (MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,600 employees globally. Learn more at www.microsemi.com.

Thank You