



RTG4 Enabled by Microsemi Power Technology Portfolio

Microsemi Space Forum 2015

Ken O'Neill, Director of Marketing, Space and Aviation

Brian Wilkinson, Sr Director Technical & Strategic Marketing & Applications



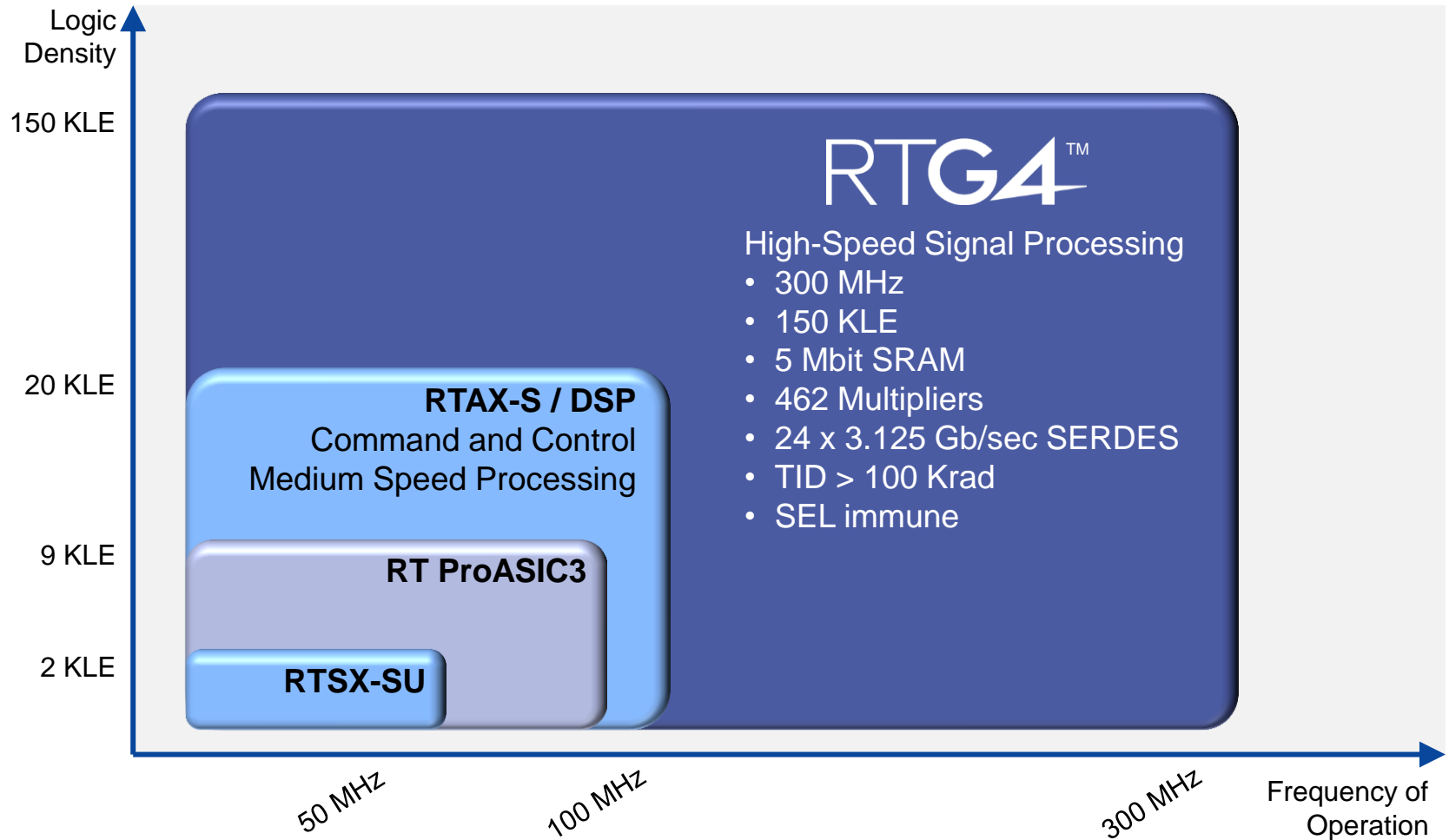
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SPACE FORUM

RTG4 Overview and Power Requirements

Agenda

- RTG4 product overview
- RTG4 power requirements
- Microsemi power components and systems

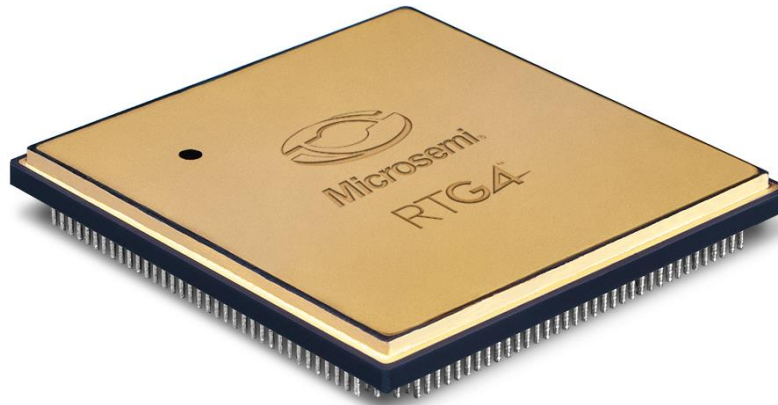
Introducing RTG4 High-Speed RT FPGAs



***RTG4 mitigates risks of ASICs and SRAM FPGAs, and has
20X improvement in signal processing throughput***

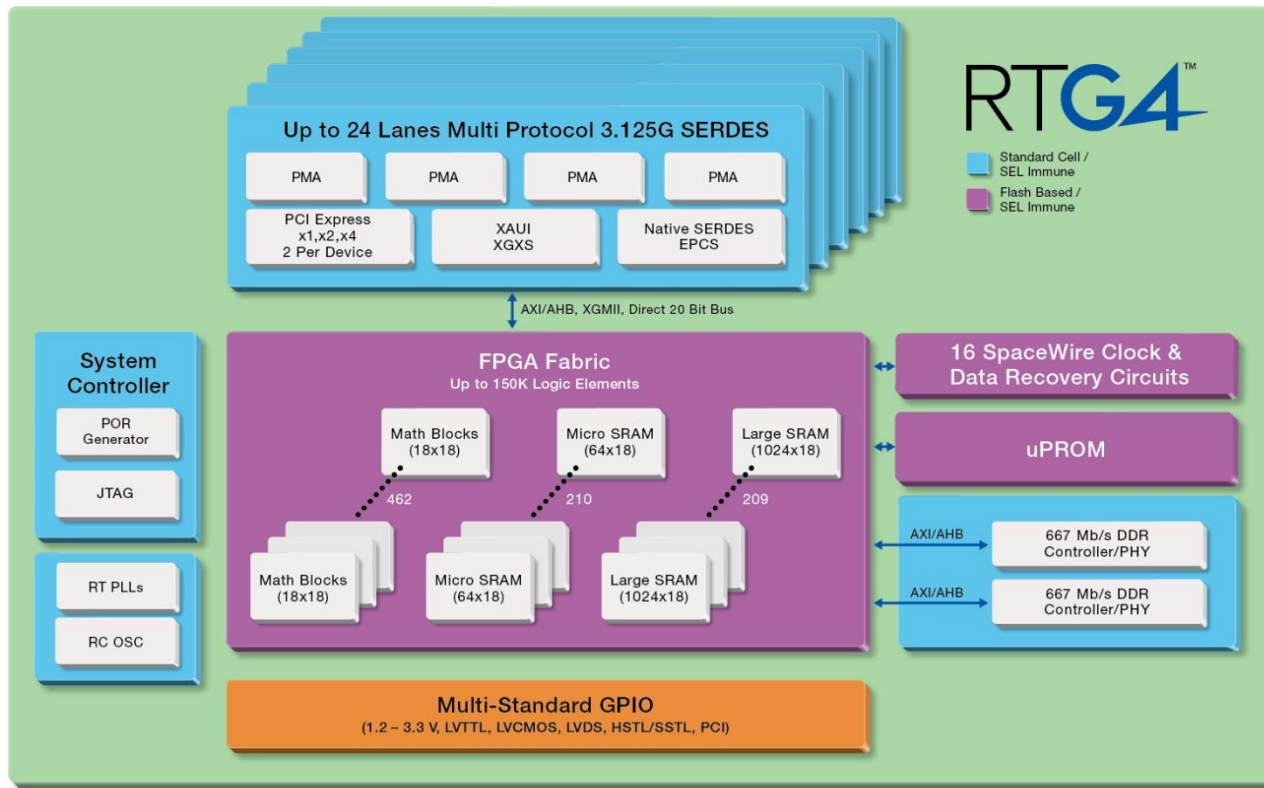
Why RTG4 is Compelling

- More flexible than an RH ASIC
 - Reprogrammable, no NRE, no cost and schedule risk
- More signal-processing features than any other RT FPGA
 - More registers, combinatorial logic, multiply blocks, and transceivers
 - Lower power, live at power-up, no external boot memory needed
- Radiation enhanced for Geosynchronous Earth Orbit and deep space
 - RTG4 65nm Flash has complete immunity to configuration upsets (SEU)
 - Total ionizing dose (TID) and single event effects (SEE) hardened by design



RTG4 offers groundbreaking features for satellite applications

RTG4 Radiation-Mitigated Architecture



- Total-dose hardening of Flash cells
- Single-event hardening of registers, SRAM, multipliers, PLLs

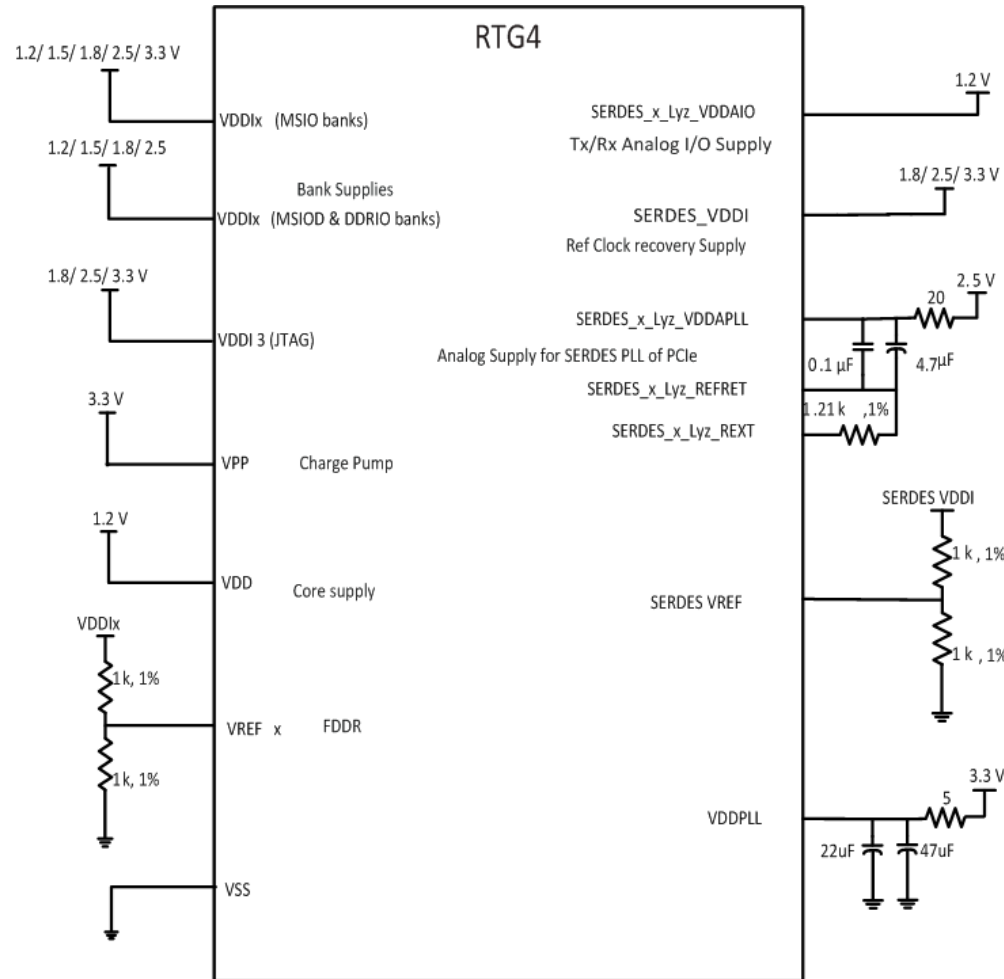
***Comprehensive radiation-mitigated architecture
for signal processing applications***

RTG4 Family Resources

Resources	RT4G075	RT4G150
Logic Elements (TMR Register + 4-Input C Logic)	77,712	151,824
18x18 Multiply-Accumulate Blocks	224	462
RAM Mbits (1.5 Kbit and 24 Kbit Blocks, with ECC)	2.8	5.2
UPROM Kbits	254	381
DDR2/3 SDRAM Controller (with ECC)	2x32	2x32
PCI Express Endpoints	2	2
Globals	24	24
PLLs (Rad Tolerant)	8	8
SpaceWire Clock & Data Recovery Circuits	16	16
User IO (excluding SERDES)	528	720
SERDES lanes (3.125 Gbit/sec)	16	24
Hermetic, Ceramic Column-Grid Packages		
CG1432 (Six Sigma Columns)	✓	
CG1657 (Six Sigma Columns)	✓	✓

- RT4G150 is the first device, available now in Engineering Samples
- RT4G075 availability TBD

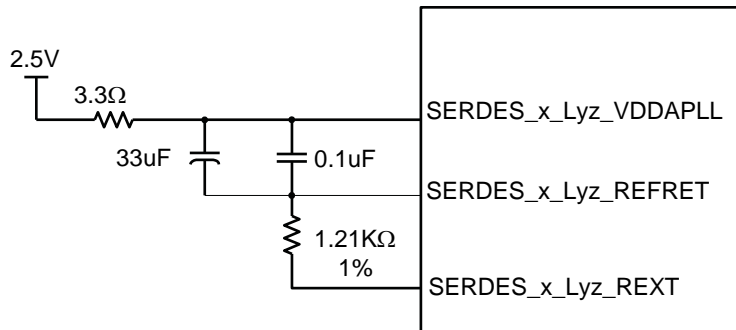
Power Supplies



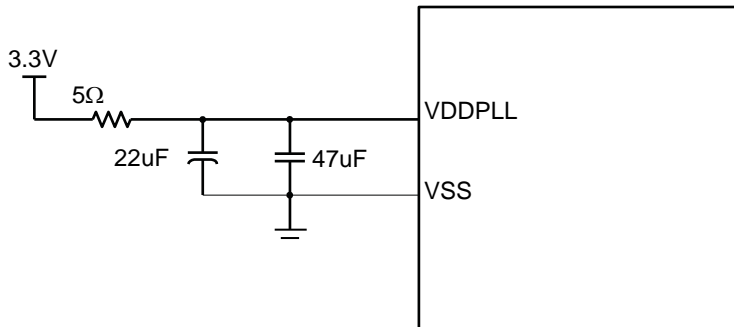
Supply	Voltage	Description
VDD	1.2 V	Core supply voltage
VPP	3.3 V	Power supply for device charge pumps
VDDPLL	3.3 V	Power for eight corner PLLs, PLLs in SERDES PCIe/PCS blocks, and FDDR PLL
VDDIx	1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V	Bank supplies
VREFx	0.5 * VDDIx	FDDR reference voltage
SERDES_x_Lyz_VDDAIO	1.2 V	TX/RX analog I/O voltage for SERDES lanes.
SERDES_x_Lyz_VDDAPLL	2.5 V	Analog power for SERDES TXPLL and CDRPLL
SERDES_VDDI	1.8 V, 2.5 V, or 3.3 V	Power for SERDES reference clock receiver supply.
SERDES_VREF	0.5 * SERDES_VDDI	External differential receiver reference voltage for SERDES Reference Clocks

Analog Supplies

SERDES VDDAPLL Supply



FPGA PLL Supply



- External R-C filters provide filtering to sensitive analog PLL supplies.
- SERDES PLL = 2.5V
 - SERDES TXPLL and CDRPLL supply
 - SERDES Calibration resistor(REXT). 1.21KΩ
 - impedance calibration (transmit, receive, and receiver equalization)
- FPGA PLLs = 3.3V
- Place all passive components as close to device as possible.

Power Supply Specifications

- Key power supplies must comply to the specifications including operating range, POR trip points, and power supply ramp rates

Symbol	Description	Min	Typ	Max	Units
VDD	Core Supply Voltage	1.14	1.2	1.26	V
VPP	Flash operating voltage	3	3.3	3.45	V
VDDt	Power ON Reset Threshold for VDD supply		0.8		V
VPPt	Power ON Reset Threshold for VPP supply		2.6		V
VDDr	VDD Power supply ramp rates (from GND/0V) for all power supplies	0.006		24	mV/ μ s
VPPr	VPP Power supply ramp rates (from GND/0V) for all power supplies	0.016		66	mV/ μ s
	Monotonicity of VDD/VPP/VDDIx required through its rise time	Yes			
Tvddpor	Power Up to Functional time (From VDD/VPP/VDDIx ramp to beginning of device ready		60		ms

Power Supply Decoupling Capacitors

- Proper on-board power supply decoupling is required
 - Keep decoupling caps close to pin (use 402's where possible on underside)
 - Distribute overall decoupling capacitance around the device perimeter
 - Use blind vias to remove crosstalk risk and cap surface mount area
 - Use larger power vias to reduce inductance – especially for high layer count boards
- PME (Precious Metal Electrode) decoupling caps within the FPGA package enhances overall PCB decoupling

Pin Name	Internal PME capacitance available for CG1657 package
VDD	2.2uF/4V
VDDI0	2.2uF/4V
VDDI1	2.2uF/4V
VDDI2	2.2uF/4V
VDDI4	0.68uF/6.3V
VDDI5	0.68uF/6.3V
VDDI6	0.68uF/6.3V
VDDI7	2.2uF/4V
VDDI8	2.2uF/4V
VDDI9	2.2uF/4V
VDDPLL	2.2uF/4V

Radiation Tolerant Power Supplies

- Microsemi provides many Radiation-Tolerant components that can be used to supply power to RTG4 FPGAs
- Engineers should consider the following when selecting power supply components
 - Calculate required power of the RTG4 device
 - PowerCalc spreadsheet, SmartPower tool in Libero design software
 - Select an appropriate Radiation-Tolerant regulator that can supply the required power and meet all power requirements of RTG4
 - Radiation-Tolerant Linear-Regulator (Microsemi)
 - Radiation-Tolerant Switching regulator (Microsemi)

Current Requirements

- Use RTG4 Power Calculator to estimate current required
 - Available on Microsemi web site [RTG4 Power Calculator](#)
 - Need to enter specific details for your design
 - Example is for 99% utilized RT4G150 – total 6.7W
 - 4 fast clocks (150MHz to 250MHz), 2 slow clocks (25MHz and 50MHz)
 - 496 I/O (400 LVCMOS, 66 PCI, 32 LVDS)
 - 8 Lanes of transceivers (2.5Gb/sec)

Current Summary			
Rail Breakdown			
Rail Name	Current (mA)	Voltage (V)	Power (mW)
VDD	3928.71	1.200	4714.45
VDDI 1.2	33.96	1.200	40.75
VDDI 1.5	0.00	1.500	0.00
VDDI 1.8	0.00	1.800	0.00
VDDI 2.5	535.42	2.500	1338.56
VDDI 3.3	14.73	3.300	48.61
SERDES_[01]_L[0123]_VDDAIO	287.38	1.200	344.86
SERDES_[01]_L[0123]_VDDAPLL	20.60	2.500	51.50
PLL_VDDA	60.00	2.500	150.00

Microsemi Power Solutions for RTG4

Cold Sparing

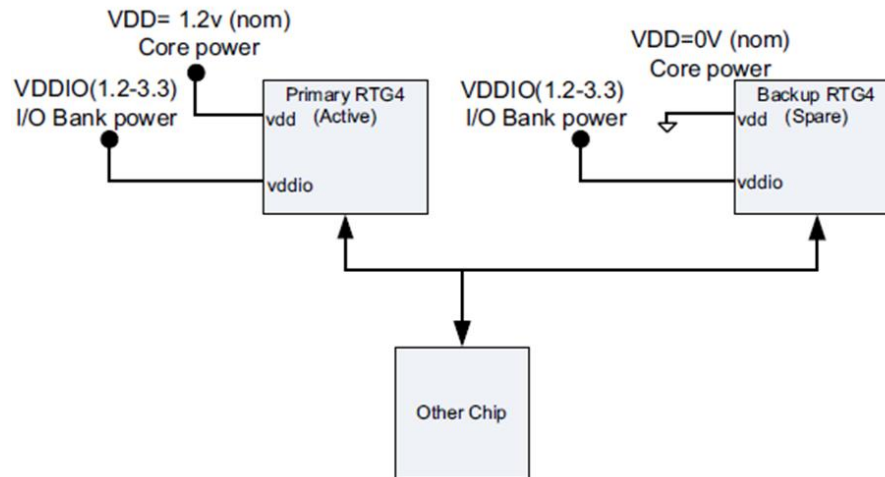
Advantages of cold sparing:

- Power-Up can be done in any sequence. (No Power supply sequencing requirements).
- No excess device leakage in spare device where implemented.

In cold sparing applications, voltage can be applied to device I/O's before and during power-up. RTG4 device is capable of cold sparing applications with the following strategies:

RTG4 Cold Sparing Strategies

- Example of a system board integrating two parallel RTG4 devices on the board with shared or common I/C connections.
- Primary RTG4 device has its core powered and fully functional until a point where a swap of devices is determined as necessary.
- Backup RTG4 device has its I/O banks powered to prevent I/O leakage through the ESD diode and fabric core un-powered. This establishes a low power, protected state for the backup RTG4 device.
- At any point, you can swap by powering down the core of the primary RTG4 device and power up the core of the backup RTG4 device going through its configuration sequence.
- Primary and backup devices are identical parts.
- Only one of the two devices might be active at one time.
- Core VDD high activates the part and low de-activates the part.
- The de-activate part must tie the VDD to the ground and must not be floating.



SA 50 Series Concept, isolated DC-DC

SMT Construction in an Industry Standard Package

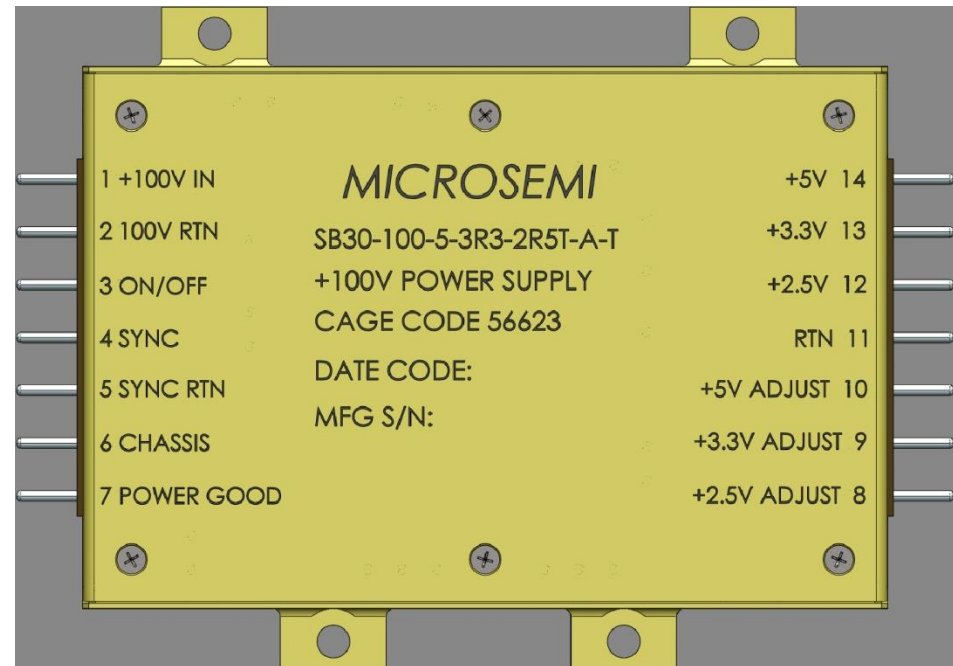


- Features:
- +28V or 120V nominal Inputs
- Internal EMI Filter (120V version)
- Triple, Dual and Single output versions
- Isolated Outputs
- 50W total combined power output
- Inhibit Feature
- Isolated Sync Input, 500kHz
- Output trim on Single & Dual Variants
- >86% efficient Full load @5 +/-15V out
- Length Width Height
- 3.055" x 2.055" x 0.50"
- Total Dose Rating of 200KRads
- Threshold (LET) with no latch-up
>80MeV-cm²/mg

SB 30 Series 30 Watt Family, isolated DC-DC

- Triple Output for Digital Loads
 - 5V @ 2A; 3.3V @ 3A; 2.5V @ 3A
- 30W total combined power output
- +28V or 100V nominal Inputs
- Internal EMI Filter (100 Vin only)
- Outputs individually regulated
- Power Good Status
- +/- 10% trim for each output
- Inhibit Feature
- Isolated Sync Input, 500kHz
- 75% efficiency
- 3.055 x 2.055" x 0.60"
- Total Dose Rating of 200KRads
- Threshold (LET) with no latch-up
>80MeV-cm²/mg

*SMT Construction in an Industry
Standard Package*



SB 30 Series 30 Watt Family, isolated DC-DC

- Designed to support multiple Low Voltage Digital loads
- Three independent outputs, each regulator with it's own PWM
- Multi Simultaneous Switching Outputs on one rail will not induce noise on an adjacent rail
- Excellent load step response
- Power up / power down sequencing built in
- Synchronize clock with other converters to reduce system noise
- For a nominal NRE, input / output voltages can be customized – consult PMG Microsemi

Isolated DC-DC converters in production

SA50-120-12S-B-P

SA50-120-12S-B-T

SA50-120-15S-A-H

SA50-120-15S-A-P

SA50-120-28S-B-H

SA50-120-28S-B-P

SA50-120-28S-B-T

SA50-120-3R3-14T-B-P

SA50-120-3R3-14T-B-TX1

SA50-120-5-12T-A-P

SA50-120-5-12T-A-T

SA50-120-5-15T-A-H

SA50-120-5-15T-A-P

SA50-120-5-15T-A-T

SA50-28-5-15T-A-H

SA50-28-5-15T-A-P

SA50-28-5-15T-A-T

SB30-100-2R5S-3R3-5T-A-H

SB30-100-2R5S-3R3-5T-A-P

SB30-100-2R5S-3R3-5T-A-T

- Input Voltages 28V, 100V & 120V Standard, others Custom
- Single Outputs: 3.3V, 5V, 12V, 15V, 28V Standard, others Custom
- Dual Outputs: Special Configurations of Triples
- Triple Outputs: 3.3V or 5V with 12V or 15V Standard, others can be available
- Case Style

A = leads out the side

B = leads out the top

Performance Level

P = Prototype

T = SEE Tolerant, TID Hard

H = SEE Hard, TID Hard

- Go To: <http://www.microsemi.com/product-directory/modules-a-hybrids/1450-dc-to-dc-converters>

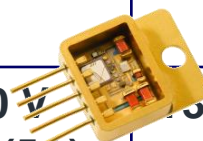
Also Available:

- Semi and full Customized Versions
- Filter Solutions e.g. SF200-28

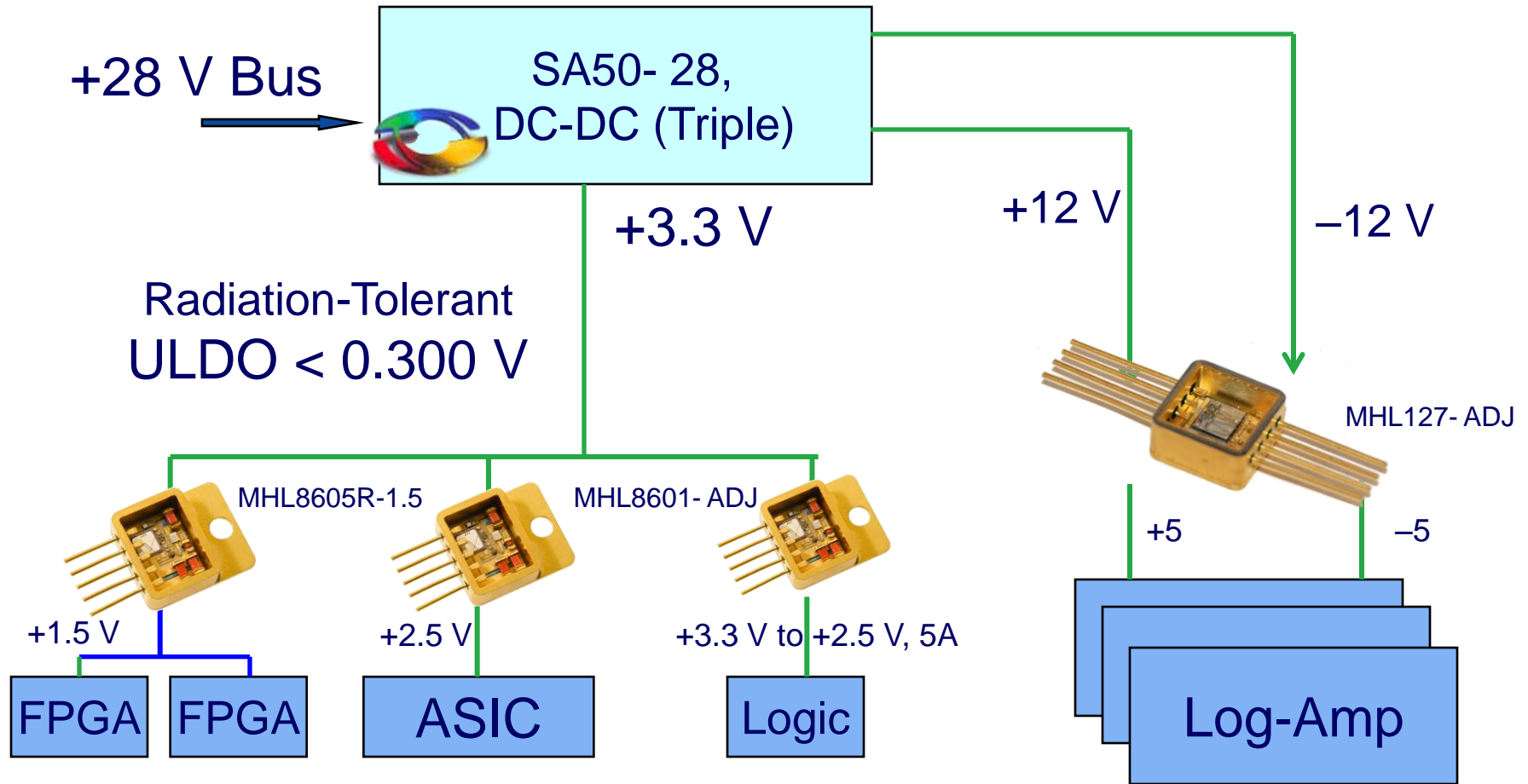
RHH- Linear Regulators



Product	Description	Critical Parameters	Vin Range	Vout Range
MHL8601	Pos., Linear, 3A Fixed or Adjustable	VLDO = 0.300 V (3A), Rad-Hard to 300Krad+	+3V to +5.5V	+1.26V to +4.5V
MHL8605	Pos., Linear, 5A, Fixed or adjustable	VLDO = 0.300 V (2A), 0.400 V (5A) RadHard to 300 Krad+	+3V to +5.5V	+1.26V to +4.5V
MHL8701/5	Pos., Linear, 5A, Fixed or adjustable, SEE = 82 MeV	VLDO = 0.400 V (2A) RadHard to 300 Krad+	+3V to +5.5V	+1.26V to +5.5V
MHL117	Pos. Linear, Adj., 1.25A, Vin = 40 V	RadHard to 300Krad	+5V to +37V	+1.21V to +4.5V
MHL127	Dual, $\pm 1A$, Pos. and Neg. Linear regulator	RadHard to 300 Krad	$\pm 5V$ to $\pm 40V$	$\pm 6.5V$ to $\pm 37V$

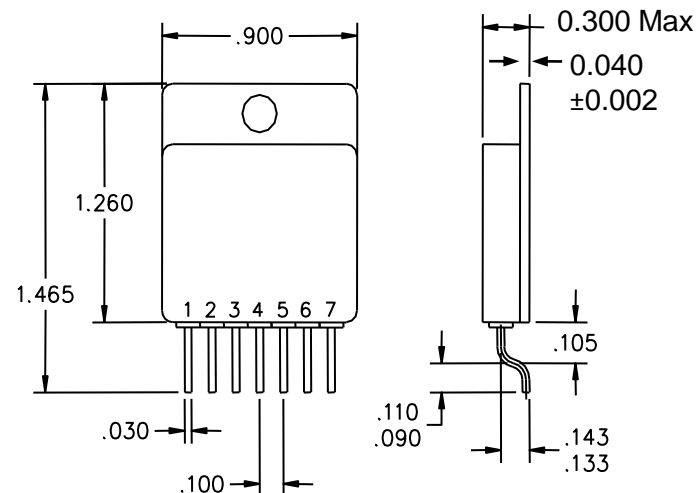


Linear Applications



ULDO Linear Regulator MHL8701

- The MHL 8701 series products are space qualified, ultra low dropout linear regulators designed for military and space flight applications. Assembled in a hermetic package, this series provides an ultra low drop out voltage of 400mV @ 2A. They are optimized for operation at +5V input or +3.3V input.
- Enhanced SEE performance, SET < 5% of Vout
- Thermal shutdown @ 150 °C
- Output Voltage: +1.26V to +4.5V
- Post Rad Output Voltage accuracy +/-6%
- Rad- Tolerant to 300 Krad HDR TID
- Rad- Tolerant to 100 Krad Eldrs .01 rads(si)/sec
- LET= 85 MeV (Au ions) No Latch-up
- Fixed & Adjustable output voltages
- 7 Pin Power SIP
- Available Now



New Product

RHH- POL's

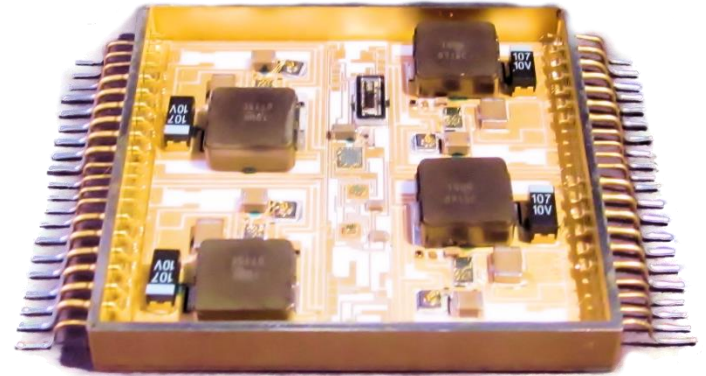
Product	Description	Critical Parameters	Vin Range (De-rated)	Vout Range
MHP8564A	Sw. Reg., 4.5A, Adj./Fixed	300 Krad, Iout= 4.0A	+4.5V to +8V	+1.21V to +4.5V
MHP8565A	Sw. Reg., 3.0A, Adj	300 Krad, Iout = 3.0A	+4.5V to +8V	+1.21V to +4.5V
MHP8566A	Quad Sw. Reg., Adjustable Vout, 15A	100 Krad TID, 15A Efficiency, 15A	+4.5V to +8V	+1.0V to +4.5V



RadHard Quad POL- MHP8566

- Rad-Tolerant to 100 Krad ¹
- Quad adjustable output to +1.21 V.
- Up to 16A output current (total of all outputs)
- Vin Range: +4.5 V to +8 V
(for +12 Vin consult factory)

Surface-mount package:
2.0 in. X 2.0 in. X 0.290 in.



42 pin flat pack = L 82.5 X W 82.5 X H 11.2 mm

- *Complete assembly – just add voltage set resistors.*

Configurable as four independent 4A POLs or one 16A POL

******FPGA Power Supply******



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Thank You



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Power Matters.™

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo, CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
email: sales.support@microsemi.com

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