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Space Power Development – Expanding Heritage with New Technology

Microsemi Space Forum 2015

Pat Franks,
Director of Engineering

Agenda

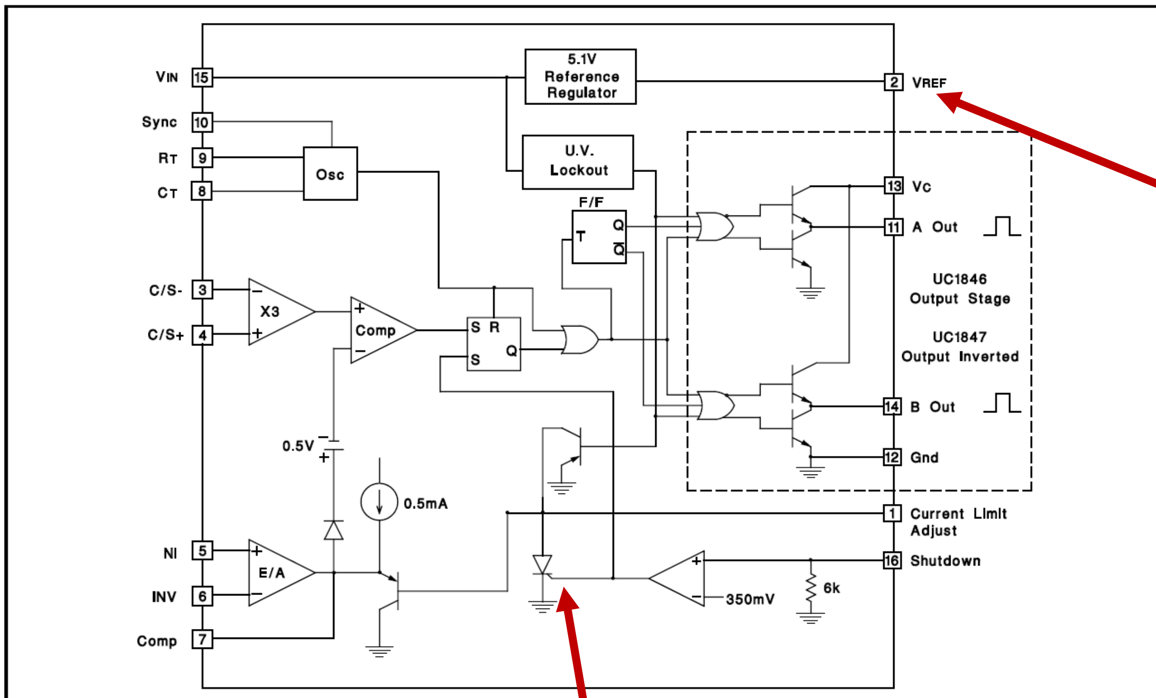
- Some topics arising from SPM's Custom Space Power Development Programs

  - Mitigation of SEE effects in PWM Controllers
  - An Introduction of SiC Technology to Space
  - Evolution of Intelligent Power Management
  - A complimentary venture in Aviation

Mitigation of SEE effects in PWM Controllers

PWM UC1846 Controller Radiation Issues

BLOCK DIAGRAM

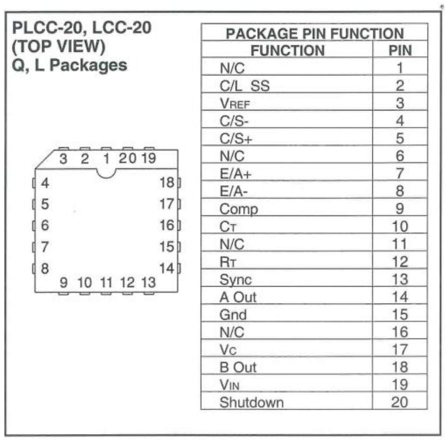


SCR

INTERNAL VREF DRIFT

Drift of the internal VREF is mitigated by using an external temperature compensated RADHARD voltage reference to maintain tight regulation.

SEE activates the SCR latch



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
C/L SS	2
VREF	3
C/S-	4
C/S+	5
N/C	6
E/A+	7
E/A-	8
Comp	9
CT	10
N/C	11
RT	12
Sync	13
A Out	14
Gnd	15
N/C	16
Vc	17
B Out	18
VIN	19
Shutdown	20

UC1846 SEU

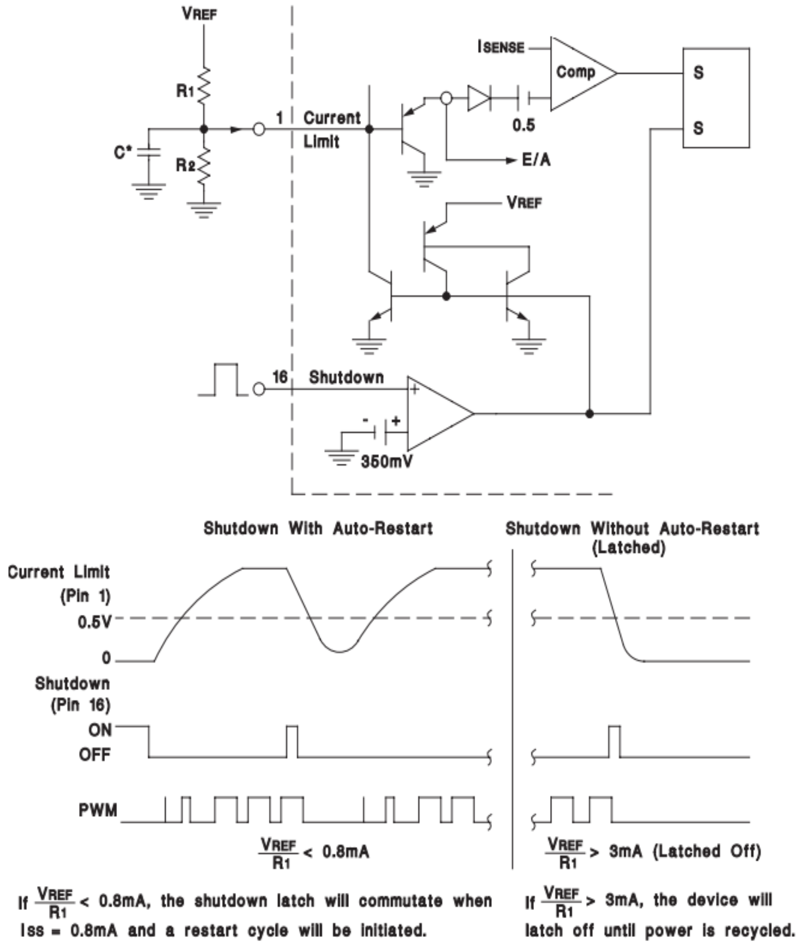


Figure 7. Soft-Start and Shutdown/Restart Functions

The UC1846 PWM IC has long space heritage. This PWM has been tested for single event transient performance by Lockheed and others and SEU performance reports are provided by Lockheed and NASA.

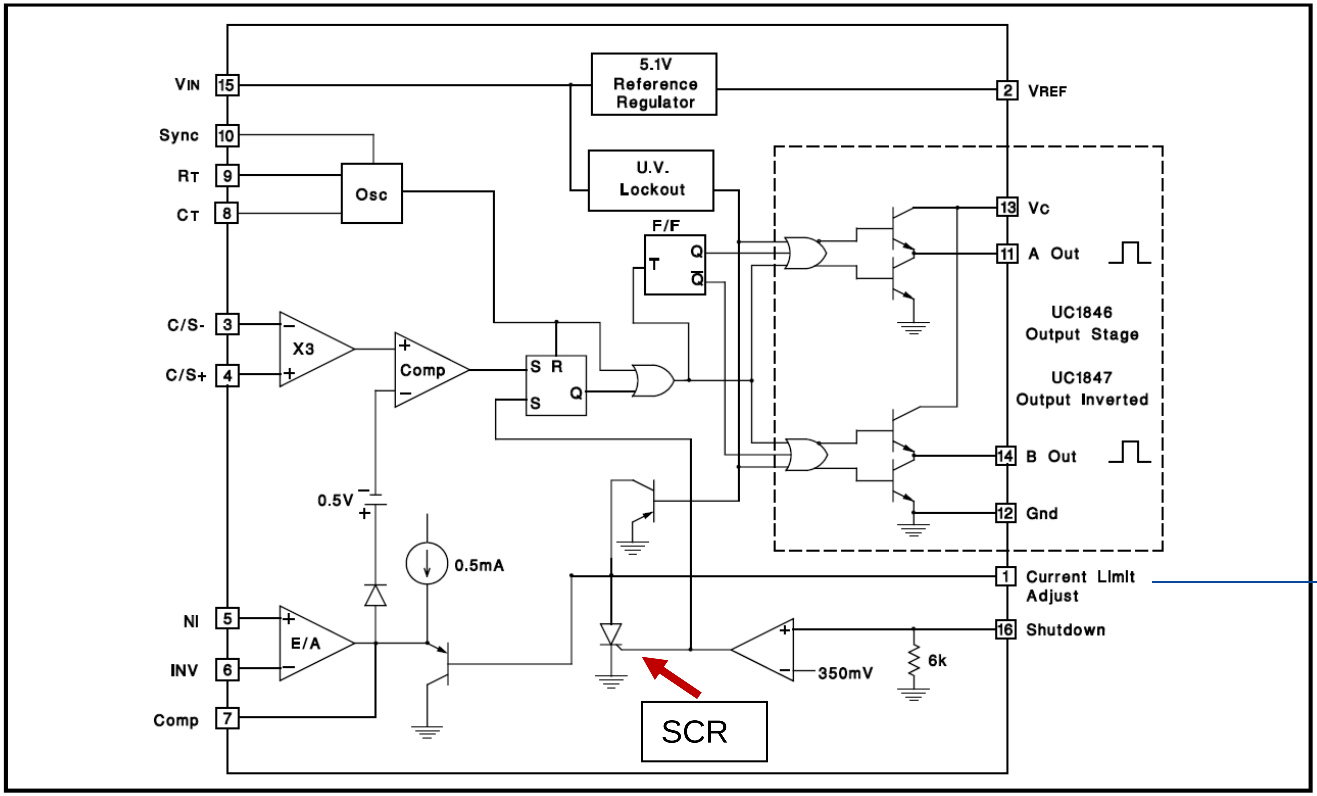
The conclusion is that SEE activates the SCR latch. The SCR latch is specified to remain latched as long as greater than 3 milliamp anode current is provided via pin 1, the Current Limit Adjust / Soft Start pin of the IC.

It has been demonstrated by SEE testing, circuit simulation and electrical test, that eliminating the anode current to the SCR latch, allows the SCR to reset in the order of micro seconds.

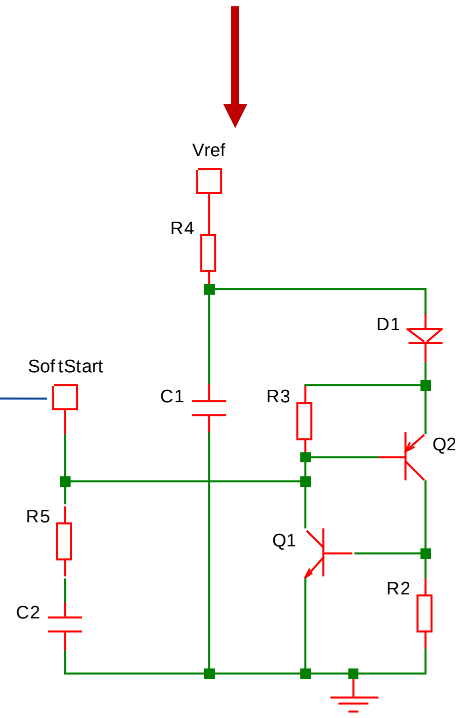
Solutions rely on eliminating the anode current to the SCR latch.

UC1846 SEU MITIGATION

BLOCK DIAGRAM

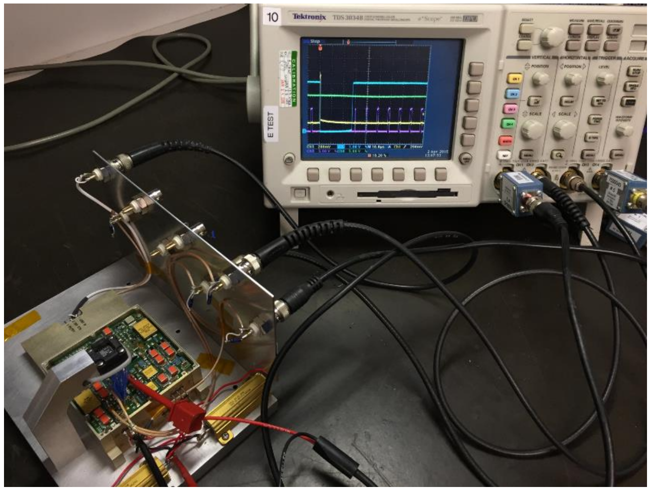


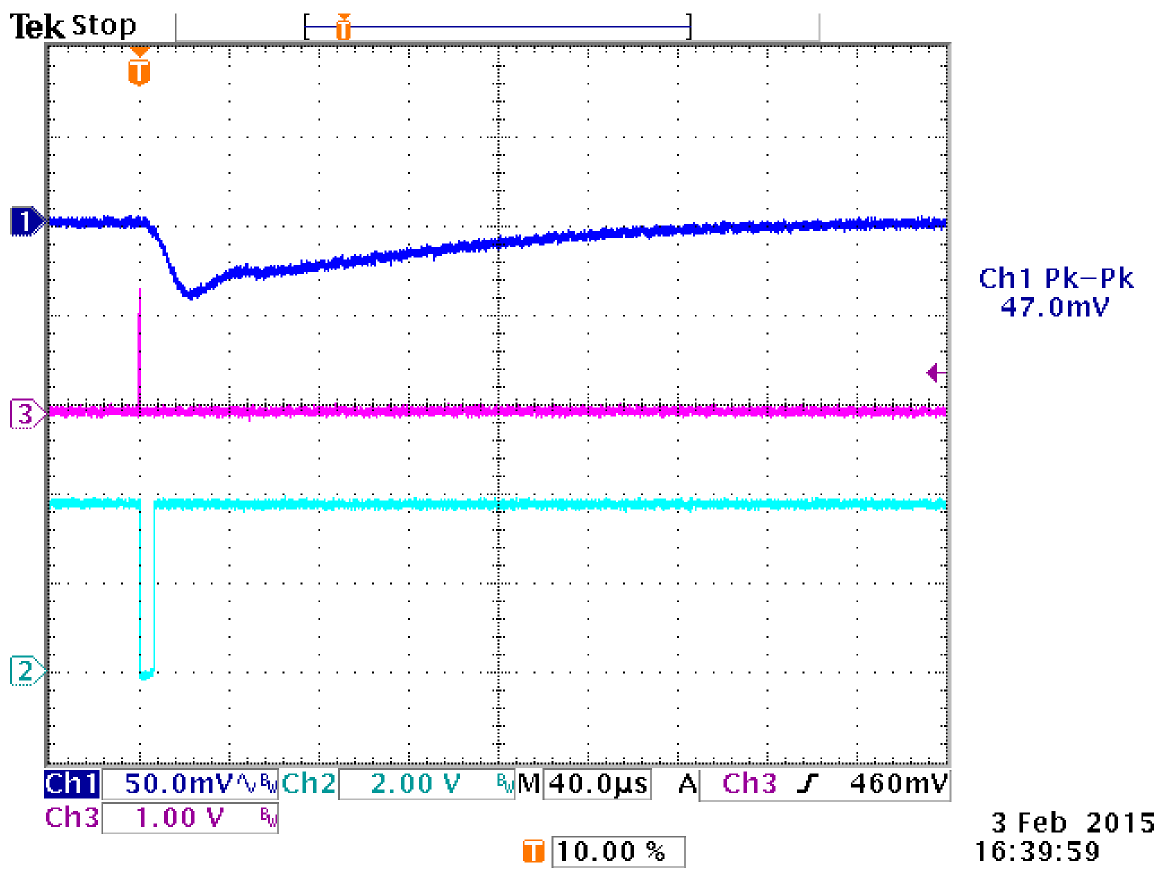
External Latch diverts current from internal SCR latch for sufficient time to ensure SCR Latch reset



Customer would not approve our Heritage circuit without validation!!

UC1846 SEU -LAB ELECTRICAL VERIFICATION





Output Voltage at max load

Ch1: Output Voltage at max load
Ch2: PWM- pin 1.
Ch3: applied pulse to PWM- pin 16 (SD) .

Customer still not convinced!!

UC1846 SEU – SEE TESTING AT LBNL

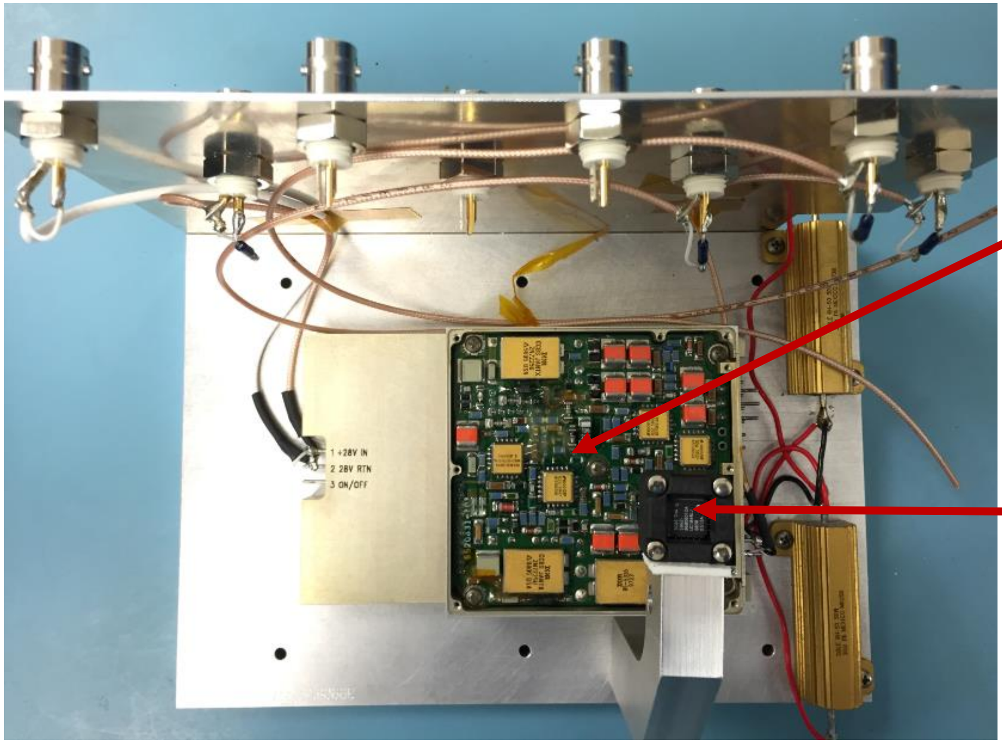
Lawrence
Berkeley National
Laboratory

UC1846 SEU -LAB RADIATION VERIFICATION

Table 5.2-1 10 MeV/n Heavy Ion Species Used During Characterization Testing

Ion Name	Symbol	Mass/ion/ charge state	Energy (MeV)	Linear Energy Transfer (LET_0) (MeV/(mg/cm^2))	Range (µm-Si)
Argon	Ar	$^{40}Ar^{+11}$	400.00	9.74	130.1
Vanadium	V	$^{51}V^{+14}$	508.27	14.59	113.4
Copper	Cu	$^{65}Cu^{+18}$	659.19	21.17	108.0
Krypton	Kr	$^{86}Kr^{+24}$	906.45	30.23	113.1
Silver	Ag	$^{107}Ag^{+29}$	1039.42	48.15	90.0
Xenon	Xe	$^{124}Xe^{+34}$	1232.55	58.78	90.0

UC1846 SEU – SEE TESTING



Heritage DC-DC Converter
"Host" Power Supply
Mitigation Circuit Identical to Customer's.

UC1846 specially extended on a socket to allow multiple evaluations

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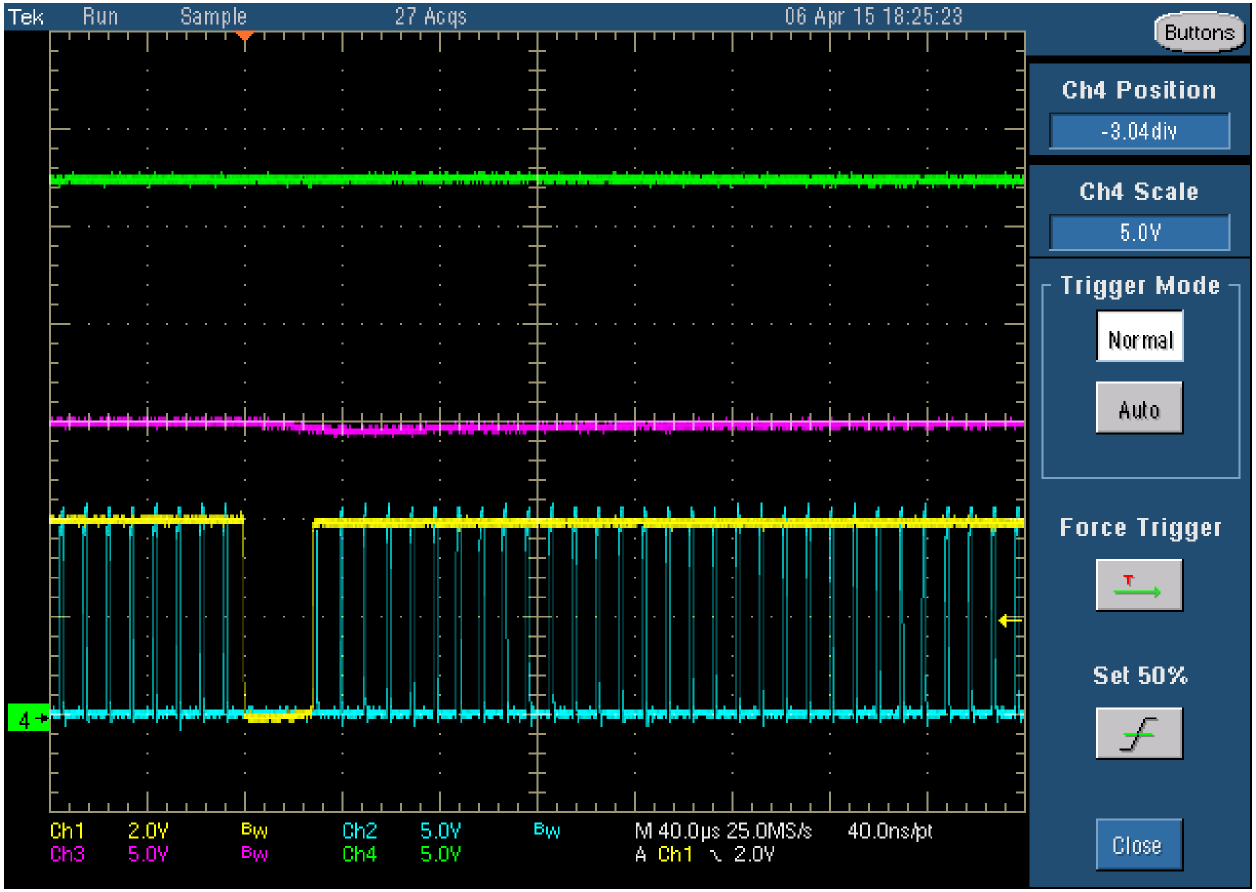
Radiation Test Results



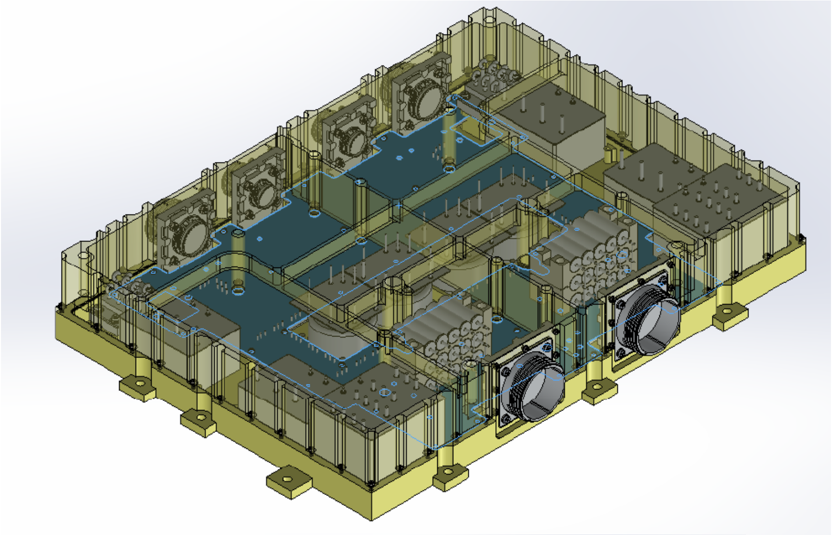
Output Voltage at max load

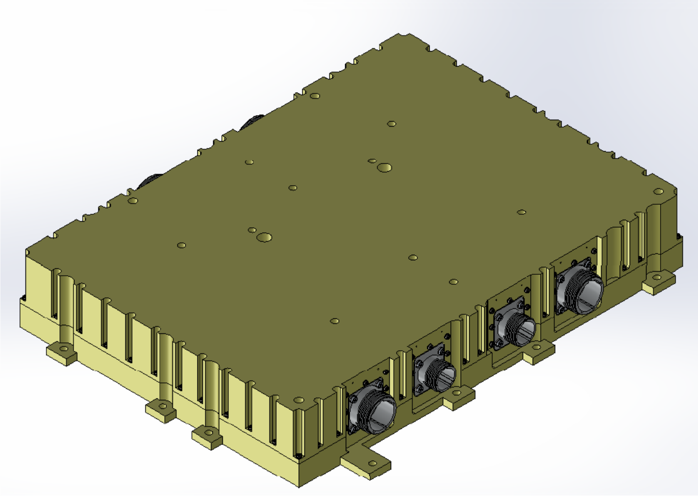
Ch1: PWM- pin 1.
Ch2: PWM output pulses
Ch3: Output Voltage at max load
Ch4: Input line voltage

An Introduction of Silicon Carbide (SiC) Technology to Space

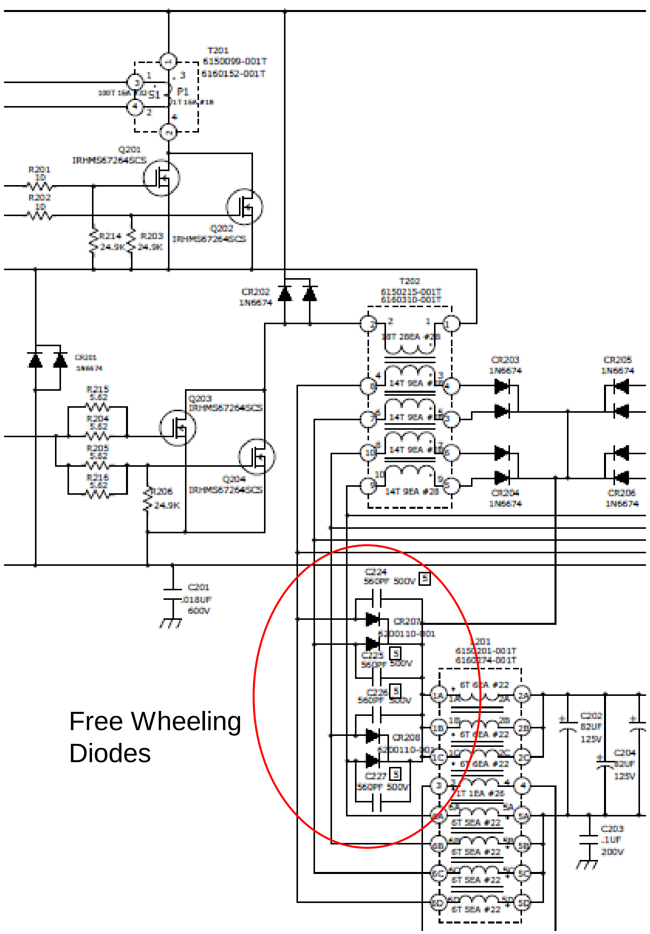
A Demanding System Requirement

- High efficiency essential
  - Mission duty
  - Heat Dissipation
- Precision current management
  - Balanced inputs
  - Individual & Joint Limit strategies
- Precision voltage output
  - Tight load transient response limits





Power Topology



Free Wheeling
Diodes

- Efficiency is an overarching requirement
- Two Switch Forward Topology
- Multiple Secondary's to promote current sharing
  - However not for freewheel current
- IN6674 Space qualified silicon diodes for all positions initially
- Problems with freewheeling diodes prompted substitution of SiC Diodes
  - Promotes electrical reliability
  - Promotes high efficiency

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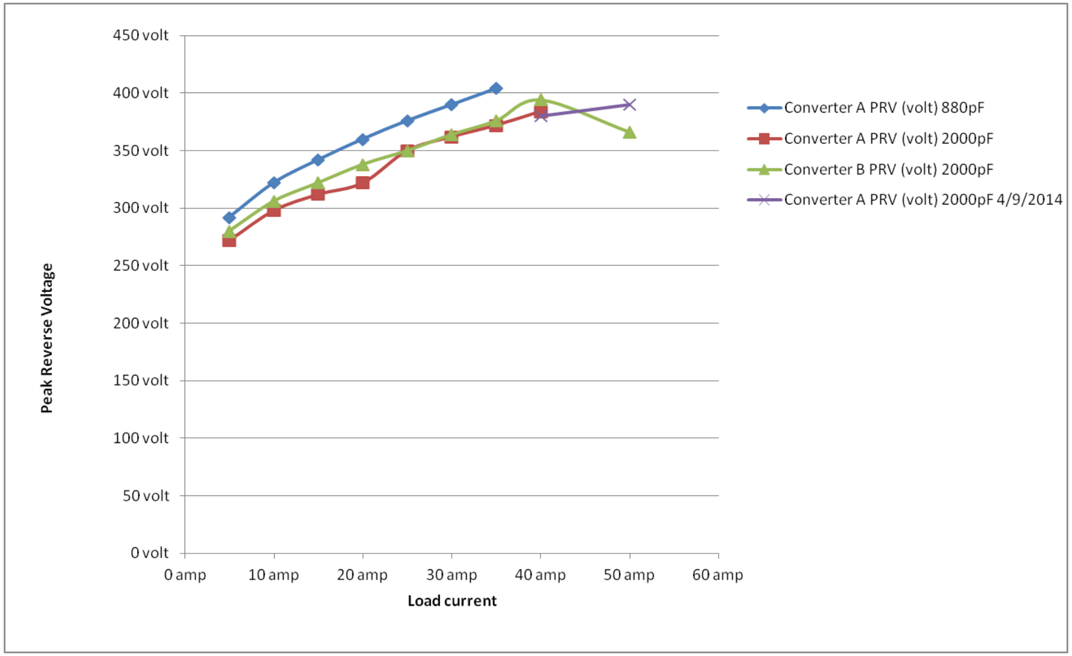
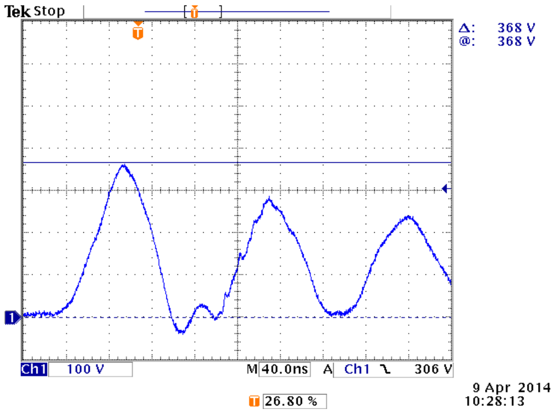
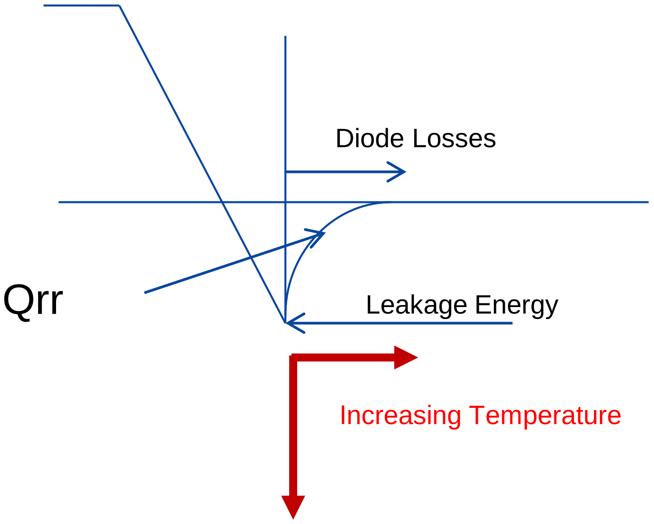
Silicon Diode Reverse Recovery Temperature Effect







- With increasing temperature:
  - Qrr increases, higher Irr peak and longer trr
  - Progressively Higher energy in Leakage inductance
  - Higher diode losses ----- potential for thermal runaway
  - Higher Peak reverse diode voltage stress
  - Performance and Risk unacceptable for the application

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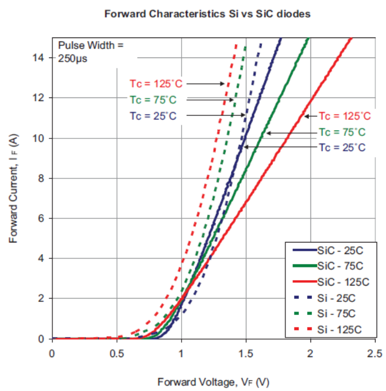
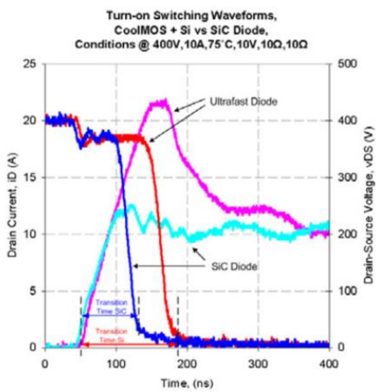
High Power DC-DC Converter benefits from SiC



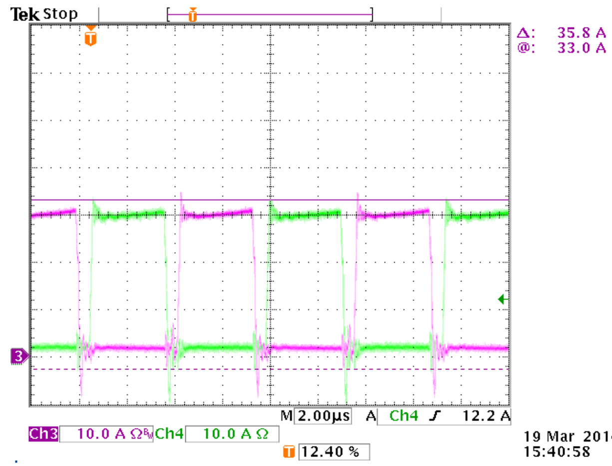
Comparison of Silicon and Silicon Carbide Forward Voltage Drops



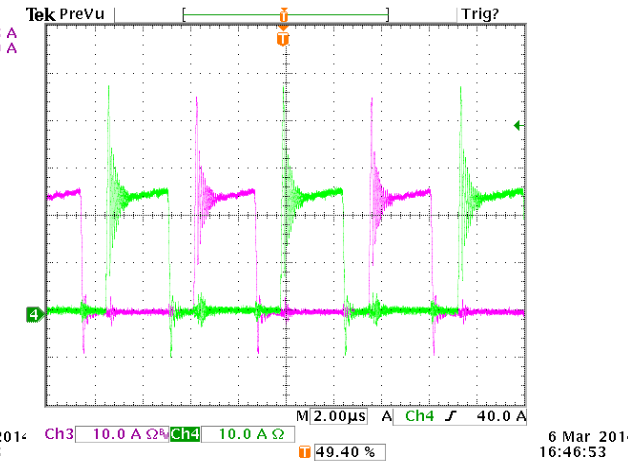
IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 28, NO. 1, JANUARY 2013 289

A Comparative Performance Study of an Interleaved Boost Converter Using Commercial Si and SiC Diodes for PV Applications

Carl Ngai-Man Ho, *Senior Member, IEEE*, Hannes Breuninger, *Member, IEEE*, Sami Pettersson, *Member, IEEE*, Gerardo Escobar, *Senior Member, IEEE*, and Francisco Canales, *Member, IEEE*



Current Driving a Silicon Carbide Free Wheeling Diode

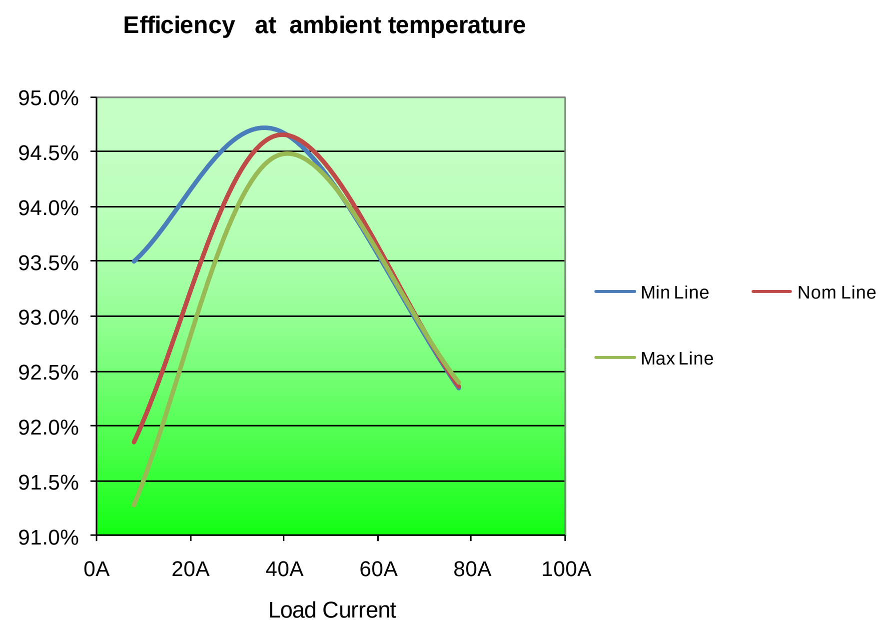


Current Driving a Silicon Free Wheeling Diode

- Forward voltage drop favors Silicon
- However the dominant loss in the topology comes from reverse recovery
- Silicon Carbide a clear winner with close to zero Qrr!!

Microsemi responds with a strong Inter-Divisional solution

- Initial proof of concept from a Plastic Package SiC Diode
  - Switched out on Brass Board
  - Plastic not acceptable for Space
- SiC Die from Microsemi Bend Oregon (PPG) {now DPG}
- Hermetic Packaging capability from Lawerence Mass (HRG) {now also DPG}
- Microsemi builds & qualifies a new hermetic SiC diode part in very short order
  - Recovery plan supports critical program schedule
  - Recovery plan necessarily includes full ENVIRONMENTAL and RADIATION assessments of the new SiC diode



Final efficiency of SiC version meets desired efficiency profile

Test Assets to support rapid evaluations

- Dedicated Test Station
  - Part Number 7500659
    - DC Source
    - Electronic Load
    - Data logger
    - Interface harness
    - Unique interface circuitry
- Standard equipment
    - Oscilloscope with probes
    - Thermal chamber
    - Thermal imaging
    - Spectrum analyzer

Early investment is paid back by test labor savings even in the first article

SiC Diode Chip from Plastic to Hermetic

SiC Microsemi

Microsemi

APT20SCD65K

650V 20A

NSD305 TO254 Kyocera BeO Metalize 102x102x15 SiC Dual Chips (1-Side) Tc=25C

MAXIMUM RATINGS T_C = 25°C unless otherwise specified.

Symbol	Characteristic / Test Conditions		Ratings	Unit
V_R	Maximum D.C. Reverse Voltage		650	Volts
V_{RRM}	Maximum Peak Repetitive Reverse Voltage			
V_{RWM}	Maximum Working Peak Reverse Voltage			
I_F	Maximum D.C. Forward Current	T_c = 25°C	32	Amps
		T_c = 90°C	20	
I_{FRM}	Repetitive Peak Forward Surge Current (T_c = 25°C, t_p = 10ms, Half Sine Wave)		75	
I_{FSM}	Non-Repetitive Forward Surge Current (T_c = 25°C, t_p = 10ms, Half Sine)		165	
P_{TOT}	Power Dissipation	T_c = 25°C	114	W
		T_c = 110°C	36	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to 150	

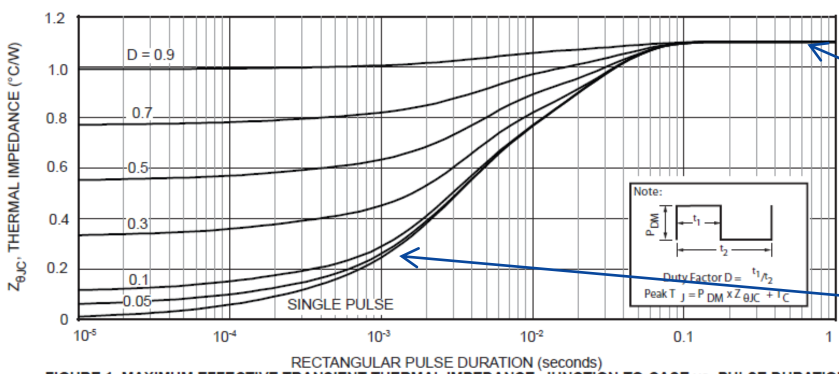
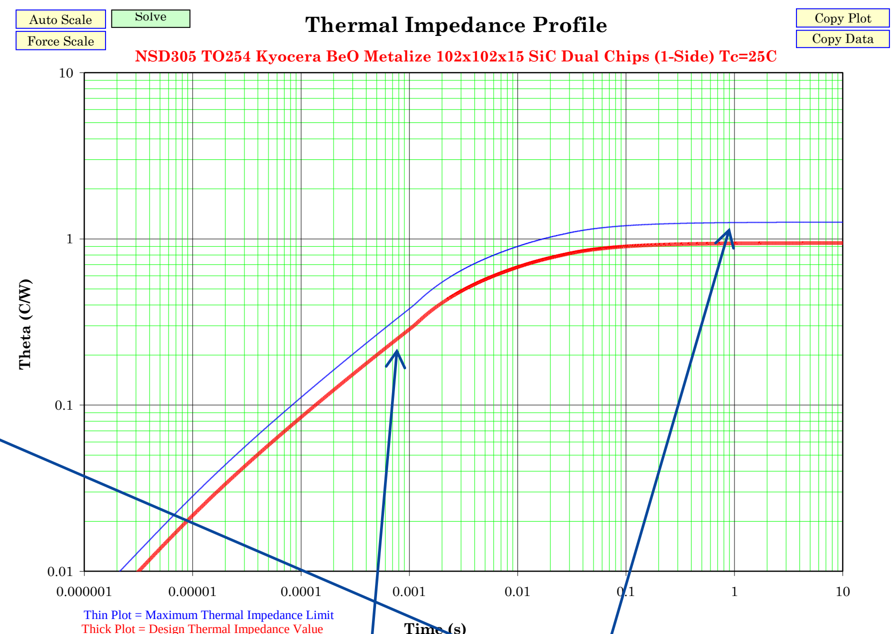


FIGURE 1. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs. PULSE DURATION



Data Similar ---- 0.3 @ 0.001 sec ; 1.1 @ 1 sec

- Early transient impedance plots indicate that ratings are very similar
- HOWEVER INITIAL TO254 Surge current screening @120A failed >50% devices
  - Suitable surge screening level an URGENT HOT TOPIC!!!

Revised Surge Current Test Requirements

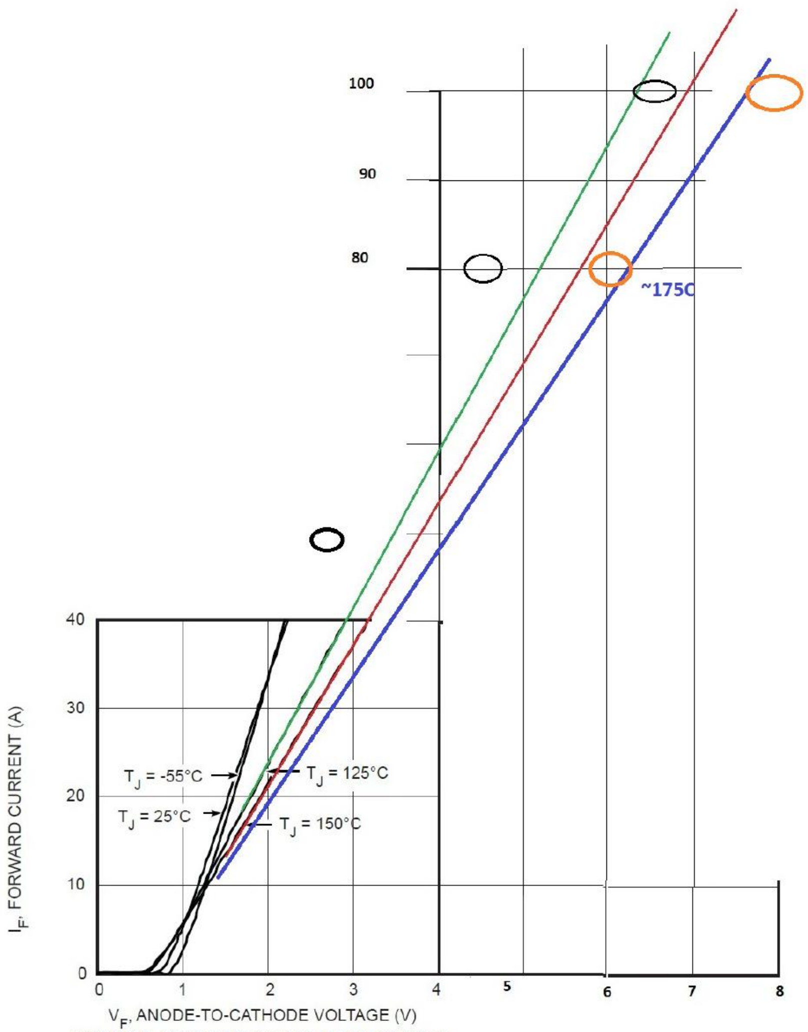


FIGURE 2, Forward Current vs. Forward Voltage

- Forward current as a function of forward voltage from Plastic Datasheet
- Black circles represent measured Vf values
- Orange circles represent effective Vf values adjusted for dynamic temperature rise
- Orange points assume 50% additional energy input due to dT/dt

Revised Surge Current Test Requirements

- Balanced risk principle
  - Strong enough to stress the diode and expose defects, die & attach
  - Not so strong as to weaken the diode reducing reliability & life
- Aim for a nominal Tj rise of 125°C (over 25°C ambient)
- Vf is a function of If and temperature
  - Die temperature rises during surge pulse
  - Need to account for dT/dt in total energy calculation
- Rational & assumptions developed in following slides
- Qualitative validation part of rational
  - Back off from point of failure

Revised Surge Current Test Requirements

Vf= 1.3017*exp(0.0181*If) (From Leas Squares Fit Analysis)

If_Surge	Vf	Best Tj	Nom Tj	WC Tj
10	1.56	28.72	29.46	30.20876
20	1.87	33.92	35.70	37.48452
50	3.22	63.37	71.05	78.71973
80	5.54	130.67	151.80	172.9366
81	5.64	133.94	155.73	177.5216
82	5.74	137.30	159.76	182.2248
83	5.85	140.75	163.90	187.0489
84	5.95	144.28	168.14	191.9967
85	6.06	147.91	172.49	197.0712
86	6.17	151.63	176.95	202.2754
87	6.29	155.44	181.52	207.6123
88	6.40	159.35	186.22	213.085
89	6.52	163.35	191.03	218.6967
90	6.64	167.46	195.96	224.4507
95	7.27	189.62	222.55	255.4731
100	7.95	214.70	252.64	290.583

Tj = Power *θ JC + Tambient

*The junction temperature calculation assumes 50% more power as a result of the continued increase in temperature rise that occurs after Vf and If have been measured, which also account for the exponential rise in VF as a function of current and temperature.

Best Tj based on Best Theta_jc = 0.5°C/w @ 8.3mS
Nom Tj based on Nominal Theta_jc = 0.6°C/w @ 8.3mS
WC Tj based on Worst Case Theta_jc = 0.7°C/W @ 8.3mS

- 80 amps half sine @8.3ms recommended for surge test
- Nominal Tj matches test objective and Best / Worst spread OK

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Surge Current Test to Failure

type: APT200SCD65K			lot # A0005776						
one 8.3 ms surge pluse at each value, Ir read after surge.									
equipment: fec pls 1000 (ut 10491) ir done on curve tracer (ut 6418) socket 8070H-002.									
	IR	Surge	IR	Surge	IR	Surge	IR	Surge	IR
	650V	50A	650V	80A	650V	100A	650V	120A	650V
serial #	ua	V	ua	V	ua	V	ua	V	ma
12 leg A	4.00	2.60	4.00	4.16	4.00	6.55	4.00	13.60	>300
12 leg B	2.80	2.60	3.80	4.20	3.80	6.77	3.80	14.25	>300
13 leg A	1.40	2.57	1.60	4.15	2.50	6.51	2.50	13.25	>300
13 leg B	3.80	2.59	3.80	4.19	2.60	6.72	2.60	14.23	>300
14 leg A	2.20	2.56	2.20	4.09	2.30	6.55	2.30	14.00	>300
14 leg B	2.80	2.57	2.80	4.14	2.80	6.72	2.80	14.34	>300

- Data taken in TO254 Package
- ½ Sine wave current pulses
- No degradation in post surge leakage up to 100 amp level
- Damage / failure high probability @ 120 amp level

Qualitative Evidence from Burn-in

Device Name	NSD305										
Lot Name	A00040278										
Comment	PRE HTRB										
Test		4	5	6	7	8	9	10	11		
Item		ICBO	BVCBO	VFBC	ICBO	IR	BVR	VF	IR		
Limit		200.0uA	652.0 V	1.800 V	200.0uA	200.0uA	652.0 V	1.800 V	200.0uA		
Limit Min Max		<	>	<	<	<	>	<	<		
Bias 1		VCB 522 V	IC 250 uA	IB 20.0 A	VCB 520 V	VAK 522 V	IC 250 uA	IAK 20.0 A	VAK 520 V		
Bias 2			VMAX 999 V				VMAX 999 V				
Time		2.500ms	2.500ms	380.0us	2.500ms	2.500ms	2.500ms	380.0us	2.500ms		
Wafer Data	No										
Serial	Bin										
16	1	293.0n	971.4	1.577	292.0n	1.196u	830.8	1.572	1.206u		No Surge (Eng Lot)
17	1	1.010u	9.990k	1.587	835.5n	1.142u	945.2	1.58	1.071u		No Surge (Eng Lot)
18	1	1.162u	9.990k	1.578	1.028u	5.355u	936.4	1.588	5.638u		No Surge (Eng Lot)
19	1	235.1n	9.990k	1.571	230.0n	203.5n	976.2	1.565	192.6n		No Surge (Eng Lot)
20	1	2.642u	9.990k	1.563	2.559u	244.0n	9.990k	1.57	232.0n		No Surge (Eng Lot)
21	1	230.0n	9.990k	1.584	219.2n	549.0n	920.5	1.593	523.0n		Post 10x 100A Surge (Eng Lot)
22	1	2.140u	784.2	1.571	2.115u	444.5n	942.6	1.562	432.1n		Post 10x 100A Surge (Eng Lot)
23	1	179.3n	9.990k	1.566	177.5n	118.3n	9.990k	1.567	23.55n		Post 10x 100A Surge (Eng Lot)
25	1	4.815u	9.990k	1.549	5.061u	5.451u	9.990k	1.547	5.399u		Post 10X 120A Surge (Production Lot)
29	1	3.829u	9.990k	1.567	3.624u	8.596u	936.6	1.556	8.501u		Post 10X 120A Surge (Production Lot)
33	1	998.0n	9.990k	1.572	1.063u	8.194u	9.990k	1.569	7.673u		Post 10X 120A Surge (Production Lot)
34	1	4.813u	9.990k	1.548	4.949u	2.217u	9.990k	1.547	2.059u		Post 10X 120A Surge (Production Lot)

Device Name	NSD305										
Lot Name	A00040278										
Comment	POST HTRB										
Test		4	5	6	7	8	9	10	11		
Item		ICBO	BVCBO	VFBC	ICBO	IR	BVR	VF	IR		
Limit		200.0uA	652.0 V	1.800 V	200.0uA	200.0uA	652.0 V	1.800 V	200.0uA		
Limit Min Max		<	>	<	<	<	>	<	<		
Bias 1		VCB 522 V	IC 250 uA	IB 20.0 A	VCB 520 V	VAK 522 V	IC 250 uA	IAK 20.0 A	VAK 520 V		
Bias 2			VMAX 999 V				VMAX 999 V				
Time		2.500ms	2.500ms	380.0us	2.500ms	2.500ms	2.500ms	380.0us	2.500ms		
Wafer Data	No										
Serial	Bin										
16	1	323.0n	971	1.581	311.2n	1.409u	808.8	1.577	1.455u		No Surge (Eng Lot)
17	1	518.8n	9.990k	1.59	471.2n	652.3n	939.5	1.585	652.1n		No Surge (Eng Lot)
18	1	1.446u	9.990k	1.579	1.095u	2.646u	947.6	1.589	3.206u		No Surge (Eng Lot)
19	1	225.3n	9.990k	1.57	225.5n	204.0n	973.3	1.564	194.5n		No Surge (Eng Lot)
20	1	1.119u	9.990k	1.564	1.123u	232.7n	9.990k	1.571	229.2n		No Surge (Eng Lot)
21	1	208.0n	9.990k	1.577	198.2n	476.0n	900.9	1.585	465.1n		Post 10x 100A Surge (Eng Lot)
22	1	2.363u	765.1	1.572	2.368u	396.3n	943.8	1.563	395.0n		Post 10x 100A Surge (Eng Lot)
23	1	194.6n	9.990k	1.566	186.5n	138.9n	9.990k	1.569	136.0n		Post 10x 100A Surge (Eng Lot)
25	1	1.488u	9.990k	1.549	1.485u	4.479u	9.990k	1.548	4.429u		Post 10X 120A Surge (Production Lot)
29	1	1.353u	9.990k	1.561	1.314u	8.309u	939.9	1.553	8.270u		Post 10X 120A Surge (Production Lot)
33	1	304.1n	9.990k	1.569	279.1n	3.079u	9.990k	1.568	2.302u		Post 10X 120A Surge (Production Lot)
34	1	1.311u	9.990k	1.546	1.287u	625.5n	9.990k	1.546	615.5n		Post 10X 120A Surge (Production Lot)

Pre Burn In

Engineering and production surge test survivors were subjected to HTRB Burn in. All samples passed.

Post Burn In

Screening Requirements on the SiC Diode

- Screening Requirements

Inspection/Test 1/	MIL-STD-750	
	Method	**Conditions**
Initial Electrical Measurements	4011	V_{F1} at 25°C, I_F = 20A (pk) pulsed, V_{F1} = 1.8V max
	4016	I_{RM} at 25°C, DC Method V_R = 520V, I_{RM} = 200uA max
	4021	V_{BR} at 25°C, I_R = 200uA, V_{BR} = 650V min
	4001	C_T at 25°C, V_R = 0Vdc, f = 1MHz, Vsig = 50mV(p-p),C_T = 2000pF max
Temperature Cycling	1051	20 cycles: -55°C to +175°C
Surge Current	4066	Condition A: 10 surges, 1 per/min, 7mS min., 80A
Constant Acceleration	2006	20,000 g's Y1 direction, 10,000 g's for Power rating > 10 Watts. 1 min, Hold time not required
PIND	2052	Condition A
Mid Electrical Measurements	4011	V_{F1} at 25°C, I_F = 20A (pk) pulsed, V_{F1} = 1.8V max
	4016	I_{RM} at 25°C, DC Method V_R = 520V, I_{RM} = 200uA max
	4021	V_{BR} at 25°C, I_R = 200uA, V_{BR} = 650V min
	4001	C_T at 25°C, V_R = 0Vdc, f = 1MHz, Vsig = 50mV(p-p),C_T = 2000pF max
Burn-In	1038	Condition A, V_R =520V, T_J>150°C, Duration 160 hrs
Final Electrical Measurements	4011	V_{F1} at 25°C, I_F = 20A (pk) pulsed, V_{F1} = 1.8V max V_{F2} at 175°C, I_F = 20A (pk) pulsed, V_{F1} = 2.5V max
	4016	I_{RM} at 25°C, DC Method V_R = 520V, I_{RM} = 200uA max
	4021	V_{BR} at 25°C, I_R = 200uA, V_{BR} = 650V min
	4001	C_T at 25°C, V_R = 0Vdc, f = 1MHz, Vsig = 50mV(p-p),C_T = 2000pF max
	3101 or 4081	ThetaJX, See MIL-PRF-19500
Delta Calculations	4011	ΔV_{F1} at 25°C, I_F = 10A (pk) pulsed, +/- 100mV from initial value
	4016	I_{RM} at 25°C, DC Method V_R = 520V, ΔI_{RM} = +/- 100% of Initial Value
Hermetic Seal: Fine Gross	1071	 G2 B & D
Radiographic	2076	

1/ Requirements are in accordance with EEE-INST-002

Radiation Evaluation

Single Event Effects Radiation Testing at Texas A&M K500 Cyclotron Facility

Dates of Activity: April 28 & 29, 2014

Date of Report: Monday, May 12, 2014

1.1.1 Beam Condition 1: LET 41.4 MeVcm²/mg, range 21.6 um, Kr ion

Beam_energy (MeV/amu)	Beam_energy (MeV)	Nominal_LET (MeVcm2/mg)	Nominal_range (um)	Selected fluence (ions/cm2)	Typical Dose (rad)	Typical Aver._flux (ions/(cm2s))
1.8	151	41.4	21.6	2.9E+5	1.9E+2	4.93E+4

1.1.2 Beam Condition 2: LET 20.2 MeVcm²/mg, range 125.5 um, Cu ion

Beam_energy (MeV/amu)	Beam_energy (MeV)	Nominal_LET (MeVcm2/mg)	Nominal_range (um)	Selected fluence (ions/cm2)	Typical Dose (rad)	Typical Aver._flux (ions/(cm2s))
11.7	738	20.2	125.5	9.9E+5	3.2E+2	1.14E+4

- One Sample tested to 260Vr under Kr beam
- Three samples tested to 250Vr under Cu beam
- All samples passed without evidence of breakdown
- Test equipment limited to 300Vr.

Summary and Conclusion for SiC Diodes

- SiC diodes can greatly enhance efficiency and reliability of high power space DC-DC converters
- SiC diodes require a deep derating of Vrr to reliably withstand SEE.
  - 650V diode was derated to 250V in this case (38% of rated)
  - Derating ratio does not necessarily apply to other Vrr ratings
- We are early in characterizing SiC diodes for Space but the potential benefits certainly indicate a priority to proceed
- Surge current screening of SiC diodes should carefully account for the positive Vf characteristic and dynamic heating of the SiC die during the pulse
  - This effect is much less important in Si Diodes
- Overall a great example of Microsemi's ability to solve serious technical issues in real time by drawing on vertical resources across divisions

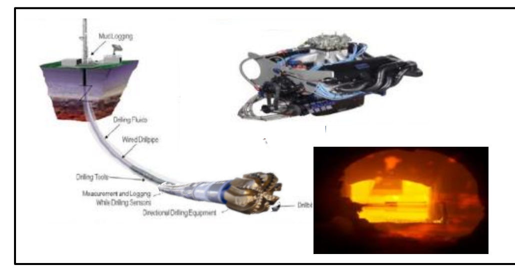
The Roadmap for Microsemi SPM

- More SMT??!
- Intelligent Power
- Higher System Integration
- Complementary developments in Aviation

AEROSPACE

SPACE

MILITARY & DEFENSE



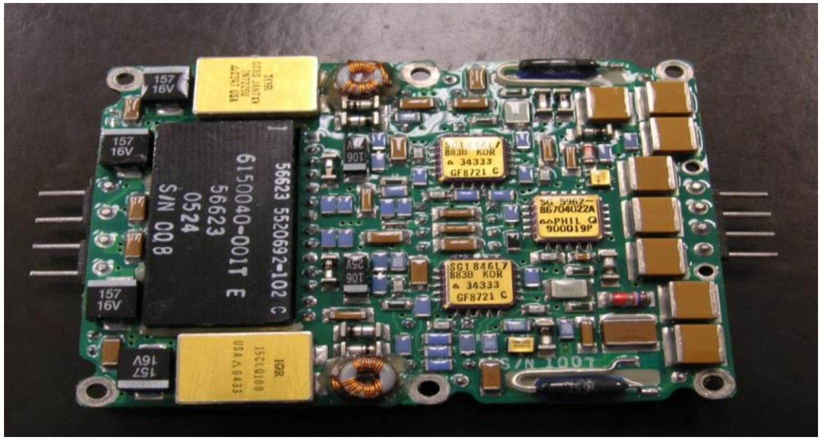
EXTREME ENVIRONMENT

PWA Surface Mount vs. Hybrid Technology

- PWA Standard Modules are constructed with Heritage SMT processes

	SMT	HYBRID
Assembly Process	Automated	Manual
Device Attachment	Solder	Eutectic / Epoxy
Connections	Solder	Wire Bond
Components	Package pre-screened	Basic Die

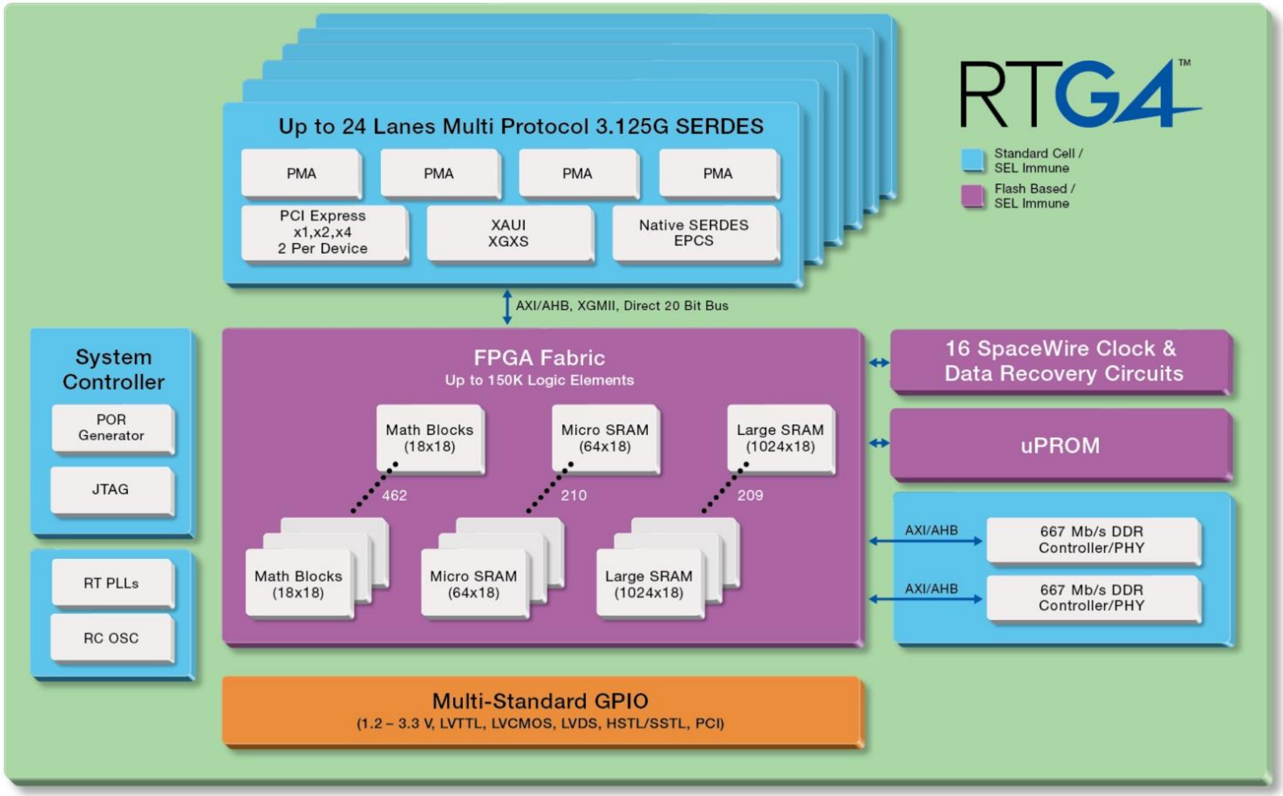
SMT Process Yields High Product Consistency and Quality



Following the launch of our highly successful SA50 DC-DC Converter product line, we see a rising demand to replace Hybrid DC- DC Converters with the SMT alternative.

- Faster lead times
- Ability to customize and add value
- Lower risk of LOT Qualification issues with disastrous reach back

Intelligent Power - RTG4



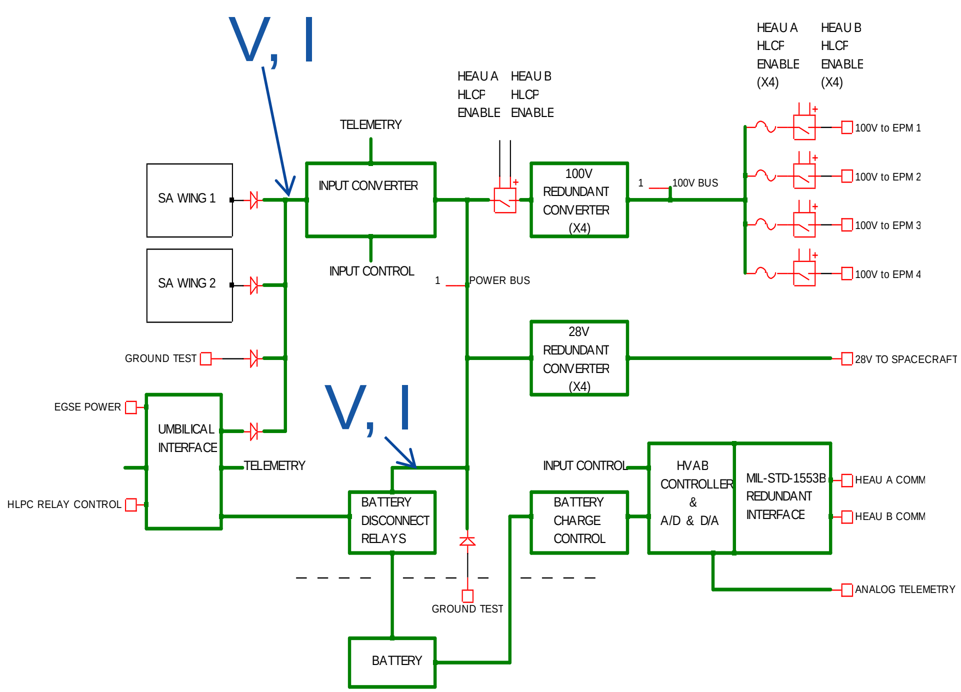
- Total-dose hardening of Flash cells
- Single-event hardening of registers, SRAM, multipliers, PLLs

Comprehensive radiation-mitigated architecture for signal processing applications

Radiation Tolerant Power Supplies

- Microsemi provides many Radiation-Tolerant components that can be used to supply power to RTG4 FPGAs
- Engineers should consider the following when selecting power supply components
  - Calculate required power of the RTG4 device
    - PowerCalc spreadsheet, SmartPower tool in Libero design software
  - Select an appropriate Radiation-Tolerant regulator that can supply the required power and meet all power requirements of RTG4
    - Radiation-Tolerant Linear-Regulator (Microsemi)
    - Radiation-Tolerant Switching regulator (Microsemi)

Solar Array Conversion – PDU Concept



REGULATION STATES

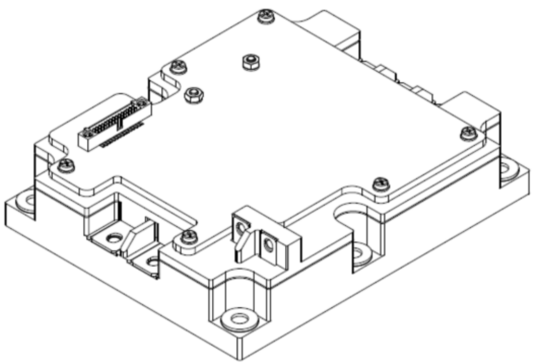
CONSTANT BATTERY CURRENT
CONSTANT BATTERY VOLTAGE
PEAK ARRAY POWER

- RTG4 FPGA manages full Solar Array conversion controls
  - Generates PWM Drives
- Data Acquisition
  - SA Voltage & Current
  - Battery Voltage & Current
- Battery at End Of Charge Voltage
  - SA Converter regulates Constant Voltage
- Battery Charging
  - SA available power > load
  - SA Converter regulates constant current
  - Current level driven to match commanded battery charge current
- Peak Power Mode
  - SA available power < load
  - SA Converter reflected input voltage adjusted to maximum power point

Aviation – A Complementary Sector

POWER CORE MODULE **MAICMMC40X120A**

SiC based flight critical actuation motor drive



- Leading the way for future space applications
  - Serial Bus Control
  - Embedded FPGA Controller
  - 2 year SiC proof of life program
  - SEE radiation requirement

Features

- SiC MOSFET and SiC Schottky diode for power conversion
  - Low $R_{DS(on)}$ for MOSFET
  - Zero Reverse Recovery for SiC SBD
  - High Power Efficiency
- Integrated Gate drive circuitry with isolation and shoot through detection
- 5kVA / 25Amp drive capability
- Integrated control card with embedded FPGA for H-bridge control
- High speed LVDS communication bus for data exchange
- Internal three phase current sense, DC bus voltage sense circuitry and temperature monitoring
- AlSiC base plate for extended reliability and reduced weight
- Si3N4 substrate for improved thermal performance
- Direct mounting to Heatsink (Isolated Package)
- Custom Variants are available. Please contact factory

Thank You

Microsemi Corporation (MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,600 employees globally. Learn more at www.microsemi.com.

Power Matters.™

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