Power Matters.™

Space System Managers Architecture and Performance

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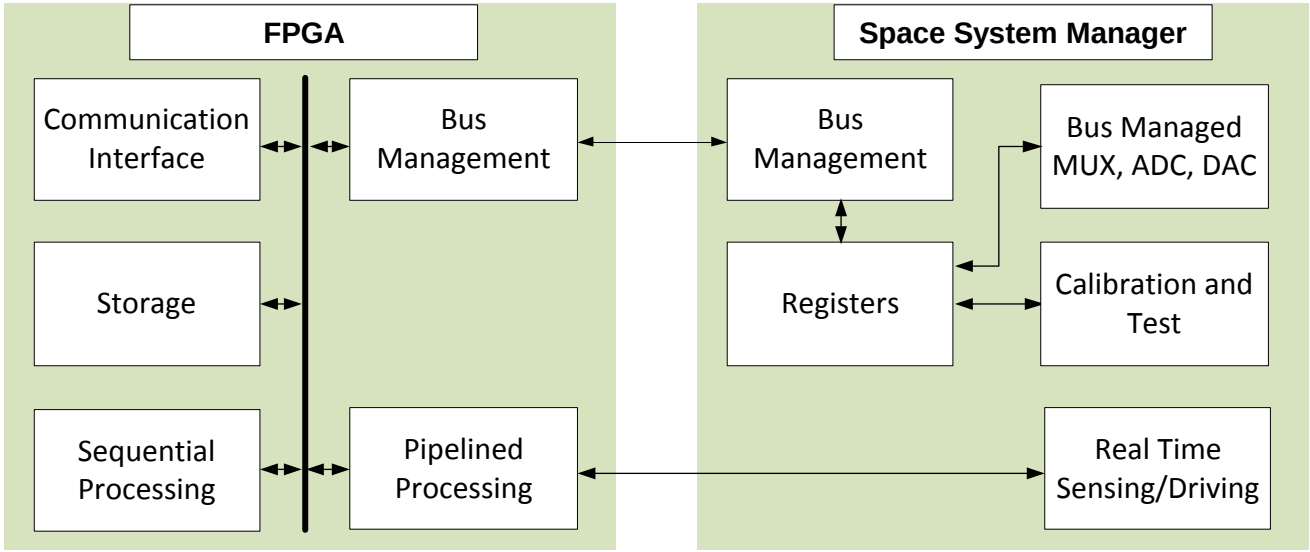
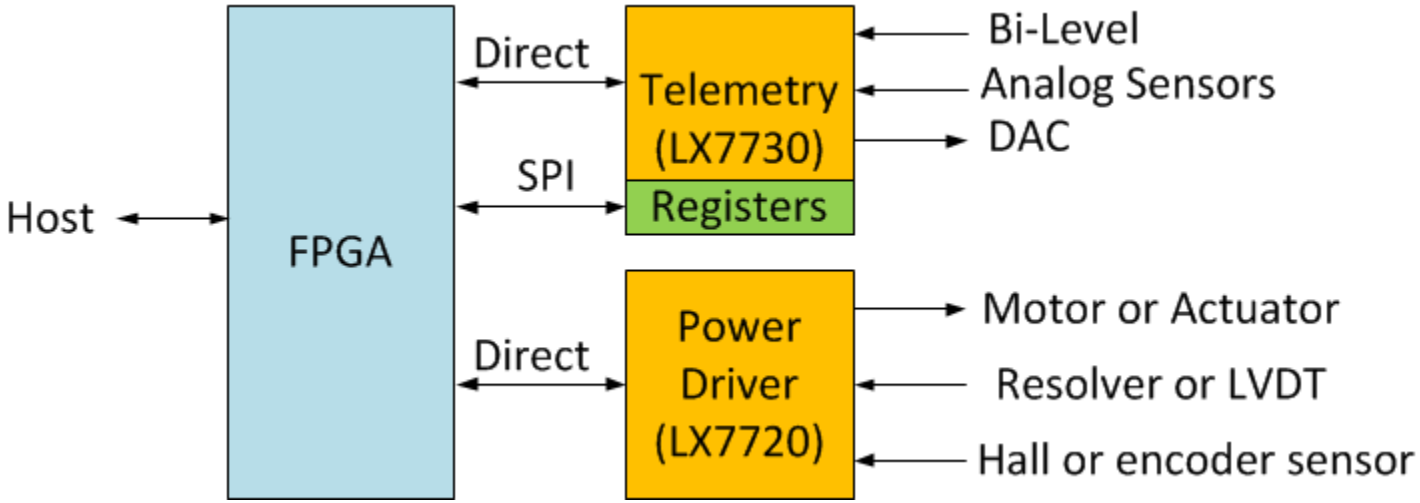
Space System Manager Concept

- Space System Manager (SSM) is a special purpose analog or power IC
- The SSM IC is intended to work with an FPGA:
  - I/O levels and timing are compatible.
  - The SSM has a minimal amount of hard coded internal logic.



Space System Manager Characteristics

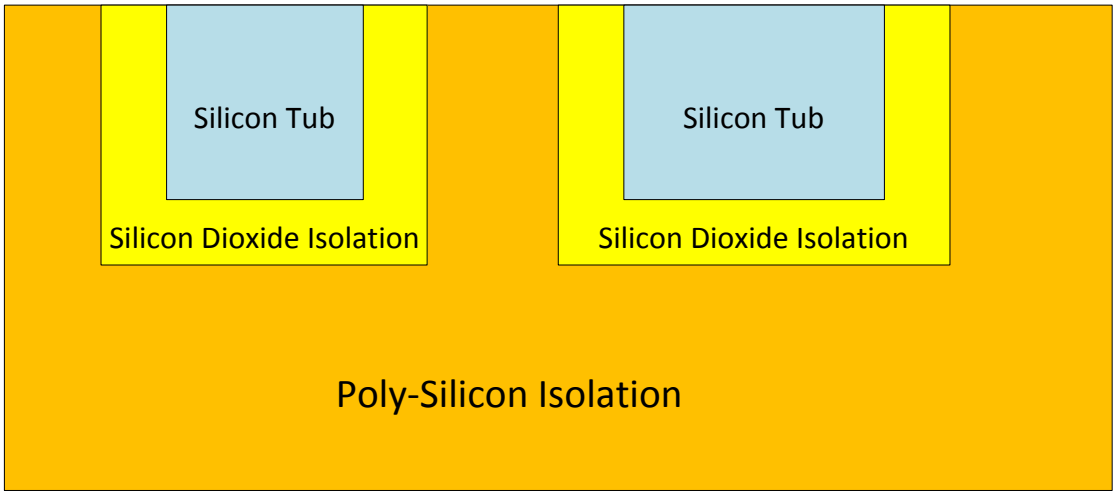
- Both the Space System Manager and the FPGA are standard parts that are space qualified and DLA listed.
- The SSM standard attributes are:
  - Radiation Tolerant: 100krad TID; 50krad ELDRS, SE tolerant
  - Inputs are cold spared and dielectrically isolated
  - ESD and overvoltage clamping



IC Process for Fault Isolation

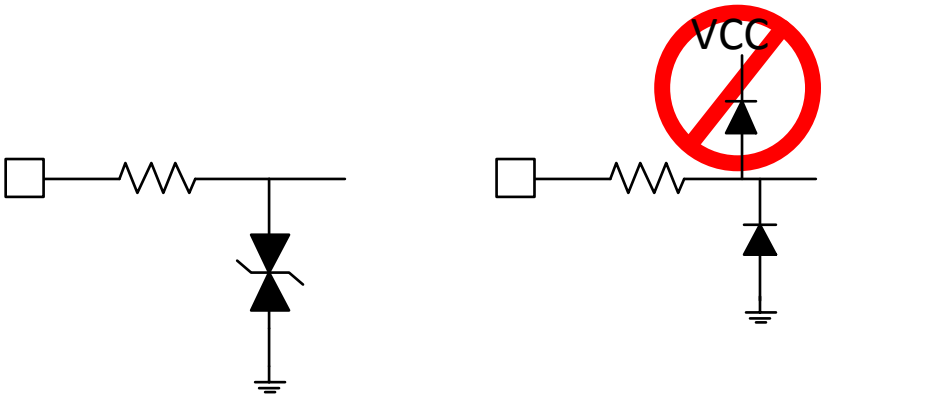
- The SSM uses a special Dielectric Isolated (DI) process such that if any channel within the IC becomes compromised due to an external fault, the remaining IC continues to function normally.
  - There is not a common substrate connection that you find with other IC processes.
  - This process is similar in performance to the isolation achieved in hybrid circuits.
  - Isolation between tubs is at least 350V.

Dielectric Isolation
Cross Section



IC Process for Cold Sparing

- An isolated ESD structure for each SSM pin along with design techniques considering low leakage with power removed allows the SSM to be cold spared (becomes a high impedance with the power removed).

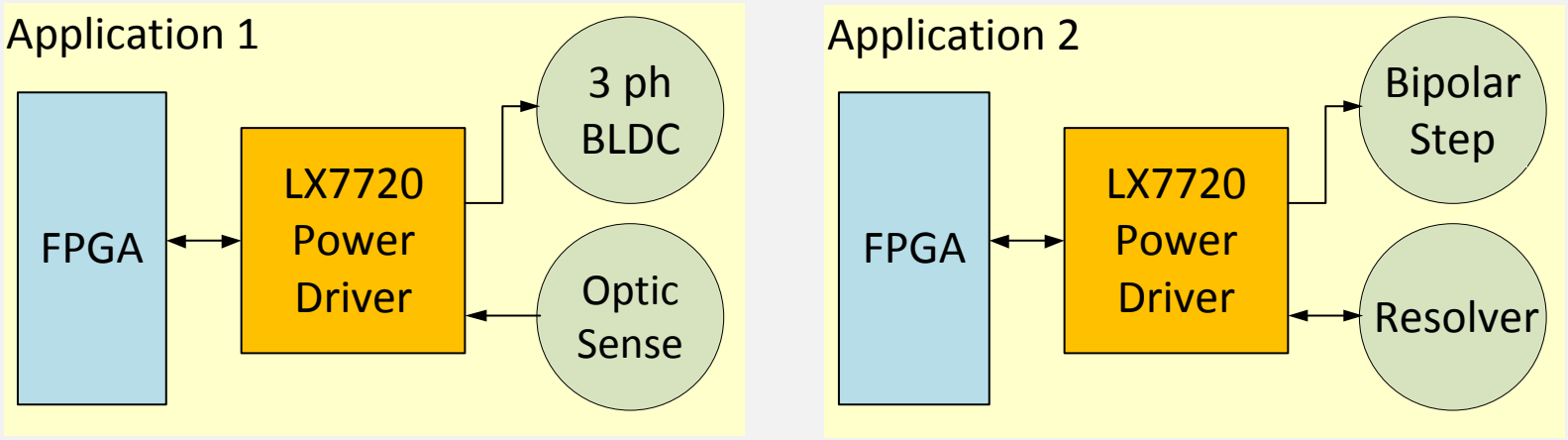


Cold Sparing Typical ESD Protection

SSM Application Versatility

- SSMs take advantage of commonality between applications.
  - Servo motor drivers require high power switches and position sensing.
  - Telemetry monitoring requires an analog MUX, ADC and bi-level inputs.

Different applications using the same IC part numbers.



System Manager System Integration

- FPGA HDL module examples are:
  - Spacecraft communication bus
  - Motor micro-stepping
  - Brushless DC servo loop
  - Resolver to digital conversion
  - Sigma Delta filtering and decimation
- SSM registers examples:
  - Programmable current source
  - ADC input range setting
  - MUX selection of inputs
- External Components adjust:
  - External NMOS power sizing for motor drivers
  - Bi-level threshold levels

HDL Modules

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Register Map

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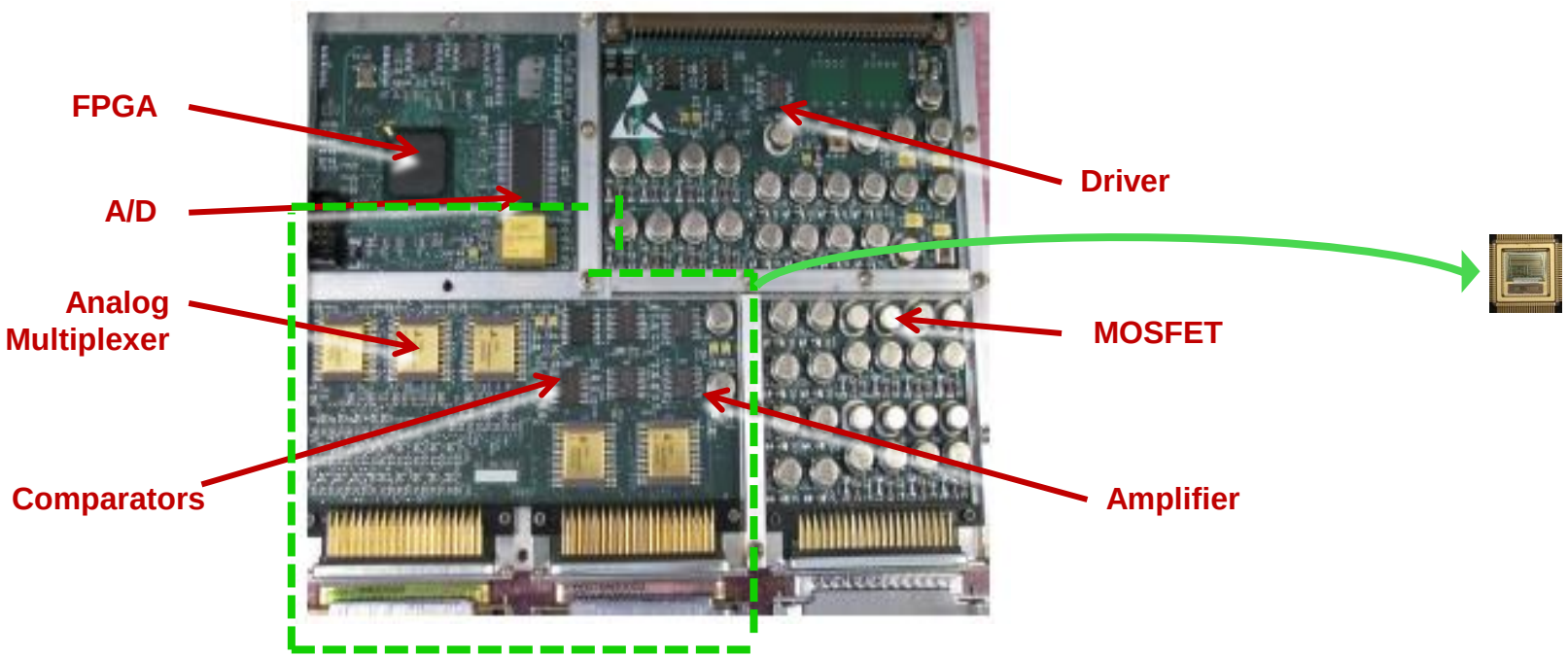
Power Sizing & Programming Components

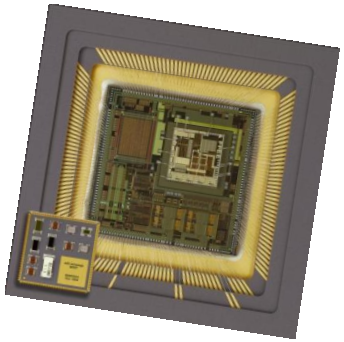
Space System Manager vs. Discrete Components



- A typical circuit uses an FPGA with analog interface functions implemented with many single function ICs and discrete components.
- SSM integrates commonly used functions into one package to reduce circuit board area and weight.
- Although utilization may not be 100% for the space system manger, it is still likely to be a more compact solution.

Space System Manager vs. Custom IC

- The custom rad-hard mixed-signal solution provides an efficient solution but presents a number of challenges:
  - Development cost for a Mixed-Signal custom for space applications is typically $1M-$2M
  - Development time typically of 1-2 year.
  - Qualification is typically 6 months to 1 year.
  - Time to production 2-3 years.



- Unlike the SSM, with a custom ASIC:
  - Very few players are able to budget such development.
  - The solution typically has minimal flexibility if requirements change.

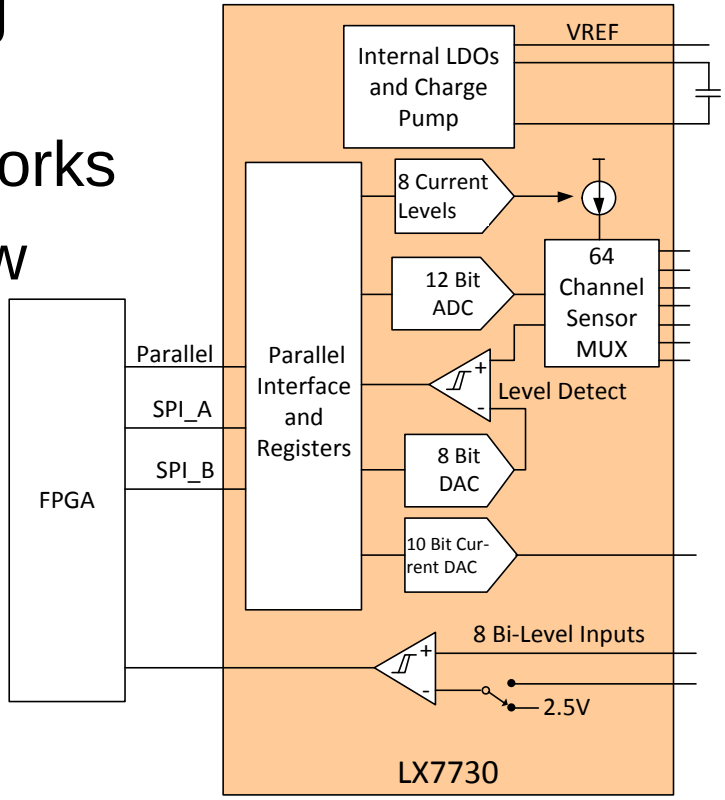
Reducing Risk While Maximizing Integration

	Discrete Solution	Space System Manager	Custom ASIC Solution
NRE	Low	Low	High
Development Time	Months	Months	Years
Qualification	Fast	Fast	Long
Risk	Small	Small	Moderate
Flexibility	High	High	Low
Power	Worst	Good	Best
Reliability	Average	Excellent	Excellent
Size and Weight	Poor	Good	Best

The LX7730
Radiation Tolerant Telemetry Controller

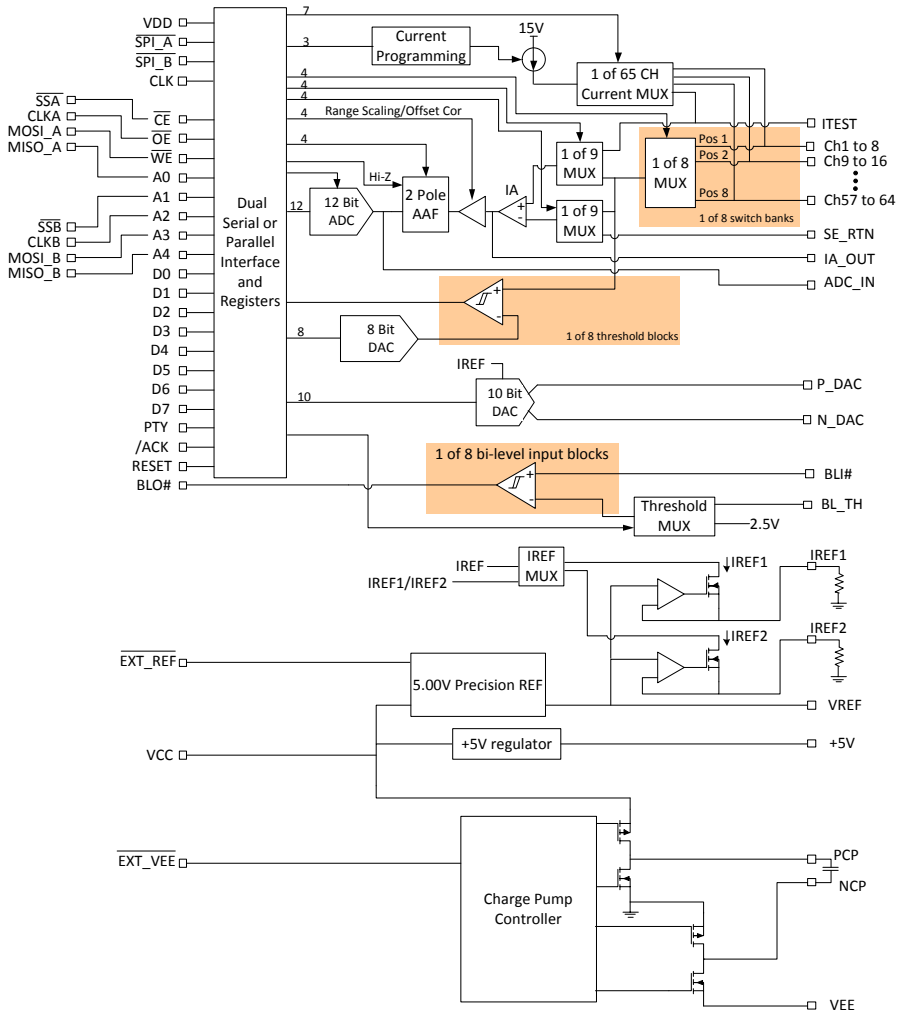
LX7730: 64 Analog Input Telemetry Controller

- Single ended sensing for 64 sensors with simultaneous monitoring of 8 sensors
- Differential (Kelvin) sensing of 32 sensors
- Current demux to any input for driving passive sensors
- Voltage reference to bias bridge networks
- ADC ranging accurately measures low level voltage changes
- DAC out for level control
- 8 bi-level logic translators



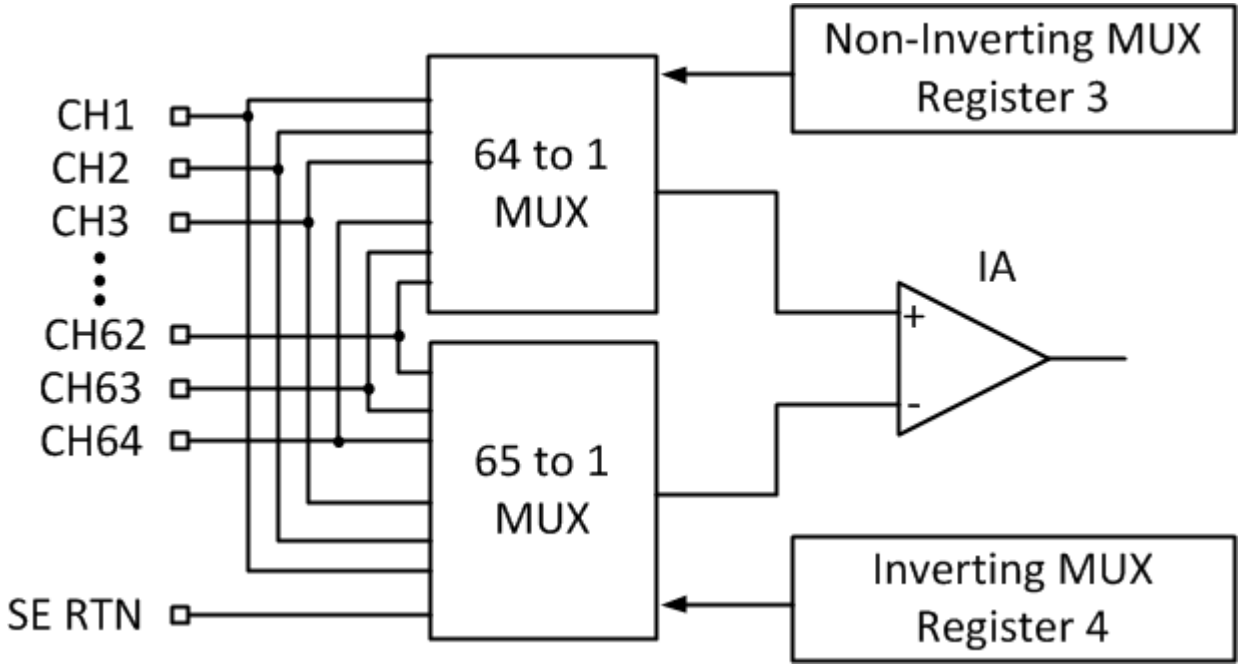
LX7730 Block Diagram

- 64 universal General Purpose sensor interfaces:
  - *64 single ended or 32 differential*
  - *ADC range pre-scaling*
  - *64 channel current source demux*
  - *Level monitoring of 8 SE channels*
  - *Break-before-make switching MUX*
- 25ksps 12 bit ADC
- Optional 2 pole anti-aliasing filter
- 8 fixed bi-level logic interfaces
  - *Internal or external threshold setting*
- 10 bit current DAC
  - *Complementary outputs*
- 1% precision reference
- 2% current references
- Parallel or Dual SPI interface
- Built in test and calibration
- +15 VCC input to internal regulators



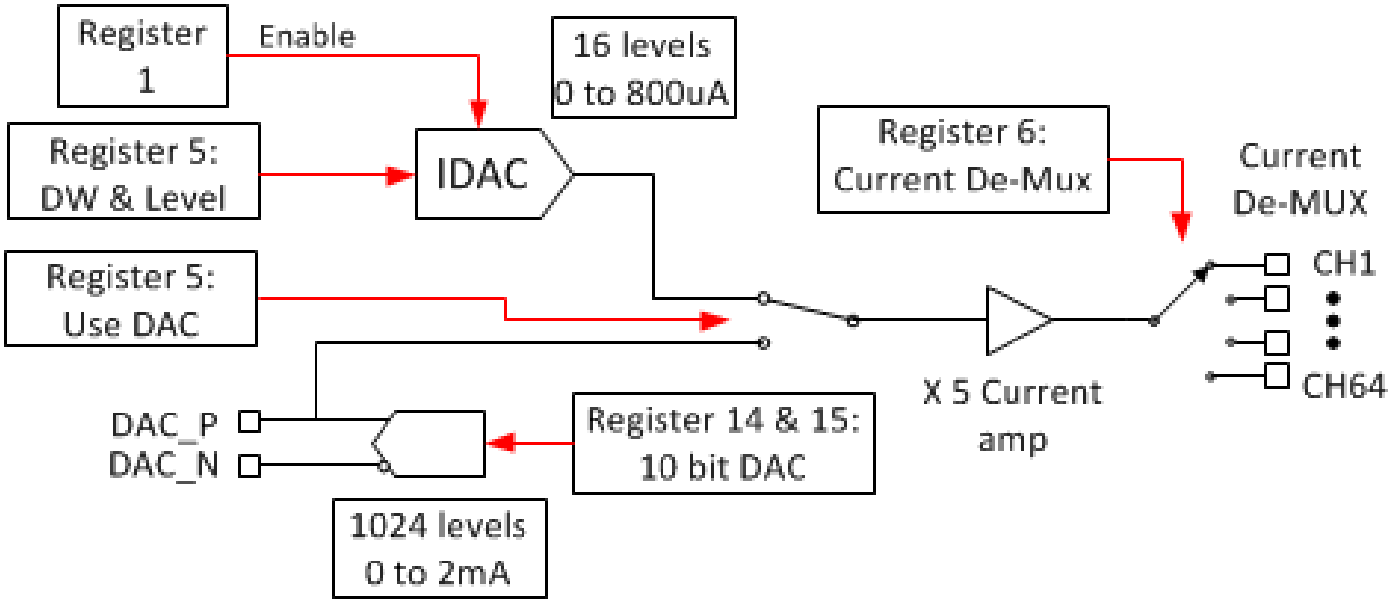
Voltage Acquisition

- LX7730 has 64 voltage acquisition input channels
- The instrumentation amplifier converts differential inputs to ground referenced. Common mode range is -5V to 5V
- Two analog multiplexers route one channel to the IA non-inverting terminal and another channel to the common single ended reference (SE RTN) for the inverting terminal



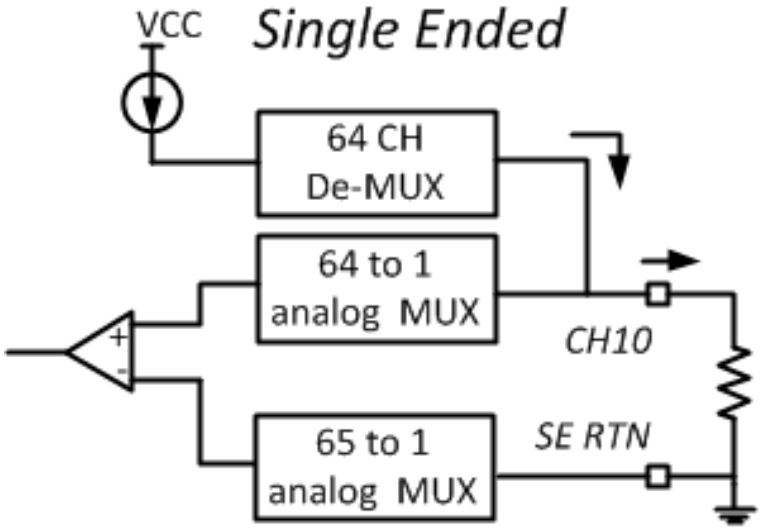
Current Source and De-MUX

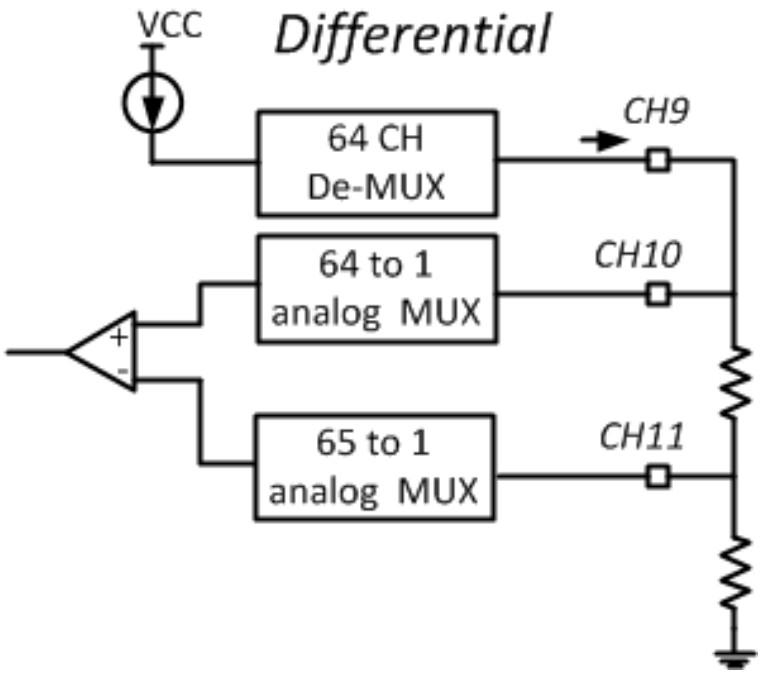
- Current source can be routed to any one of the 64 CH# pins
- The current source can be set from 250uA to 4mA in 250uA increments using the current source programming register
- Or the current source can be set using the 10 bit DAC to a resolution of 10uA starting at 0
- Wide compliance range: -15V to 10V



Measuring resistive sensors

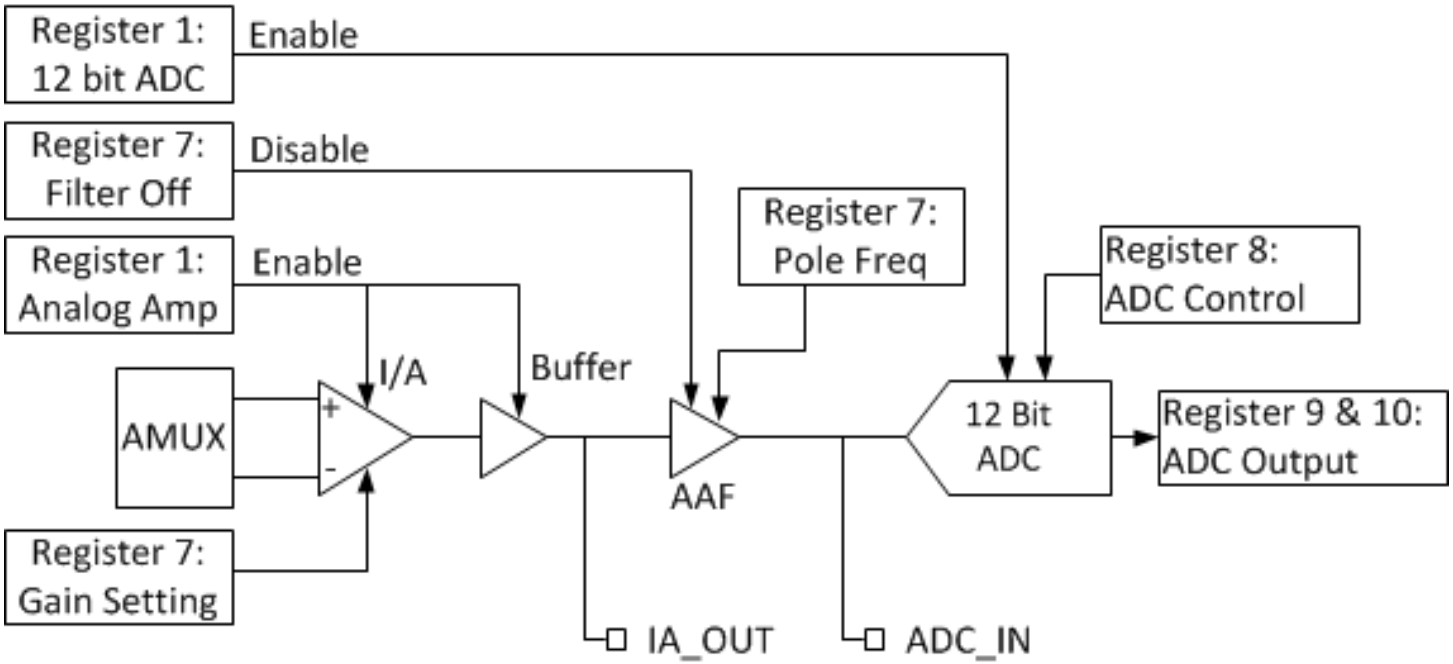
- The current source and de-MUX can be used with the analog MUX and IA to make resistance measurements
- Single ended measurements will service the most channels
- Differential measurements reduce stray resistance affects





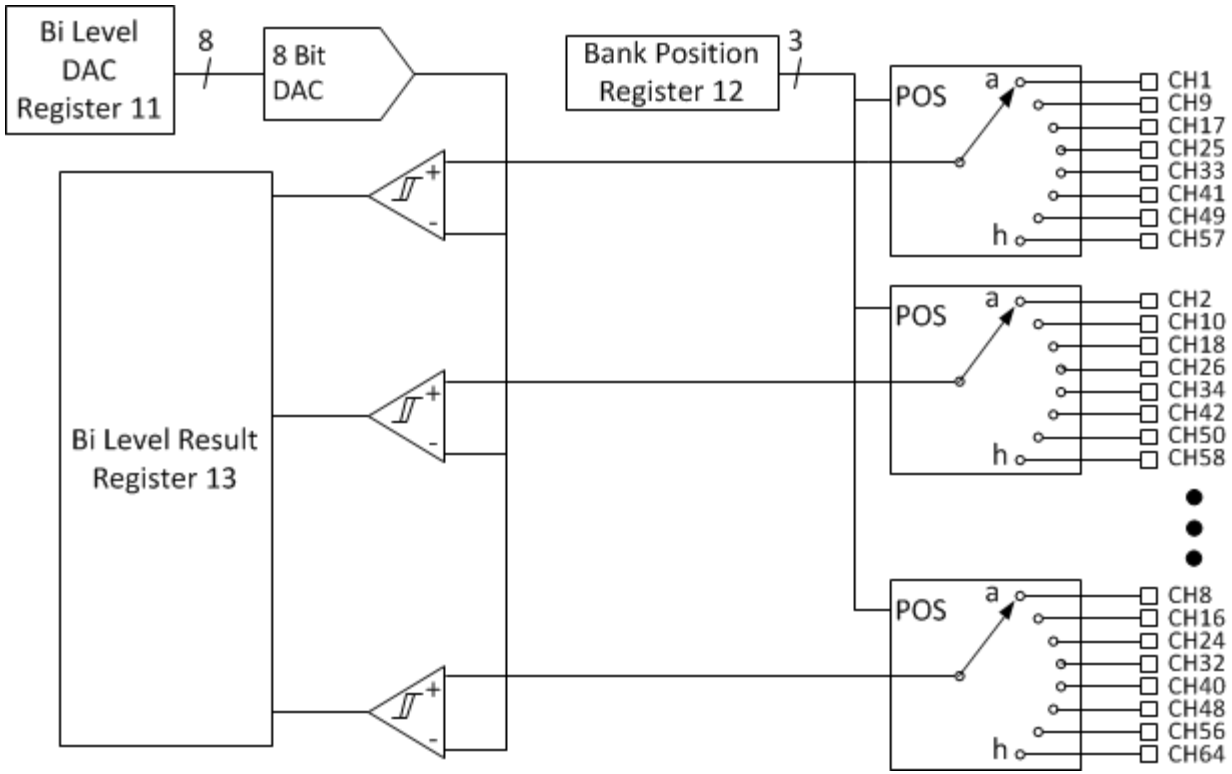
12 bit ADC

- The ADC has a dynamic range of 0 to 2V
- The IA pre-scaler sets channel range to 5V, 1V or 200mV
- The two poles of the anti-aliasing filter (AAF) can be set to 400Hz, 2kHz or 10kHz or infinity



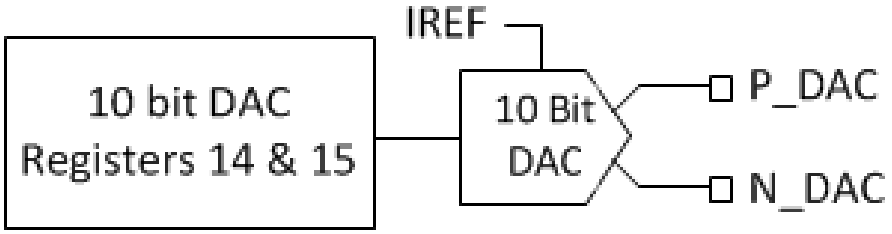
Bi-Level Bank Comparator Mode

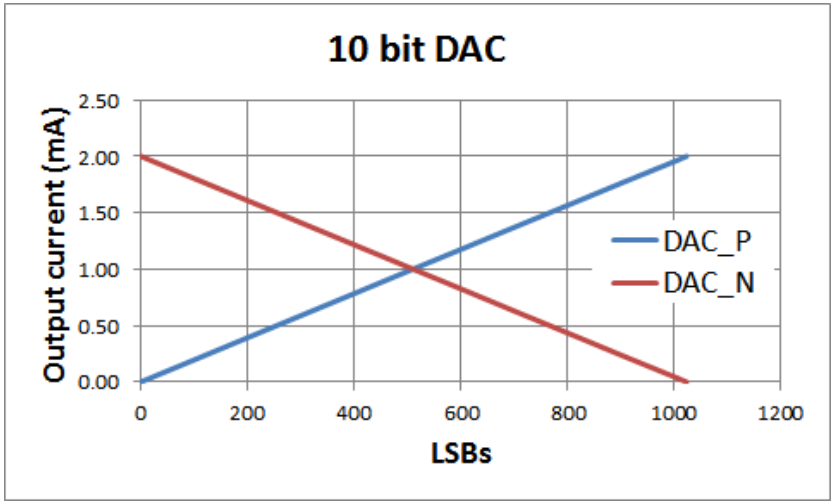
- Simultaneous voltage checks for 8 single ended channels
- Common threshold is controlled by an 8 bit DAC
- Comparator outputs are a readable register location
- Note: 64 to 1 channel AMUX is not usable in this mode



10 bit Current DAC

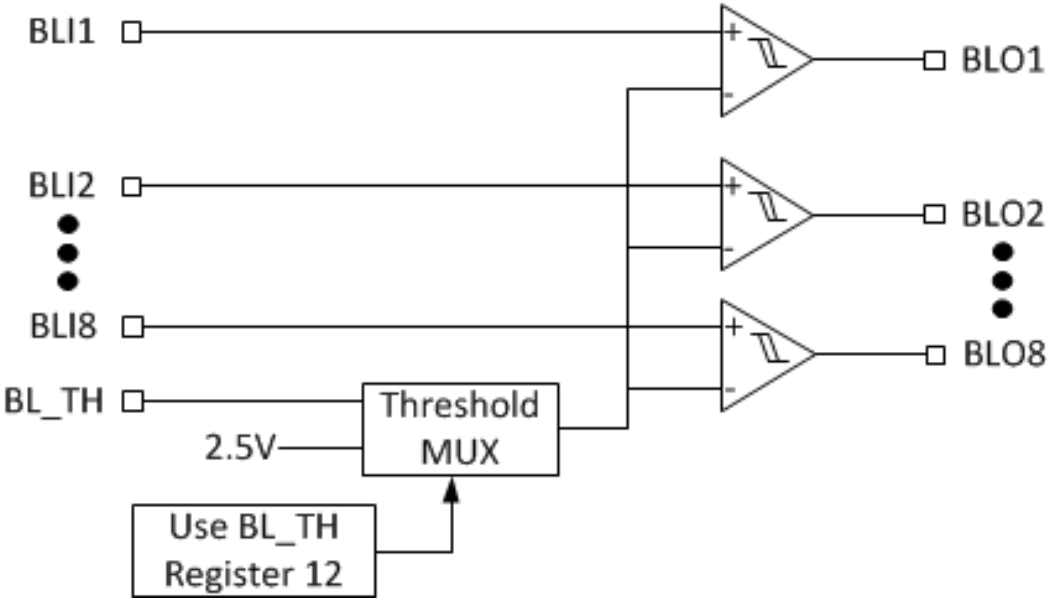
- The 10 bit current DAC is register controlled
- It has a 0 to 2mA range and a compliance from 0V to 3V
- Note: The 10 bit DAC should not be used as a DAC if it is simultaneously being used to control the current source





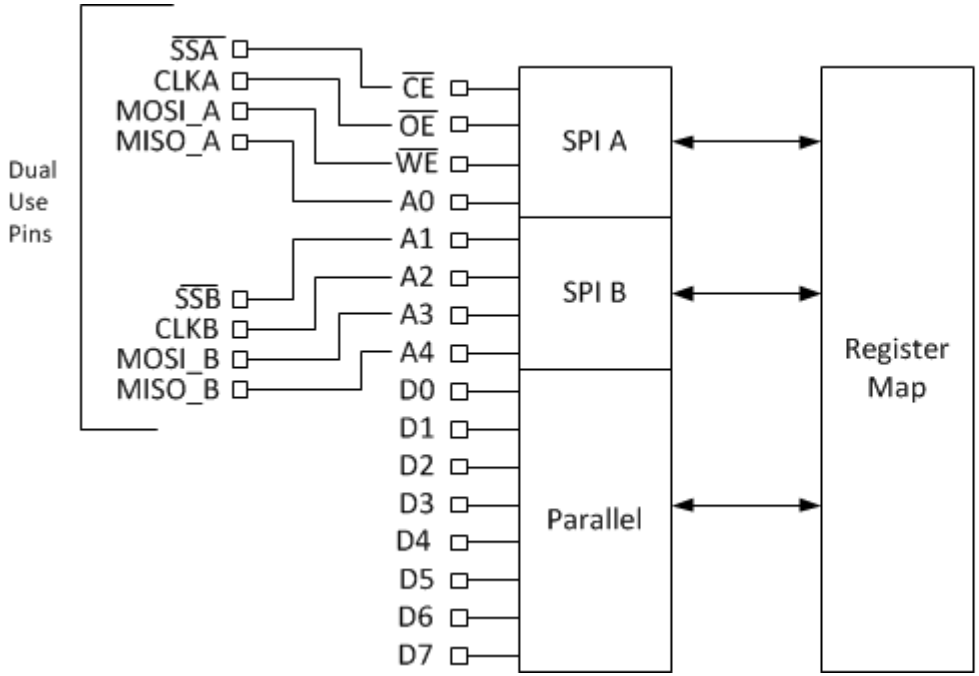
8 Pass Through Bi-level Logic Translators

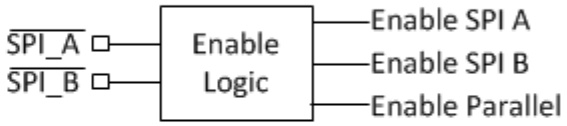
- Logic translators have input and output pin outs
- Threshold either internal 2.5V or pin programmable
- Hysteresis for noise immunity on slow ramping inputs



Digital interface

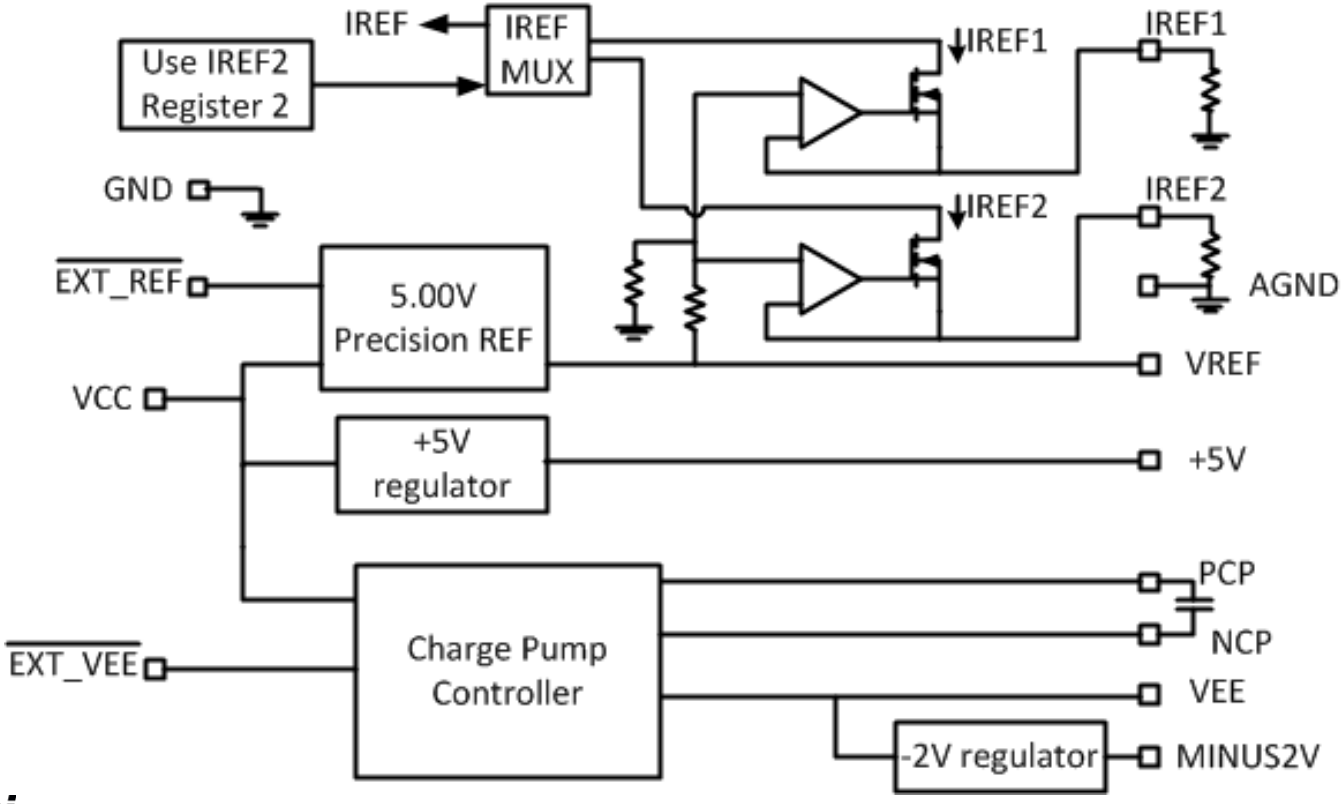
- Digital interface can be SPI_A or SPI_B or parallel
- Only one interface is active at a time
- Registers are 8 bits in length
- SPI pins are dual use for parallel interface
- VDD logic supply also powers FPGA I/O





Power supplies

- Requires a VCC (12V or 15V) and VDD for logic (2.5V to 5V)
- Charge pump for negative rail (VEE) or disable if not used
- 1% reference with option to use external 5V reference
- Redundant IREF avoids single point failure

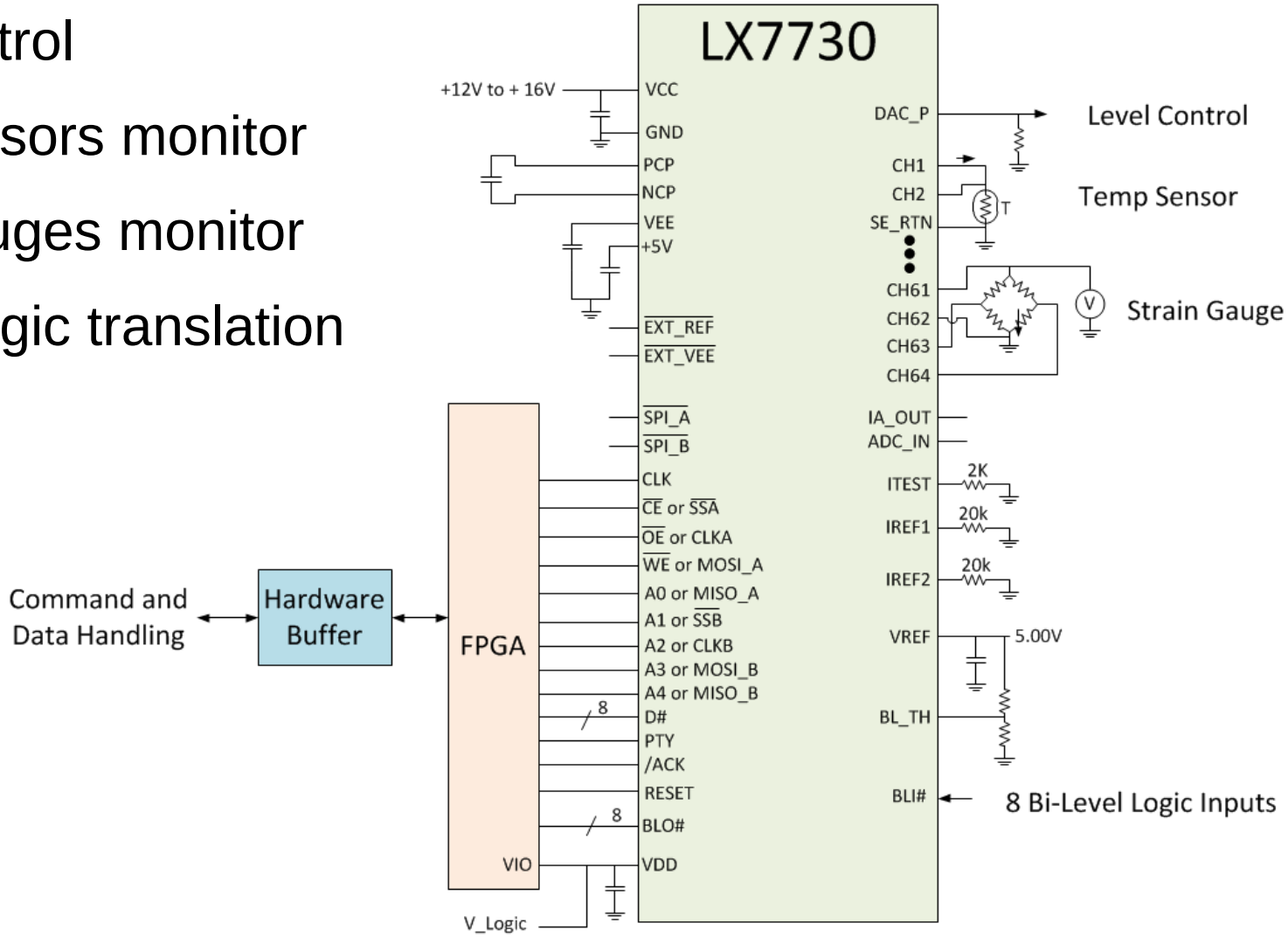


Key Features

- 1kV ESD protection on CH pins, 2kV on all other pins
- +/- 20V clamps on CH# pins and +/-15 for BLI# pins
- Cold sparing on CH# pins and BLI# pins
- Redundant IREF
- Redundant SPI interface

LX7730: Application Figure

- Level control
- Temp sensors monitor
- Strain gauges monitor
- Bi-level logic translation

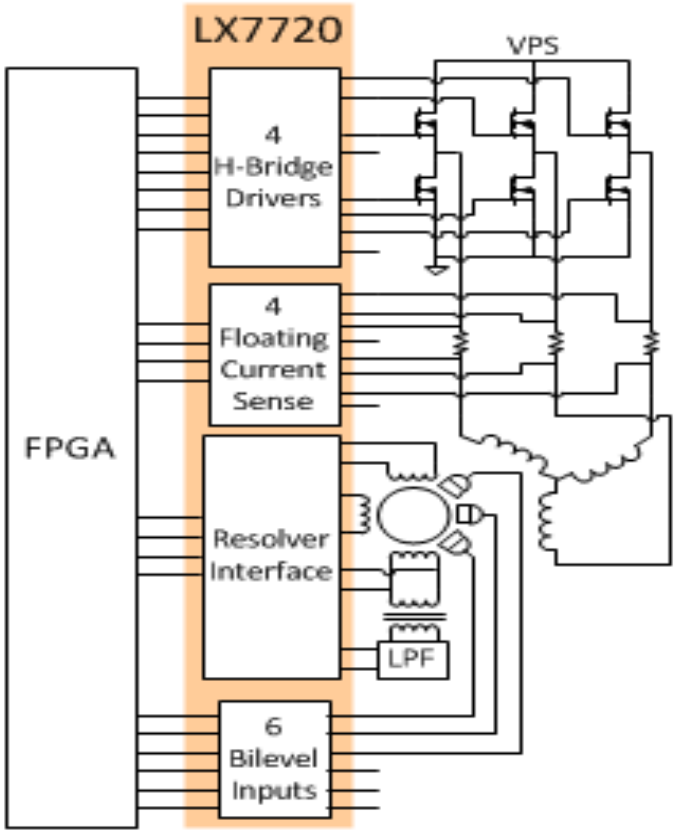


LX7730 Performance Highlights

Parameter	Comment	Min	Typ	Max	Units
SE or Diff sensor input		0		5	V
Differential Sensor common mode		-5		5	V
ADC conversion rate			25		kHz
ADC resolution			12		bits
Reference voltage	Internal V_{REF}	4.95	5.00	5.05	V
MUX settling time			1.5		µs
MUX leakage current	Power on or off	-100		100	nA
Bi-level threshold range		0.5		4.6	V
Bi-level propagation delay			1		µs
DAC compliance range		0		3.0	V
DAC full scale current	Sourcing	1.94	2.00	2.06	mA

LX7720 Power Driver w Position Feedback

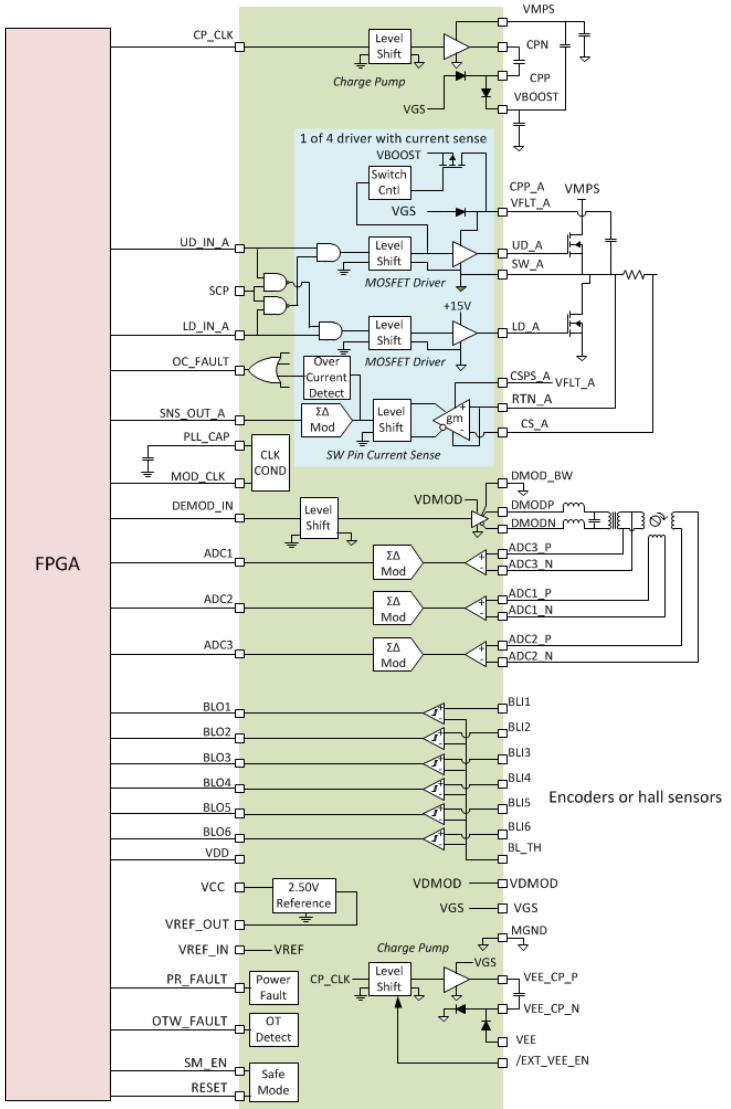
- Provides MOSFET motor drivers for
  - 3 phase motors
  - Unipolar or bipolar steppers
  - Individually controlled switches
- Up to 4 current sensors
  - In-line (floating)
  - High side or ground referenced
- Sensing for resolver or LVDT
- Detecting pulse sensors and limit switches



LX7720 Block Diagram

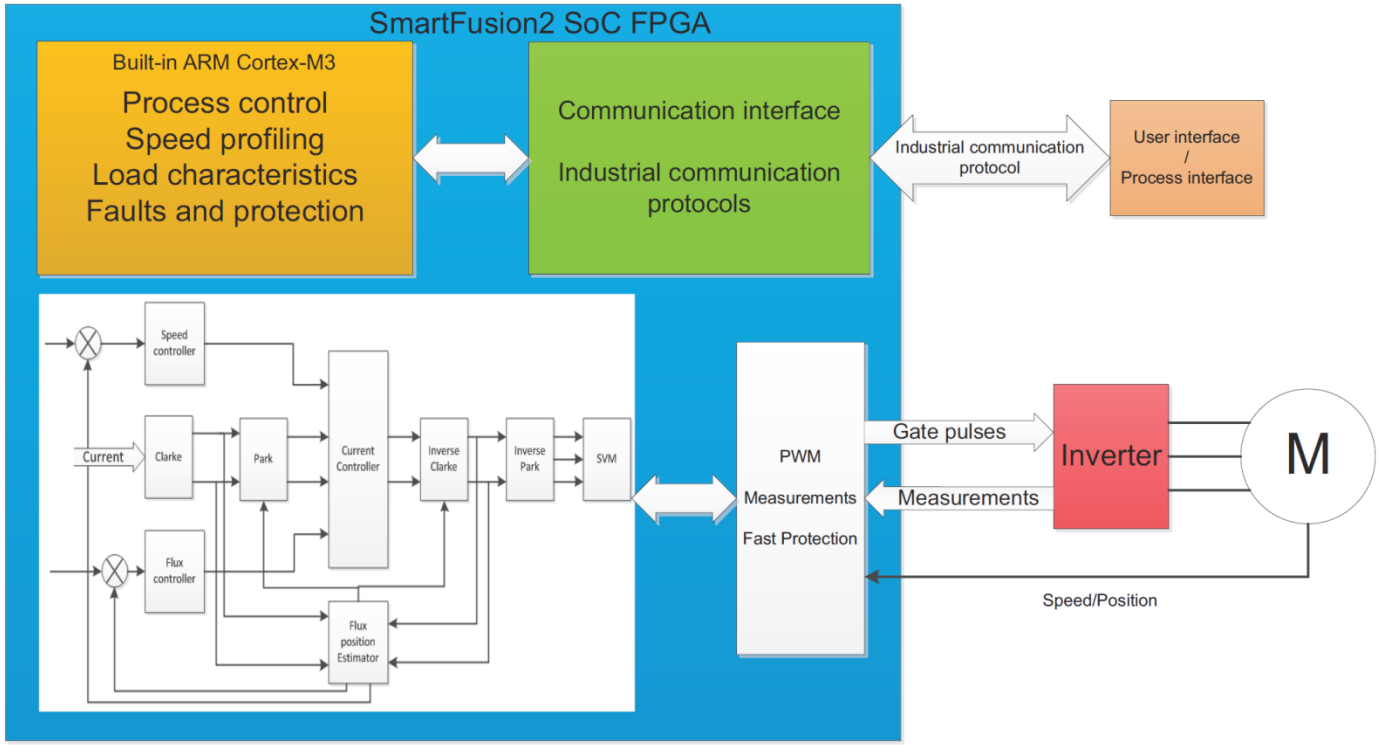
Features:

- Four Half-Bridge N-channel MOSFET drivers
- Four floating differential current sensors with ΣΔ modulated processed outputs to FPGA
- Pulse density modulated resolver exciter
- Three differential resolver sensors with ΣΔ modulated processed outputs to FPGA
- Six bi-level logic inputs
- 5V GND isolation signal-to-motor



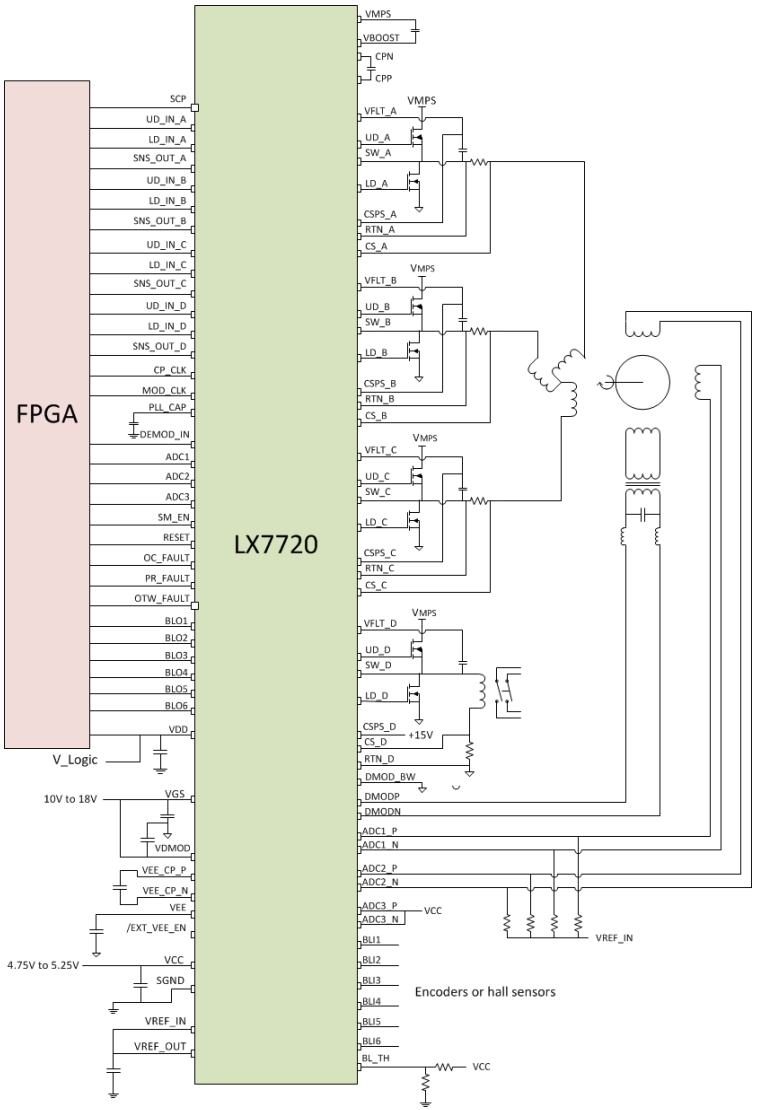
LX7720 is a companion to the RTG4 FPGA

- Fabric based motor control algorithm developed for RTG4 and LX7720
- Demonstration dual axis code available using SF2-MC-StarterKit
- Resolver to digital position feedback option



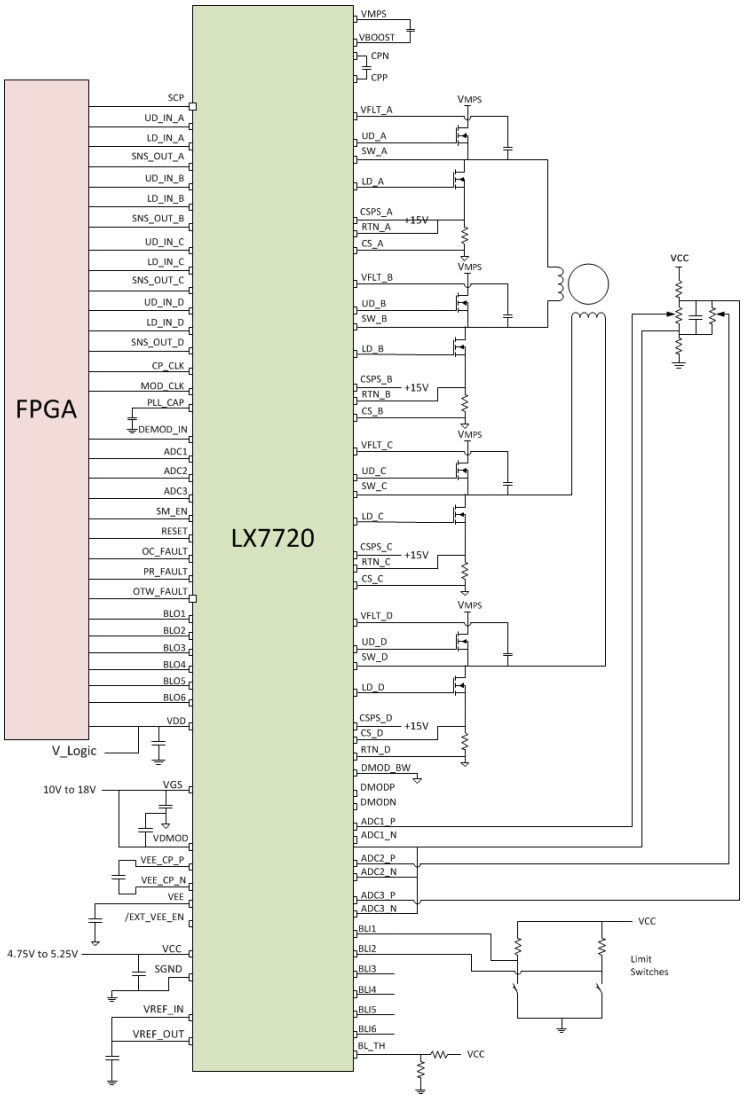
LX7720 PMSM Application

- Three phase PMSM motor
- Tracking resolver
- In line current sensing
- Phase D used for relay driver with current sense in return path.



LX7720 Bipolar Microstepper

- Bipolar stepper motor
- Return path current sensing
- Potentiometer position sensing
- Limit switch sensing



LX7720 Performance Highlights

Parameter	Comment	Min	Typ	Max	Units
Motor Power Supply	De-rated by 20%	20	48	150	V
MOSFET driver impedance	Source or sink		1		Ω
PWM frequency		DC		200	kHz
Current sense range		-250		250	mV
Current sense accuracy			7		bits
Current sense latency			4		µS
Resolver carrier frequency		0.36		20	kHz
Resolver accuracy			16		bits
Bi-level threshold range		0.5		4.6	V
Bi-level propagation delay			1		µs

Space System Manager Advantages

- Provides a high level of integration (smaller size and weight)
- Is a standard part so there is minimal design risk or qualification risk
- No development NRE
- Designed to work with an FPGA so the flexibility is designed-in
- Designed for space applications so additional buffers and level shifting are not necessary
- Radiation tolerance of TID > 100kRad; ELDRS > 50KRad; SEL tolerant
- Cold spared
- Fault tolerant

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