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RTG4 Software Features

Microsemi Space Forum 2015

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Microsemi
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Agenda

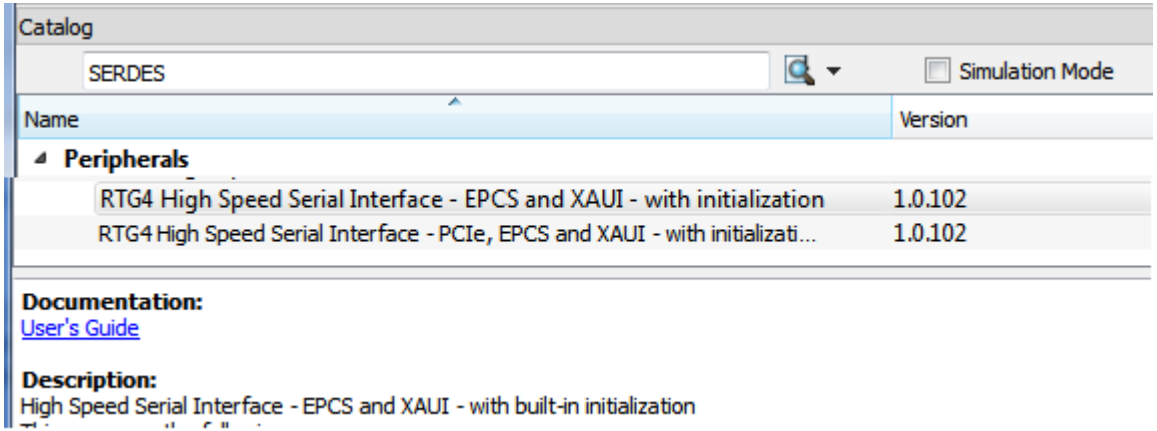
- Design Considerations
- Design Software Options
- System Controller Suspend Mode
- SPI Slave Programming
- Programming Options
- Package Pins Changes
- Conclusion

Design Considerations – RAM EDAC

- RAM blocks have built in EDAC (SECDED)
  - SECDED is single error correct, double error detect
  - Optional at word widths 18 bits and higher. Not available at smaller word widths
  - Scrubbing is not built in to the RAM EDAC. Use Microsemi IP (CoreEDAC) or build your own in fabric
- EDAC has flags that shows single correction has happened or double detection has happened
- Software provides GUI Configurators for the LSRAM and uSRAM blocks
- To access the built in EDAC features, use the RAM Configurator instead of RAM inference through Synthesis
- If EDAC is not needed, RAM inference is supported and available with Synplify synthesis tools

Design Considerations - SERDES

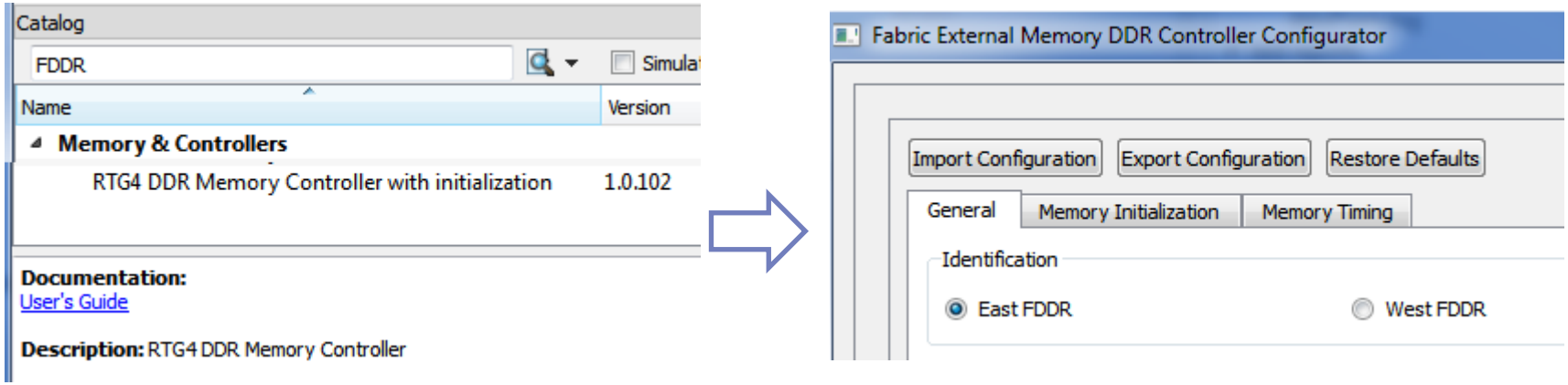
- SERDES Configurator and automatic configuration initialization
- Two type of SERDES blocks
  - Support for PCIe, EPCS, and XAUI
  - Support for EPCS, XAUI (no PCIe support)
- Configurators in Catalog reflect the different SERDES blocks types



- SERDES configurator has built-in automatic initialization mechanism
  - Initialization is generated automatically based on the user selected configuration

Design Considerations - FDDR

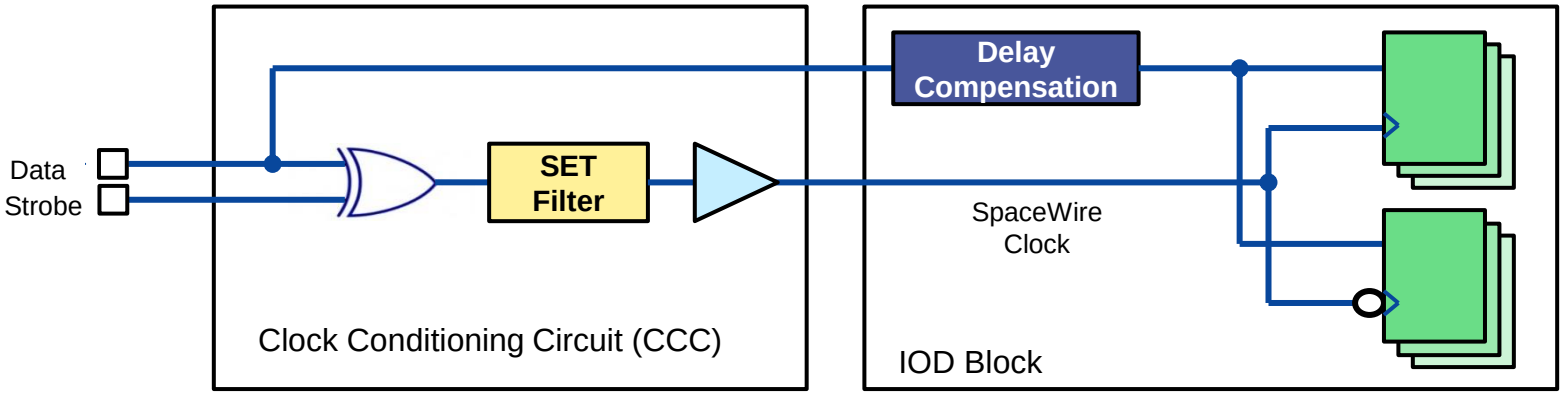
- FDDR Configurator and automatic configuration initialization
- Two FDDR blocks (East FDDR and West FDDR)
- FDDR configurator accessed from Catalog and location selection is made in the Configurator GUI



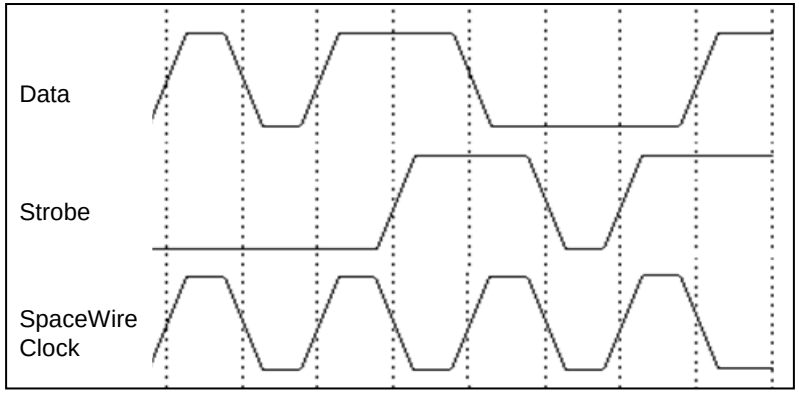
- FDDR configurator has built-in automatic initialization mechanism
  - Initialization is generated automatically based on the user selected configuration

Design Considerations - SpaceWire

- CCC/PLL Configurator and hardened SpaceWire RX Clock/Data Recovery

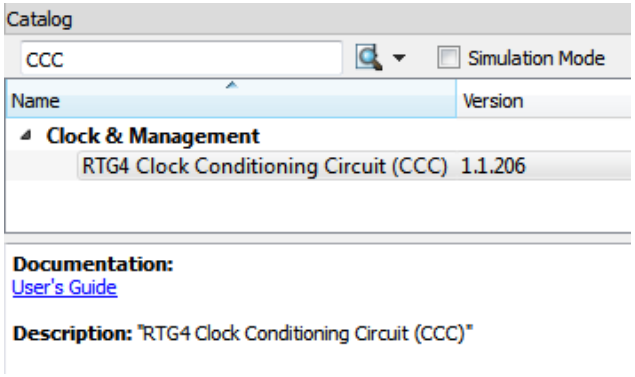


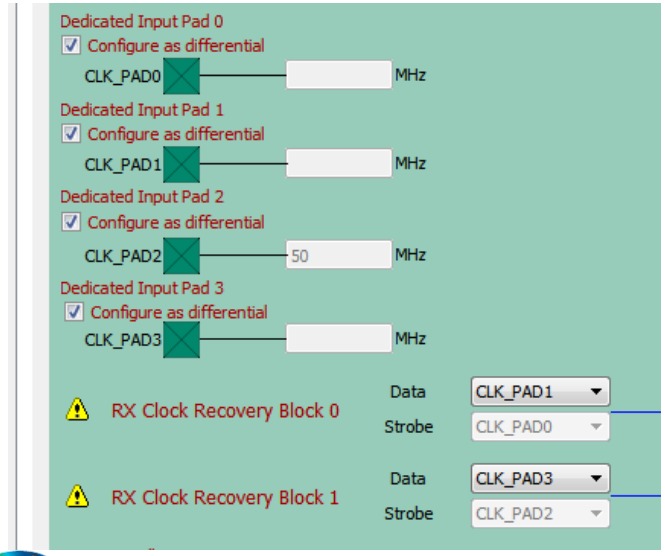
- Each CCC has a built in SpaceWire Clock/Data Recovery circuit
- SpaceWire interface used for command-and-control and data
  - Data and Strobe are XORed to recover SpaceWire clock
  - Hardwired and SET protected
  - Delay compensation option is available in IO block to align data and SpaceWire clock
  - 16 SpaceWire Clock/Data Recovery circuits on each RTG4

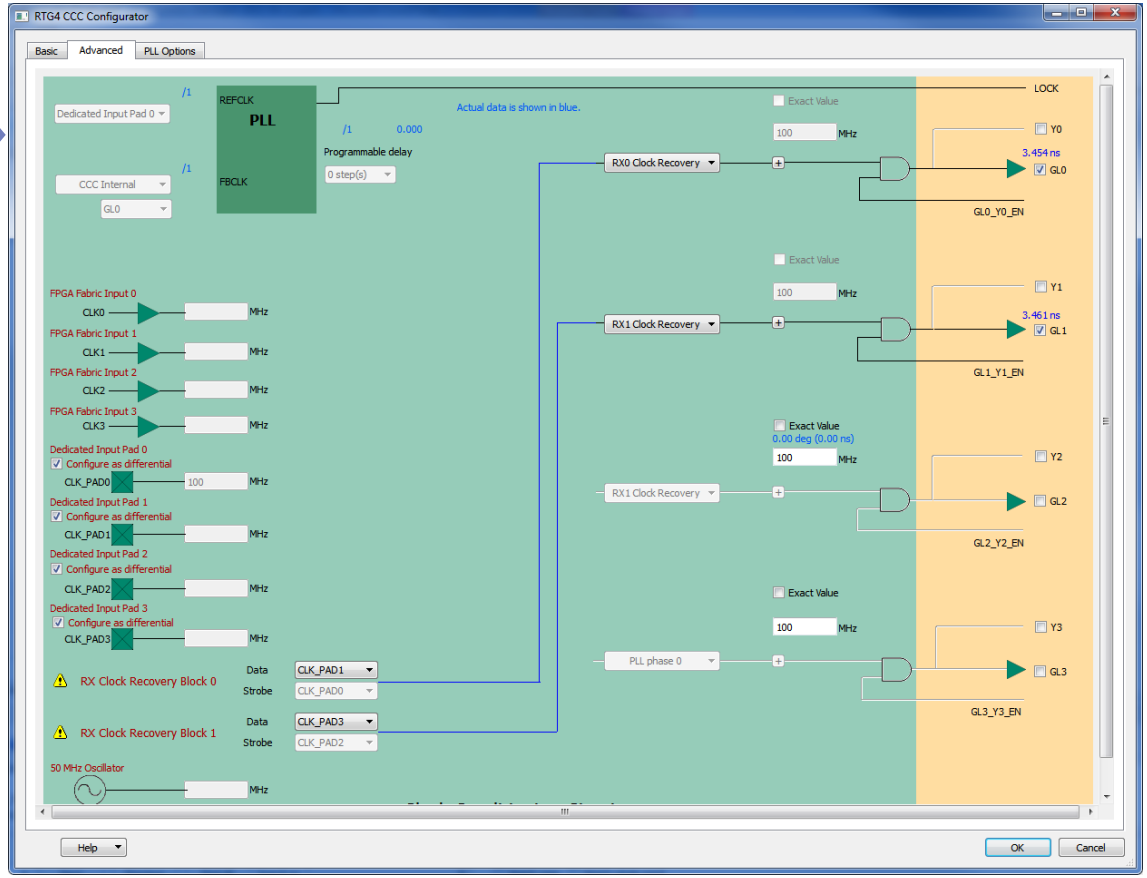


Design Considerations - CCC

- CCC/PLL configurator accessed from Catalog
- SpaceWire options are part of the CCC Configurator



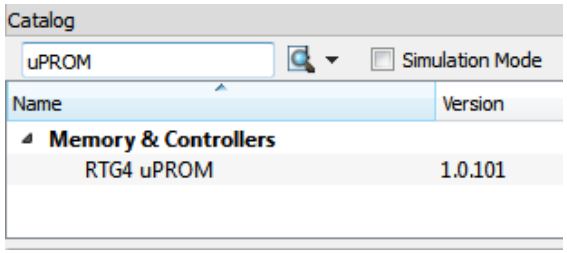


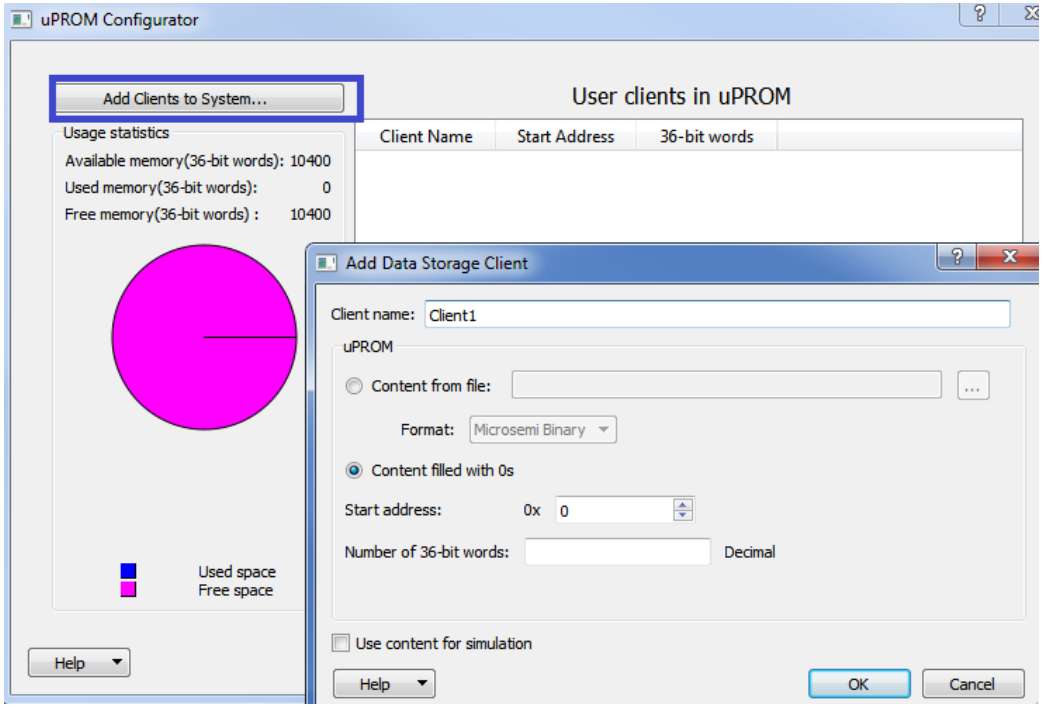


Design Considerations - uPROM

- The RTG4 FPGA fabric has one embedded programmable read only memory (uPROM) block (10,400 36-bit words)
  - Used for storing program data such as initialization data for LSRAM and uSRAM blocks

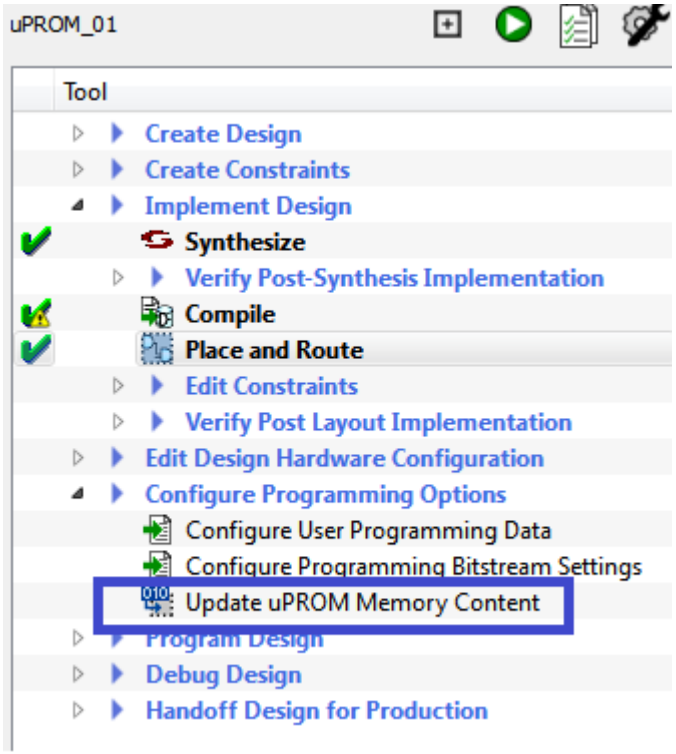
- uPROM Configurator and design flow
  - uPROM configurator accessed from Catalog
  - Create clients based on:
    - Address
    - Number of words
    - Memory file





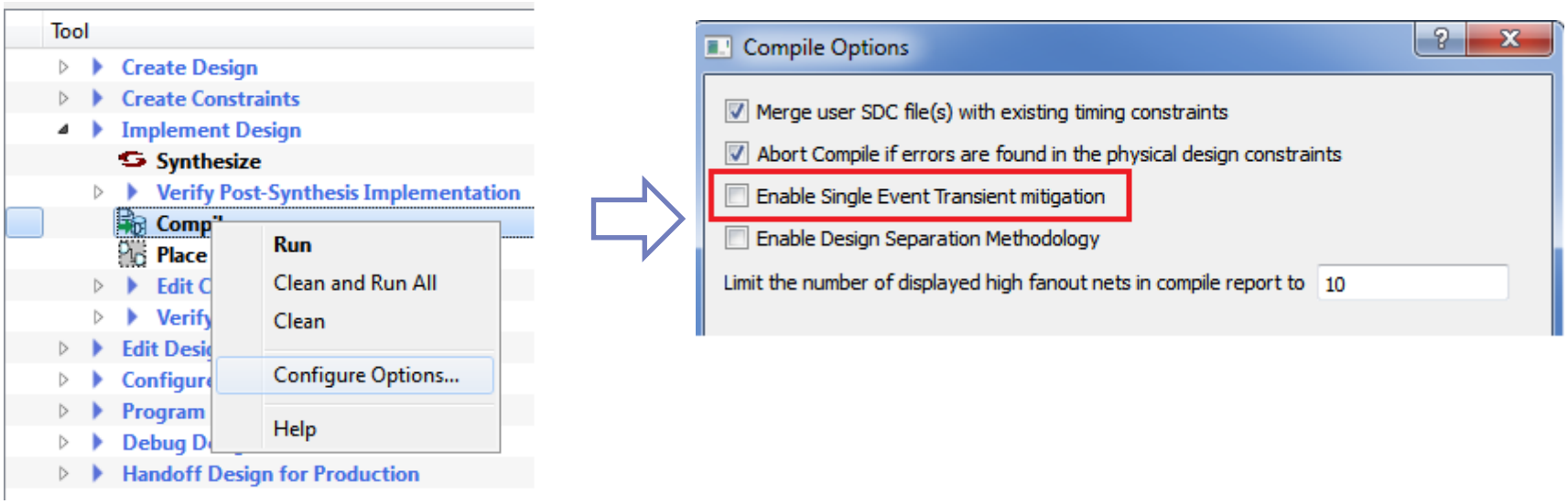
Design Considerations - uPROM

- Update the uPROM content without recompiling or running through the Place & Route flow
  - Only programing file re-generation is required



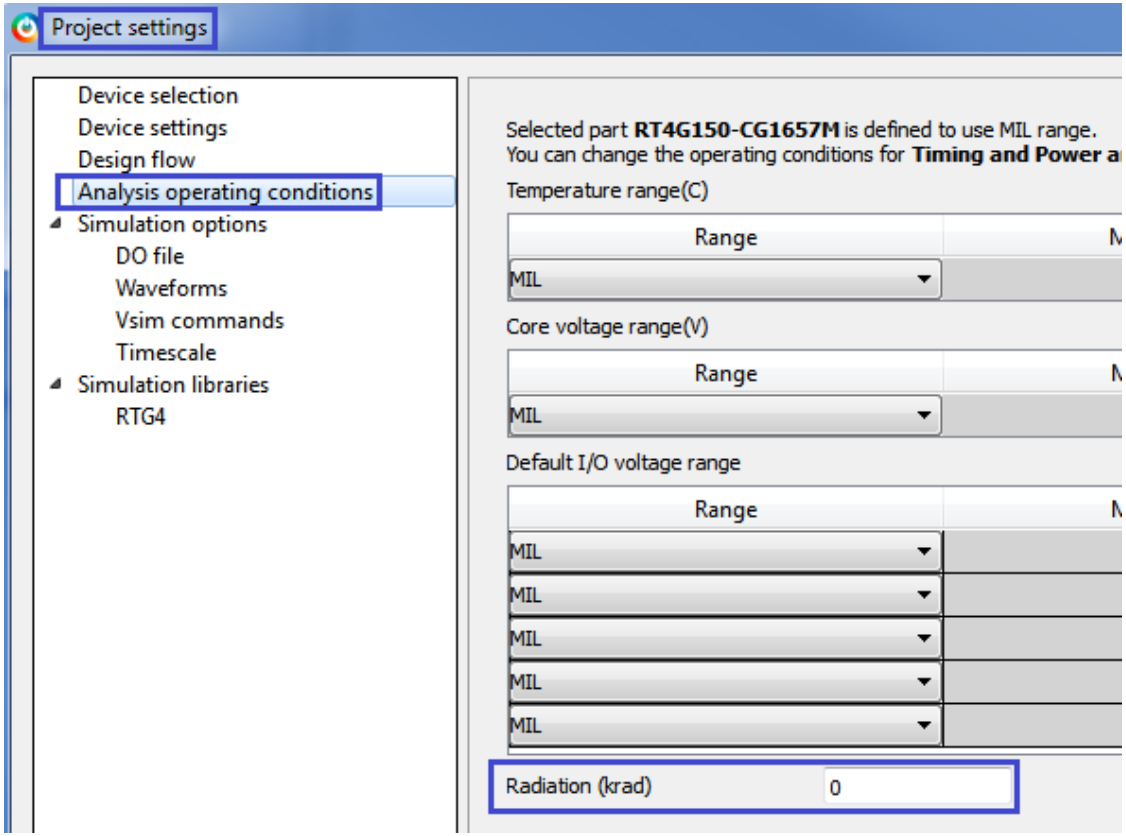
Design Software Options - SET Filter

- Single Event Transient (SET) Mitigation
  - SW provides a Compile option to enable and disable the SET mitigation in the FPGA fabric
  - When the option is checked, SET filters are turned on globally to help mitigate radiation-induced transients. By default, this box is unchecked
    - Individual block SET Filter control is planned for future versions of the Software
  - The setting is propagated to Verify Timing, Verify Power and Back-annotated Netlist for you to perform Timing/Power Analysis
  - There is 943ps Data Setup Time increase with SET filter ON



Design Software Options - Radiation

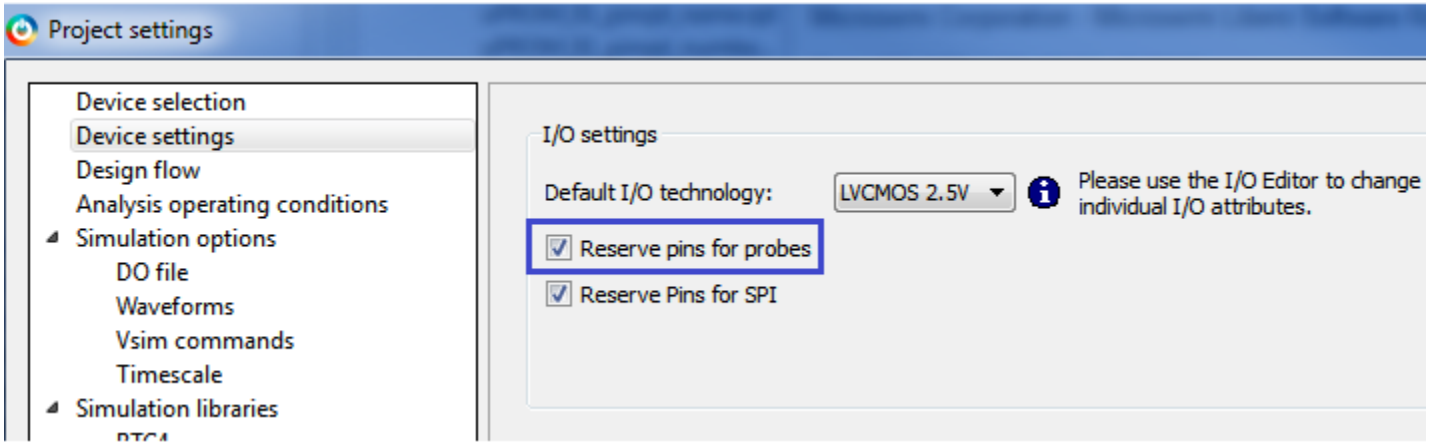
- Option to specify radiation value (in Krad)
  - Valid range is from 0 to 100
- The setting is propagated to Verify Timing, Verify Power and Back-annotated Netlist for you to perform Timing/Power Analysis



Design Software Options - Probes

- RTG4 has two types of Probes
  - One Live Probes channel
  - One dedicate Live capture interface
    - Ability to capture FF contents at the same time and then read back over time.
  - Reserve your pins for probing if you intend to debug using SmartDebug
  - Use SmartDebug debug tool to access the non-invasive probes within the RTG4 devices

- Check “Reserve pins for probes” option to reserve dedicated probe pins
  - If not reserved, probe pins can be used as regular user I/Os



System Controller Suspend Mode

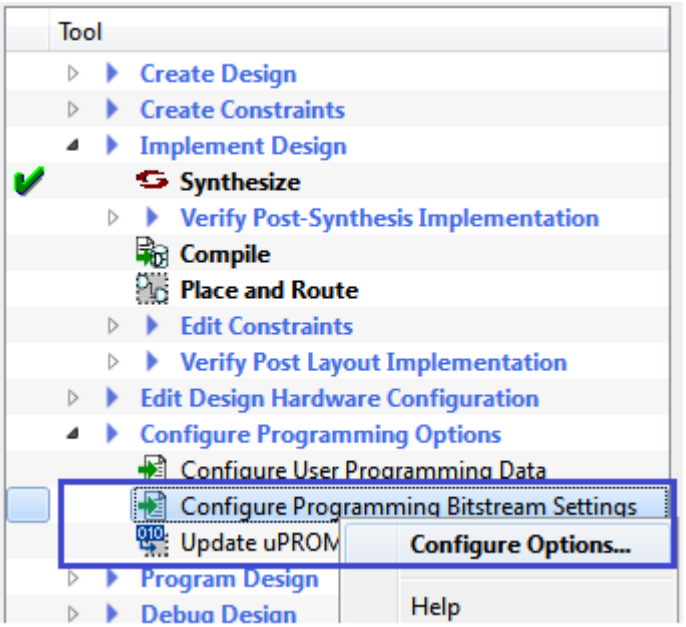
- Use this mode to protect the device from unintended behavior due to single event upset (SEUs) in the System Controller

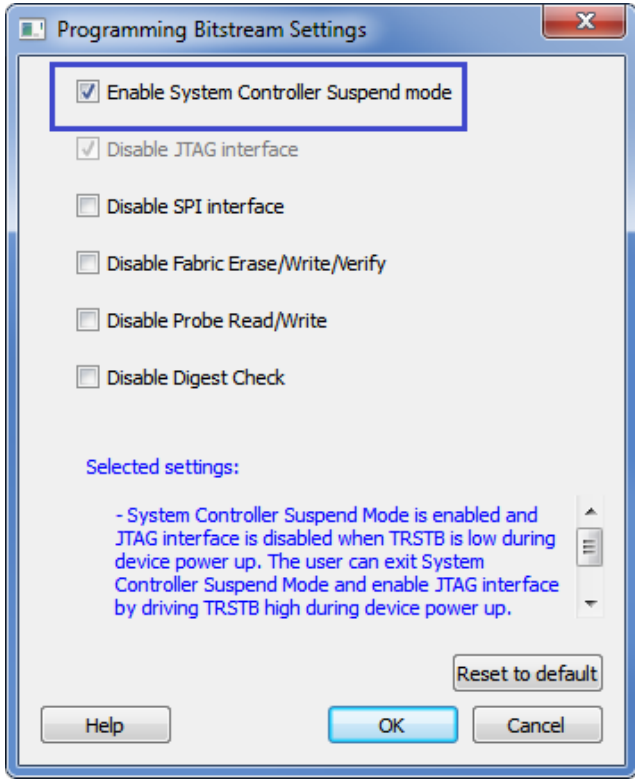
- The System Controller can be held in Suspend mode after device initialization
  - JTAG interface is disabled when System Controller is in Suspend mode
  - System Controller activate if the device is power-cycled or if a hard reset is applied, but it returns to Suspend mode once power-up is completed.
  - System Controller Suspend mode setting is set during device programming
  - The setting is only accessible through the programming file loaded into the device

- To reprogram or debug the device while in System Controller Suspend mode, drive the TRSTB pin High
  - If the TRSTB pin is Low, all the other JTAG input signals are blocked from activating the System Controller
  - When in space, while operational, the TRSTB pin must be held Low

System Controller Suspend Mode

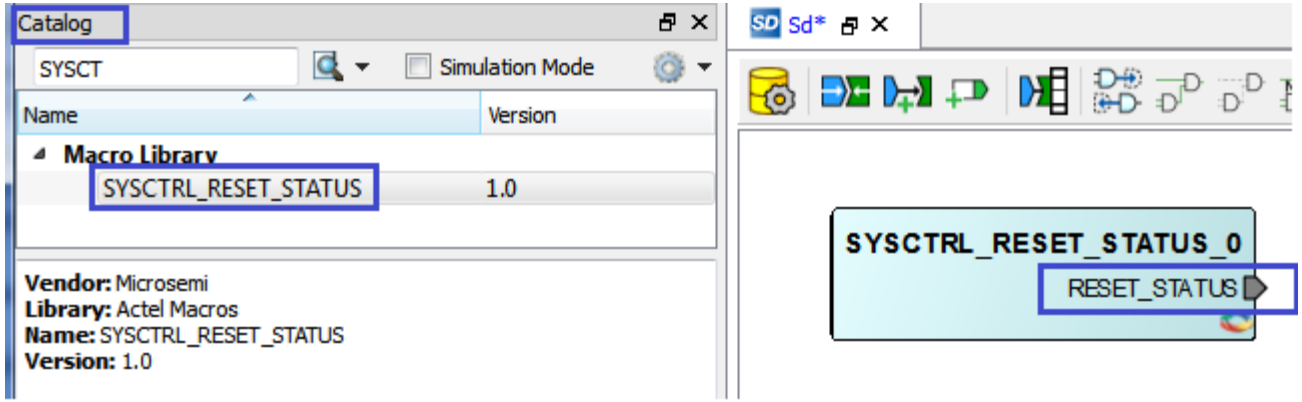
- Enable System Controller Suspend mode Software Option
  - Option is part of a programming bitstream settings
    - Use this option for ground test of design
- You can also exit System Controller Suspend Mode and enable JTAG interface by driving TRSTB high during device power up





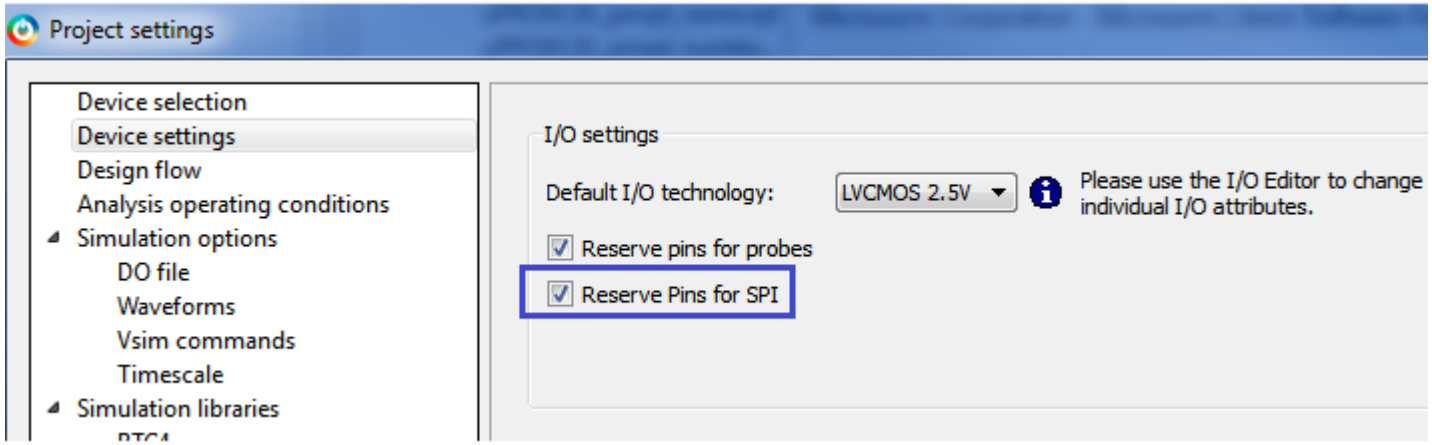
System Controller Suspend Mode

- A RESET_STATUS signal can be monitored to confirm the status of the System Controller
- You get access to this signal by instantiating SYSTEM_RESET_STATUS macro from Libero SoC Catalog
- RESET_STATUS output port will go high if the System Controller is in reset
  - System Controller Suspend Mode option enabled in Libero device setting



SPI Slave Programming – Reserve SPI Pins

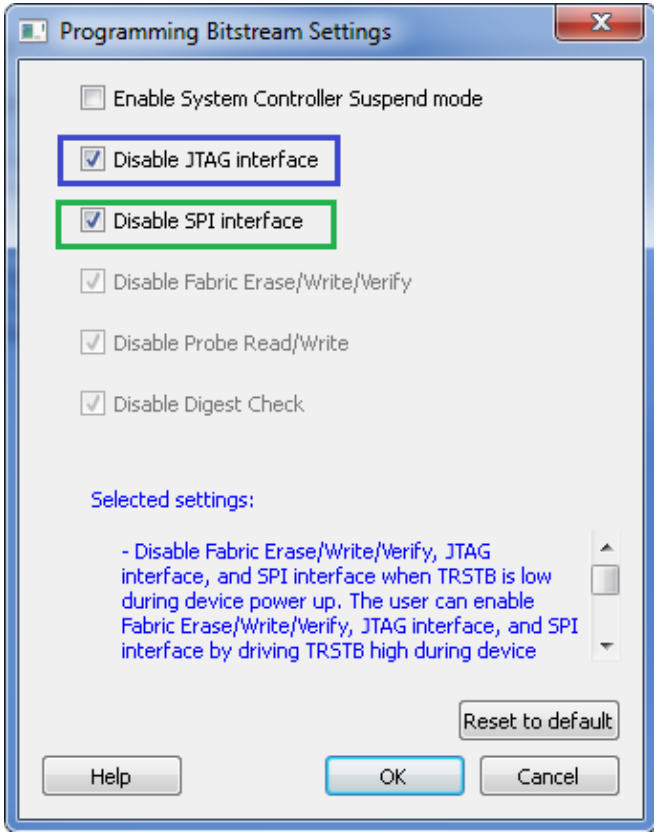
- Dedicate SPI (Slave only) interface as alternative method for programming
  - The SPI block is part of the System Controller
  - SPI-Slave Libero programming through FP5 will be supported in future SW releases
- If the System Controller is not held in Suspend mode, the dedicated SPI-slave interface can be used for programming functions
  - SPI Slave communicates with a remote device such microprocessor that initiates the download of the programming bit stream to the device
- Reserve Pins for SPI
  - Check this box to reserve (four) pins for SPI functionality in Programming



Programming Bitstream Settings

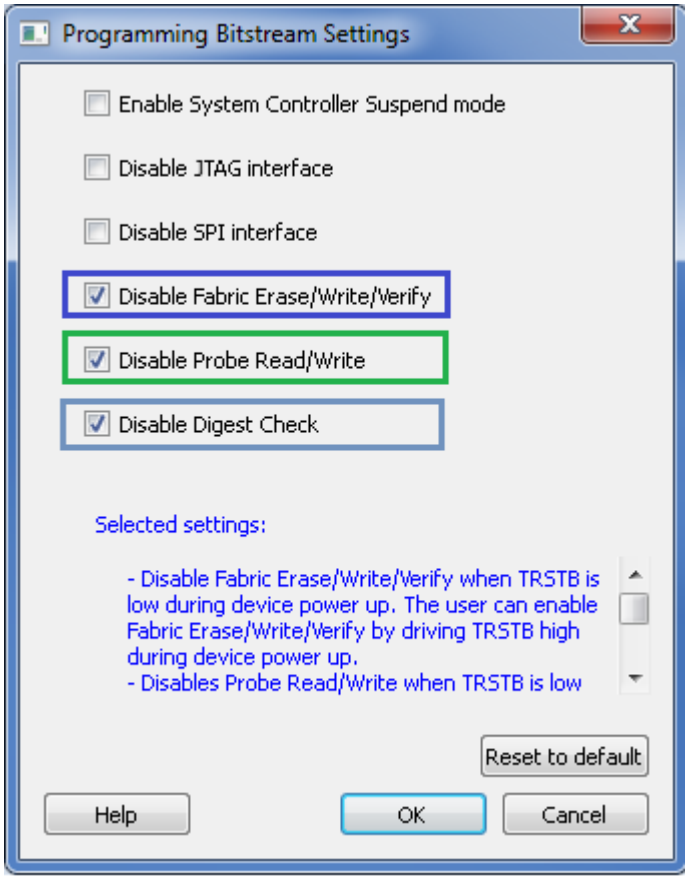
- Disable SPI interface
  - SPI interface is disabled when TRSTB is low during device power up
  - You can enable SPI interface by driving TRSTB high during device power up.
  - For this option to be available, you must reserve pins for SPI in the project settings of the Libero project (refer to the previous slide)

- Disable JTAG interface
  - Disabled when Enable System Controller Suspend mode is Checked
  - Disabled when TRSTB is low during device power up



Programming Bitstream Settings

- Disable Fabric Erase/Write Verify
  - You can enable Fabric Erase/Write/Verify by driving TRSTB high during device power up
- Disable Probe Read/Write
  - For this option to be available, you must reserve pins for Probe in the project settings of the Libero project (refer to previous slides)
- Disable Digest Check
  - Disables all Fabric reads, such as verify digest, read digest, or reading design or programming information in DEVICE_INFO when TRSTB is low during device power up.
  - You can enable Digest Check by driving TRSTB high during device power up



CG1657 Package Pins

- Two devices are available in Libero SoC Software
  - RT4G150_ES CG1657
  - RT4G150 (production) CG1657
- Software generated package pins for RT4G150_ES are not compatible with pins generated for RT4G150 device
  - Due to SpaceWire enhancements
- The following pin mapping tables are provided to help you start designing your board

SpaceWire Pin Mapping from RTG4 ES/MS Silicon to PROTO/Flight Silicon

SpaceWire Pin Mapping from RTG4 ES/MS Silicon to PROTO/Flight Silicon for RTG4 Development Kit

Conclusion

- Libero SoC Software provides full design automation from RTL to Debug
  - Includes Synphony, Synplify, Modelsim, Identify
  - With support for other simulation tools

- ECC support through RAM Configurator
- Automatic initialization for SERDES and FDDR based on user configurations
- SpaceWire RX Clock/Data recovery configuration through CCC configurator
- SET Filter On/Off option to help mitigate radiation-induced transients
- System Controller suspend mode to protect the device from unintended behavior due to single event upset (SEUs)
- Enable/disable System Controller Suspend mode using Programming Bitstream settings
- SPI programming alternative option to JTAG programming
- Debug options using Live Probe and Capture
- uPROM Configurator support

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