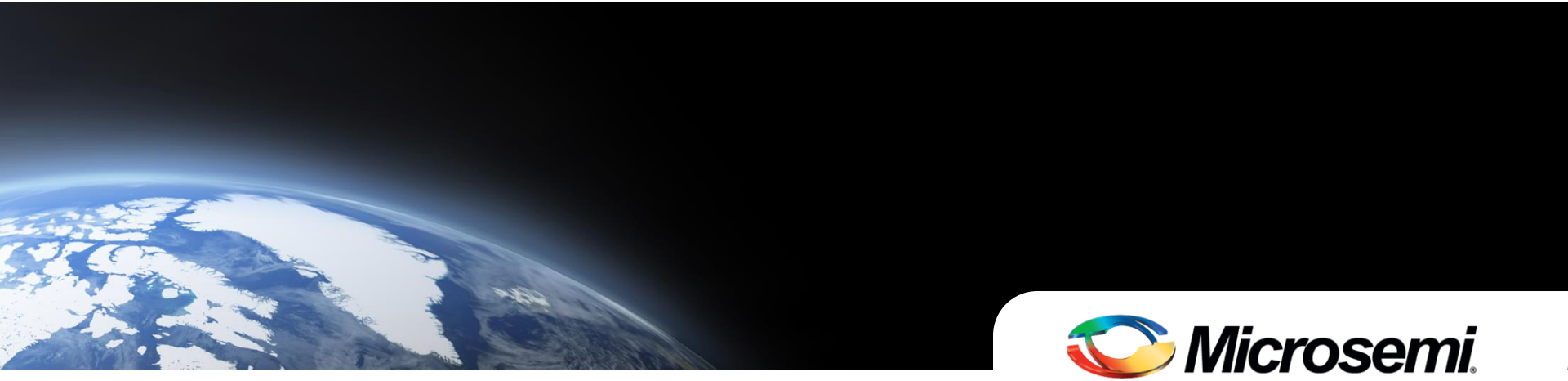
Power Matters.™



RTG4 Next-Generation Radiation-Tolerant FPGAs

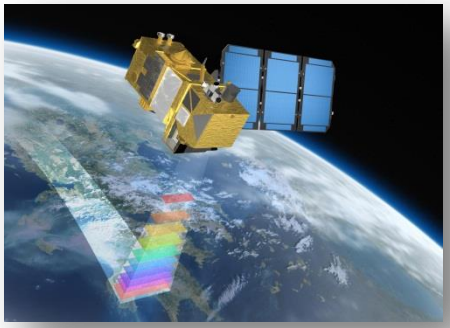
Microsemi Space Forum 2015

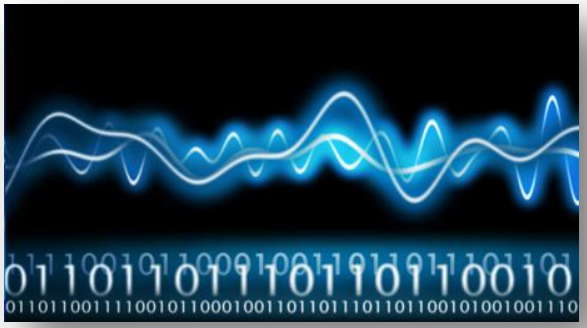
Ken O'Neill
Director of Marketing, Space and Aviation

Microsemi
SPACE FORUM

Satellite Signal Processing Congestion

- Sensor resolution increasing faster than downlink bandwidth
- Satellites required to perform more on-board processing
- Requires high-density, high-performance payload processing electronics





1. Radiation-Hardened ASICs

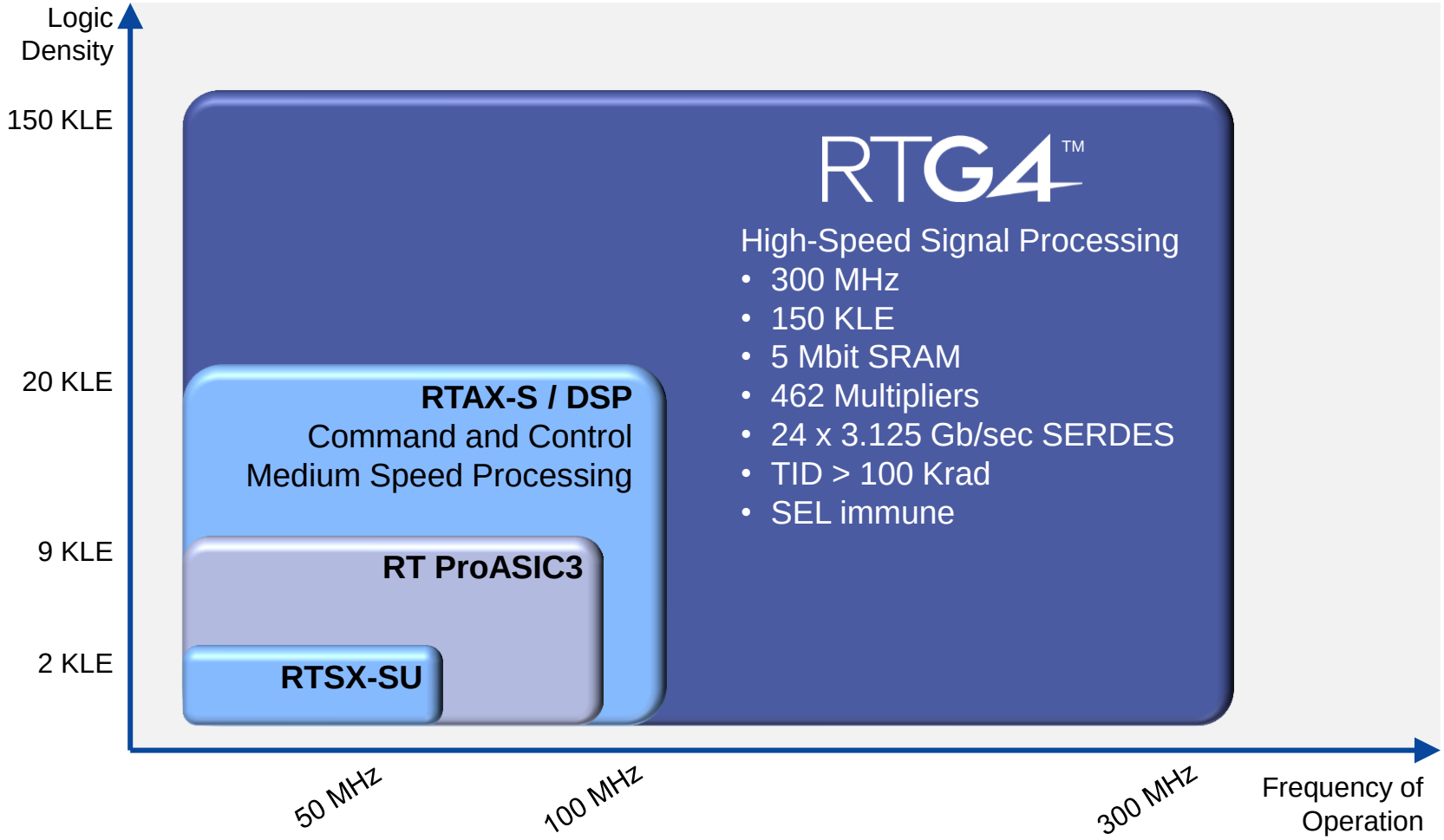
- ☑ High speed, high density, low power
- ☒ Large NRE, relatively low volumes
- ☒ Long development time, long fabrication cycle time
- ☒ High risk of schedule and cost over-runs

2. SRAM FPGAs

- ☑ Easy prototyping, reprogrammable
- ☒ Configuration SEU effects require cumbersome mitigation
- ☒ Increases Size, Weight and Power

Existing solutions for satellite on-board processing have high risks

Introducing RTG4 High-Speed RT FPGAs



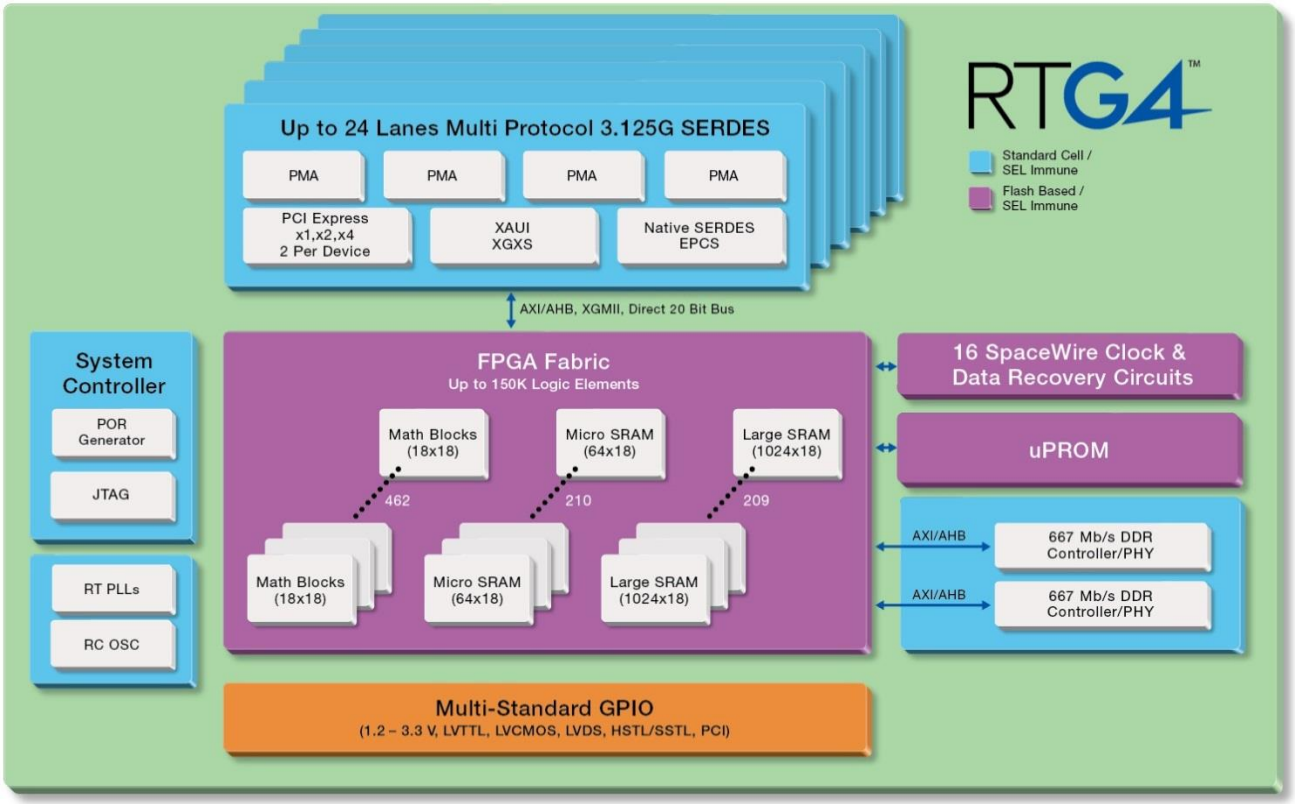
RTG4 mitigates risks of ASICs and SRAM FPGAs, and has 20X improvement in signal processing throughput

Why RTG4 is Compelling

- More flexible than an RH ASIC
  - Reprogrammable, no NRE, no cost and schedule risk
- More signal-processing features than any other RT FPGA
  - More registers, combinatorial logic, multiply blocks, and transceivers
  - Lower power, live at power-up, no external boot memory needed
- Radiation enhanced for Geosynchronous Earth Orbit and deep space
  - RTG4 65nm Flash has complete immunity to configuration upsets (SEU)
  - Total ionizing dose (TID) and single event effects (SEE) hardened by design

RTG4 offers groundbreaking features for satellite applications

RTG4 Radiation-Mitigated Architecture



- Total-dose hardening of Flash cells
- Single-event hardening of registers, SRAM, multipliers, PLLs

Comprehensive radiation-mitigated architecture for signal processing applications

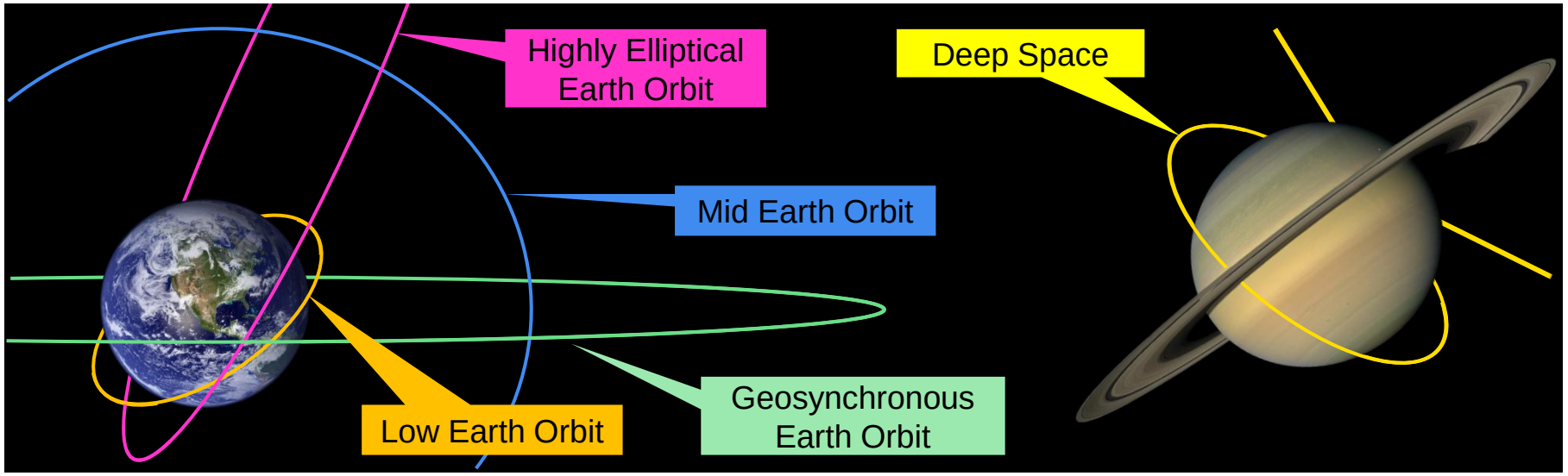
RTG4 Resources

Resources	RT4G150
Logic Elements (TMR Register + 4-Input C Logic)	151,824
18x18 Multiply-Accumulate Blocks	462
RAM Mbits (1.5 Kbit and 24 Kbit Blocks, with ECC)	5.2
UPROM Kbits	381
DDR2/3 SDRAM Controller (with ECC)	2x32
PCI Express Endpoints	2
Globals	24
PLLs (Rad Tolerant)	8
SpaceWire Clock & Data Recovery Circuits	16
User IO (excluding SERDES)	720
SERDES lanes (3.125 Gbit/sec)	24
Hermetic, Ceramic Column-Grid Packages	
CG1657 (Six Sigma Columns)	✓

- RT4G150 is available now in Engineering Samples
- Possible CQFP package – engineering investigation in progress now

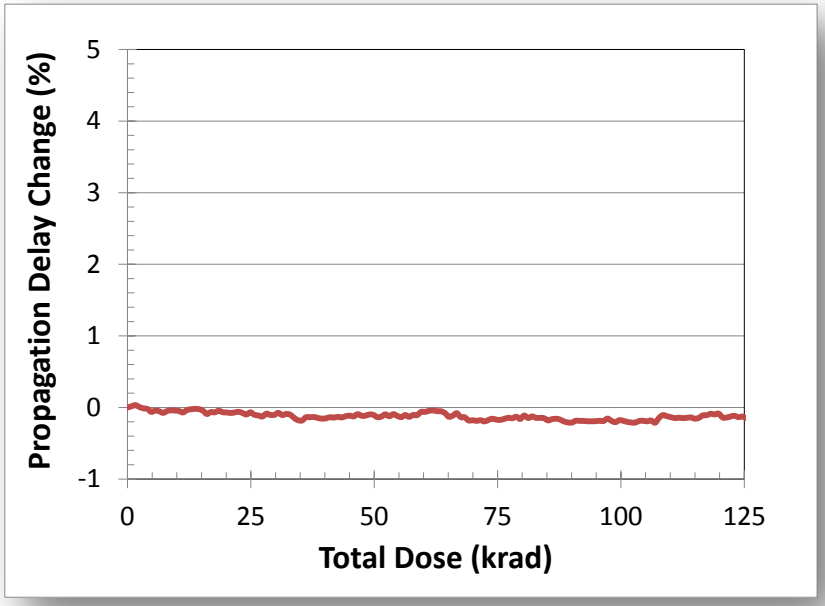
RTG4 Radiation Mitigation

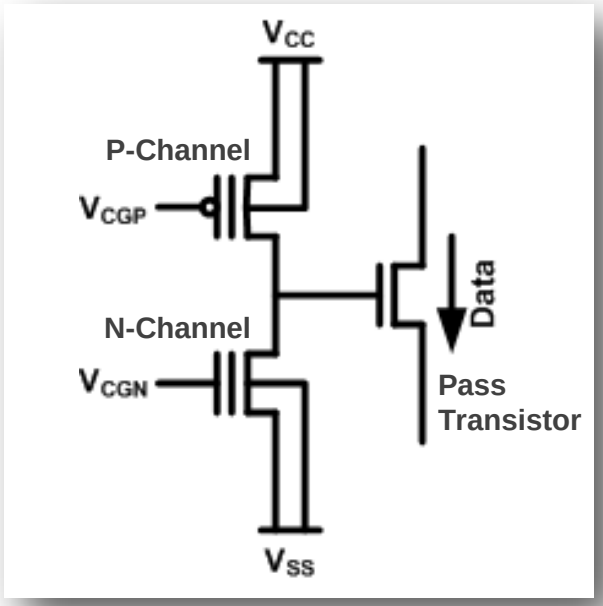
- Radiation hardening by design
  - Total ionizing dose (TID) immune to > 125 kRAD
  - Single event latch-up and configuration upset immune
    - Tested to 103 MeV-cm^2/mg (facility limit) at 100°C
  - Single event upsets in fabric < 1x10^{-11} errors/bit/day
  - Single event transient mitigation in logic can be enabled/disabled globally or individually for higher performance



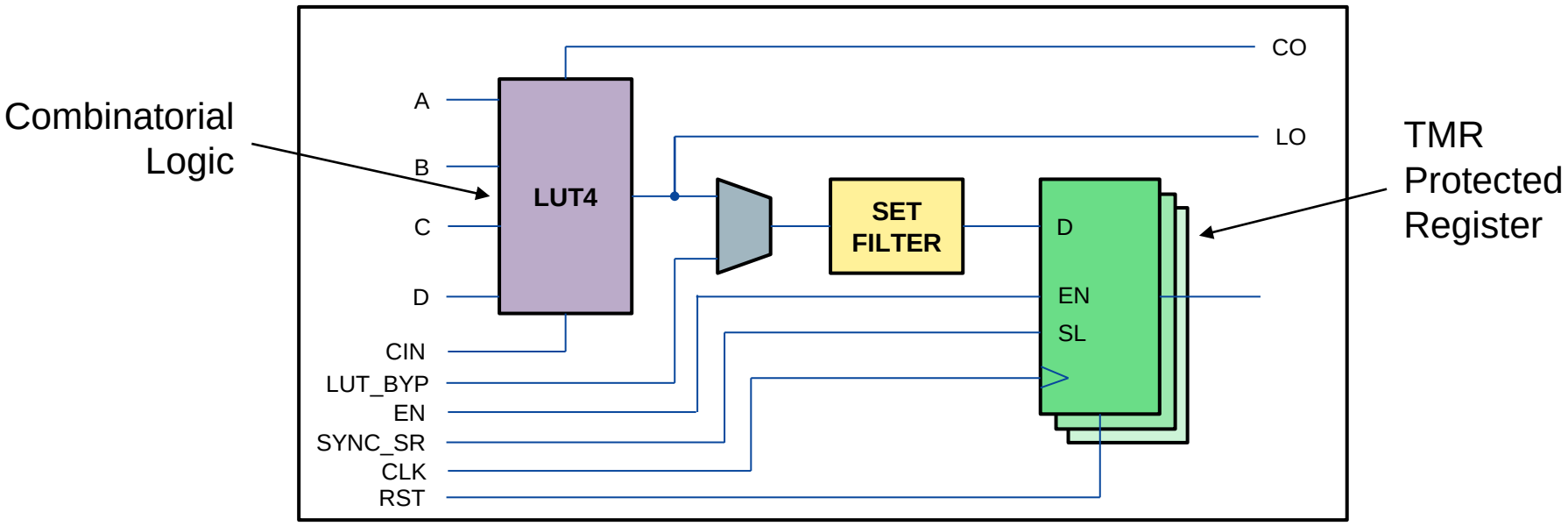
TID Mitigation in RTG4 Flash FPGAs

- RTG4 TID-tolerant interconnect
  - RTG4 FPGAs functional after TID > 125 Krad
  - Change in propagation delay ~ 0% after TID > 125 Krad
  - Pass transistor is indirectly coupled to floating gate devices
  - V_T changes in Flash cells don't change pass transistor prop. delay





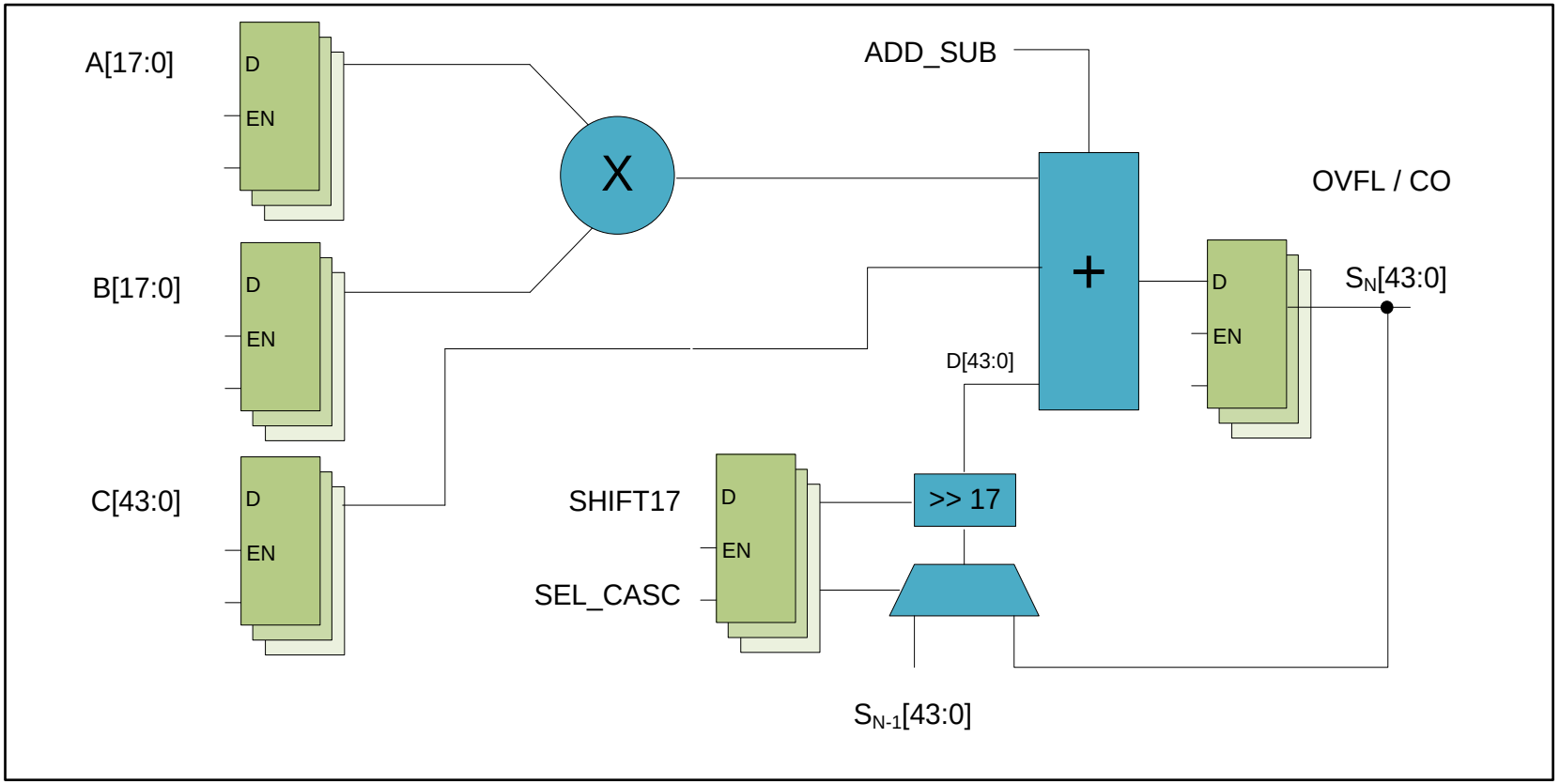
RTG4 Logic Element Radiation Mitigation



RTG4 Logic Element (LE)

- Dedicated register with efficient triple module redundant (TMR) hardening
- Single event transient (SET) filter mitigates radiation glitches from comb. logic
- Hierarchical routing architecture enables >95% module utilization

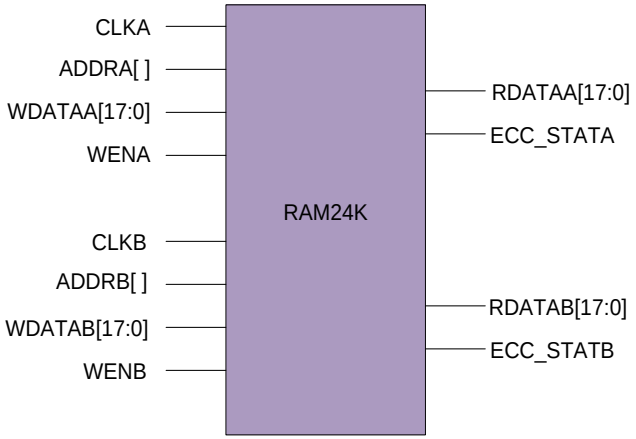
RTG4 Mathblock

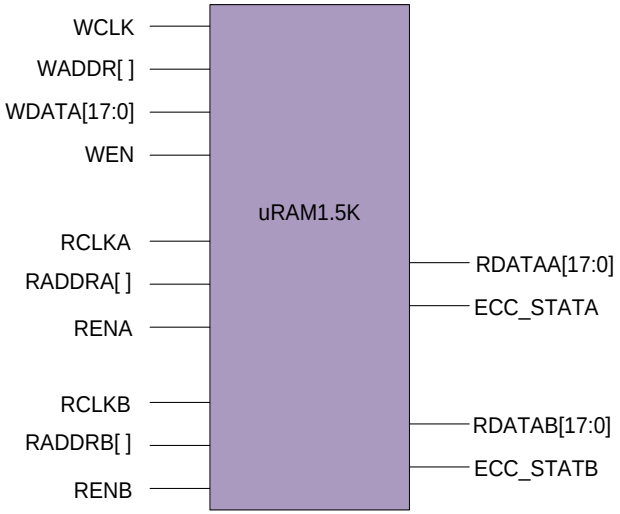


- 18 x 18 multiplier with advanced accumulate
- High performance for signal processing throughput
- Optional SEU-protected registers on inputs and outputs (including C input)

RTG4 Memory Blocks

- Radiation Tolerant
  - Resistant to multi-bit upset
  - Built-in optional EDAC (SECDED)
- LSRAM – up to 24 KBit
  - Dual-port and two-port options
  - High performance synchronous operation
  - Example usage
    - Large FFT memory
- uRAM – up to 1.5 KBit
  - Three Port Memory
    - Synchronous Write Port
    - Two Asynchronous or Synchronous Read Ports
  - Example usage
    - Folded FIR filters and FFT twiddle factors



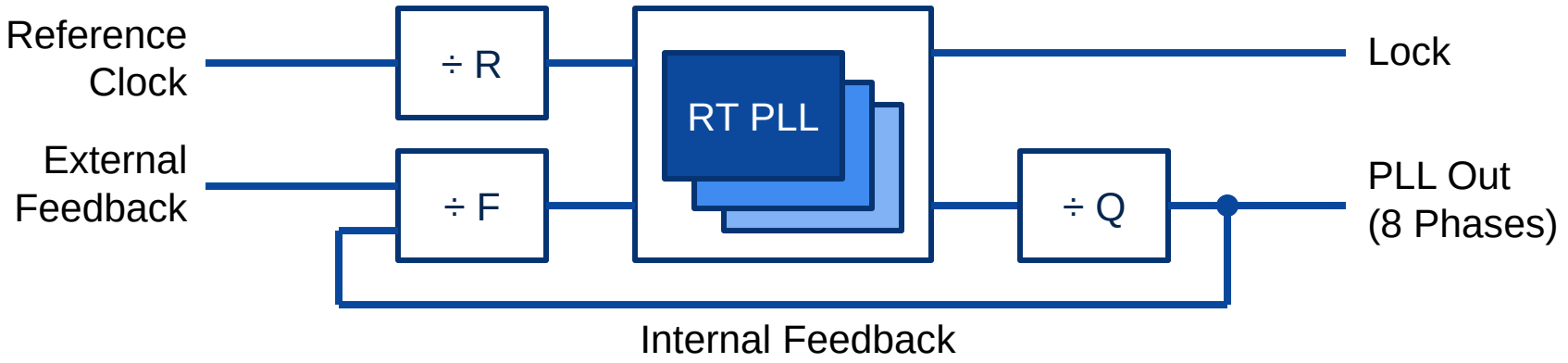


RTG4 General Purpose IO

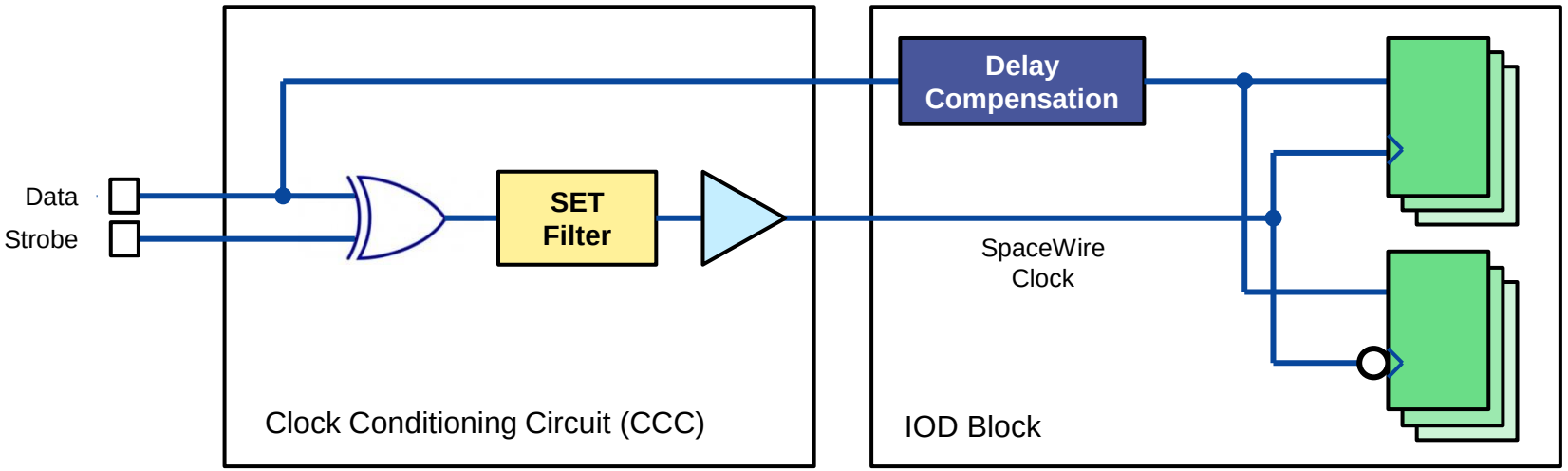
- Single ended standards
  - LVCMOS from 1.2V to 3.3V
  - LVTTL
  - PCI
- Voltage reference standards (600+ Mbps)
  - Includes on-chip termination
  - SSTL2, SSTL18 and SSTL15
    - For DDR2/DDR3 SDRAM memories
  - HSTL18 and HSTL15
    - For SRAM memories
- Differential I/O standards
  - Includes on-chip termination
  - Mini-LVDS, M-LVDS, RSDS, LVPECL

RTG4 Radiation-Tolerant PLL

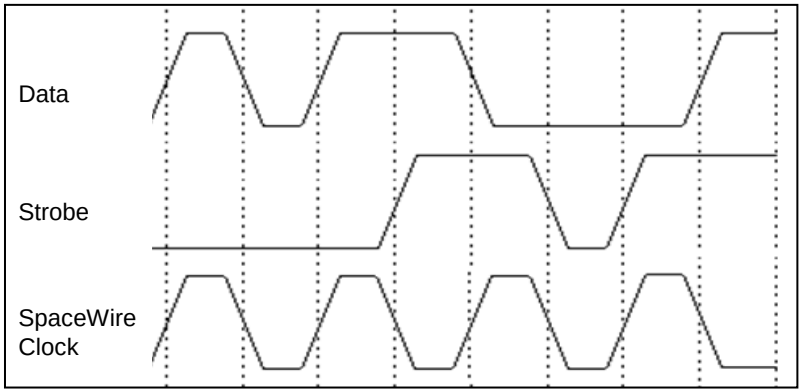
- Radiation-Tolerant PLLs are used in CCC, SERDES and DDR blocks
- Triple module redundant (TMR) PLL in internal feedback mode
  - Reference clock is fed back to all 3 sub-PLLs independently
  - Sub-PLL is SEL immune
- Single PLL in external feedback mode
  - PLL output travels through clock network and is fed back to PLL
  - Common mode used for clock network delay compensation
  - Only 1 sub-PLL is enabled in this mode
  - Sub-PLL is SEL immune



Hardened SpaceWire Clock Recovery



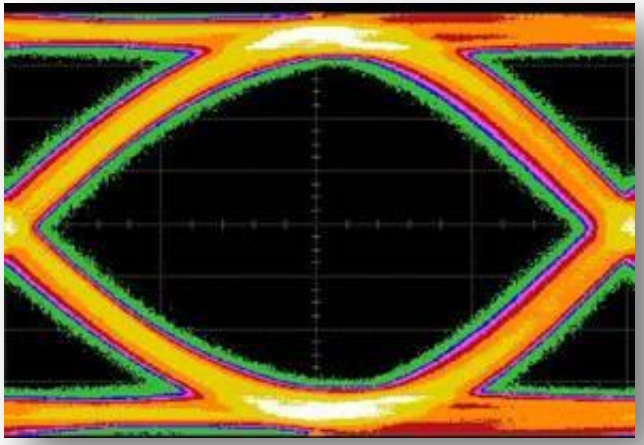
- SpaceWire interface used for command-and-control and data
  - Data and Strobe are XORed to recover SpaceWire clock
  - Hardwired and SET protected
  - Delay compensation available to align data and SpaceWire clock
  - 16 SpaceWire Clock Recovery circuits on each RTG4

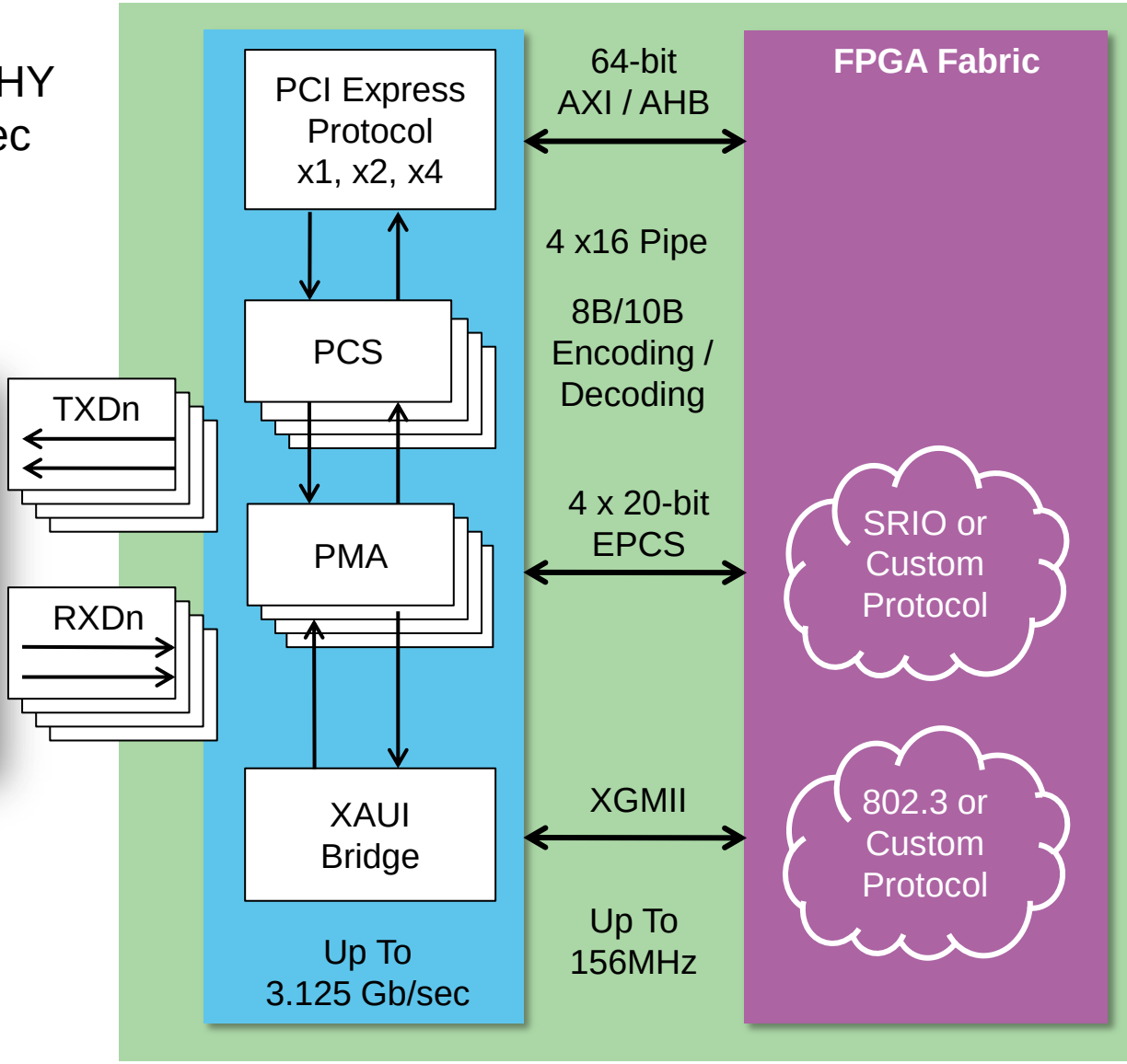


Unique Microsemi RTG4 Feature

3.125 Gb/sec SERDES

PMA Based on PCIe Gen 1 PHY
Performance 1 to 3.125 Gb/sec
Up to 6 blocks with 4 lanes



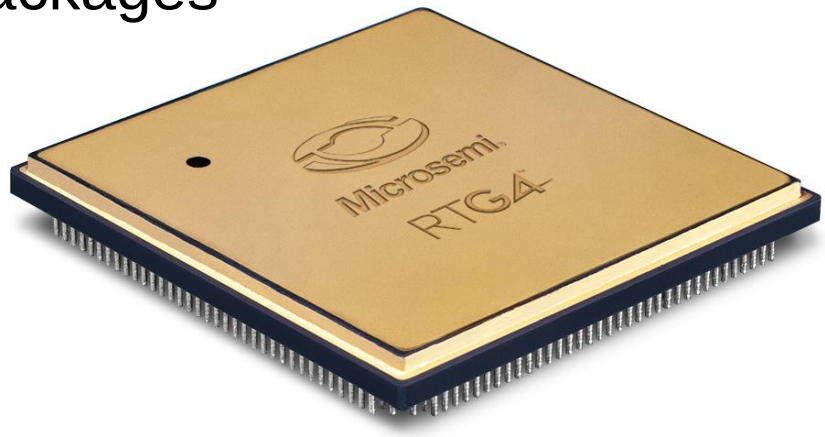


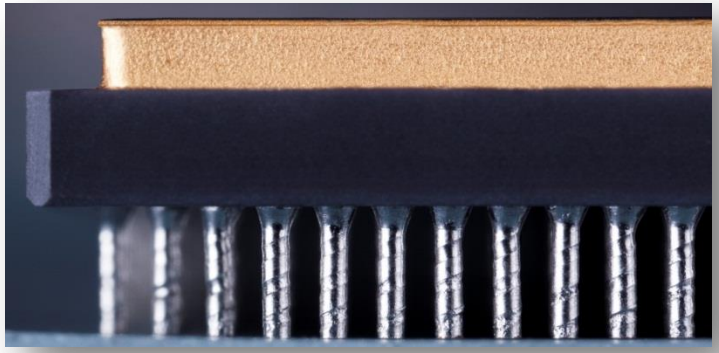
RTG4 Performance

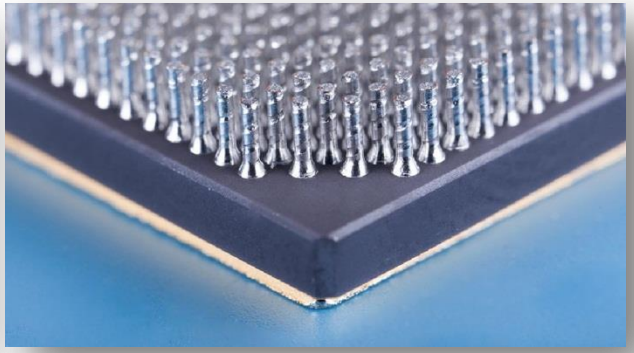
- FPGA logic
  - 250 MHz system performance with SET mitigation
  - 300 MHz system performance without SET mitigation
- DSP mathblock
  - 250 MHz pipelined performance with SET mitigation
  - 300 MHz pipelined performance without SET mitigation
- LSRAM24K and uRAM1.5K
  - > 300 MHz
- IO
  - > 600 Mb/sec LVDS and 667 Mb/sec DDR2/3 SDRAM data
  - SERDES > 3.125 Gb/sec

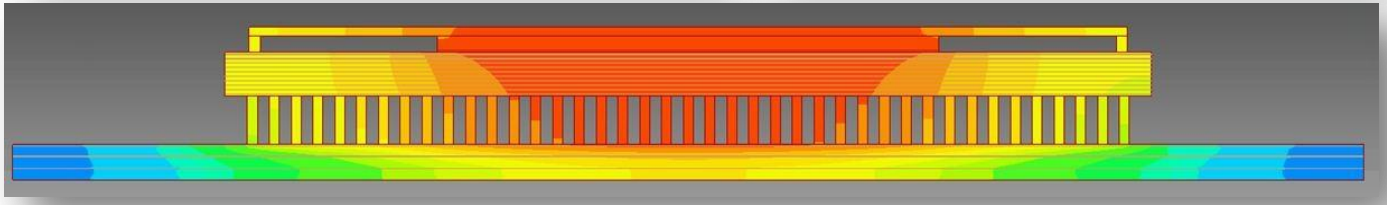
RTG4 Packaging

- Hermetically sealed, ceramic packages
  - Embedded decoupling capacitors
    - Flight models will have Precious Metal Electrode (PME) capacitors
  - Column Grid Array, Ball Grid Array, Land Grid Array









RTG4 Design Ecosystem

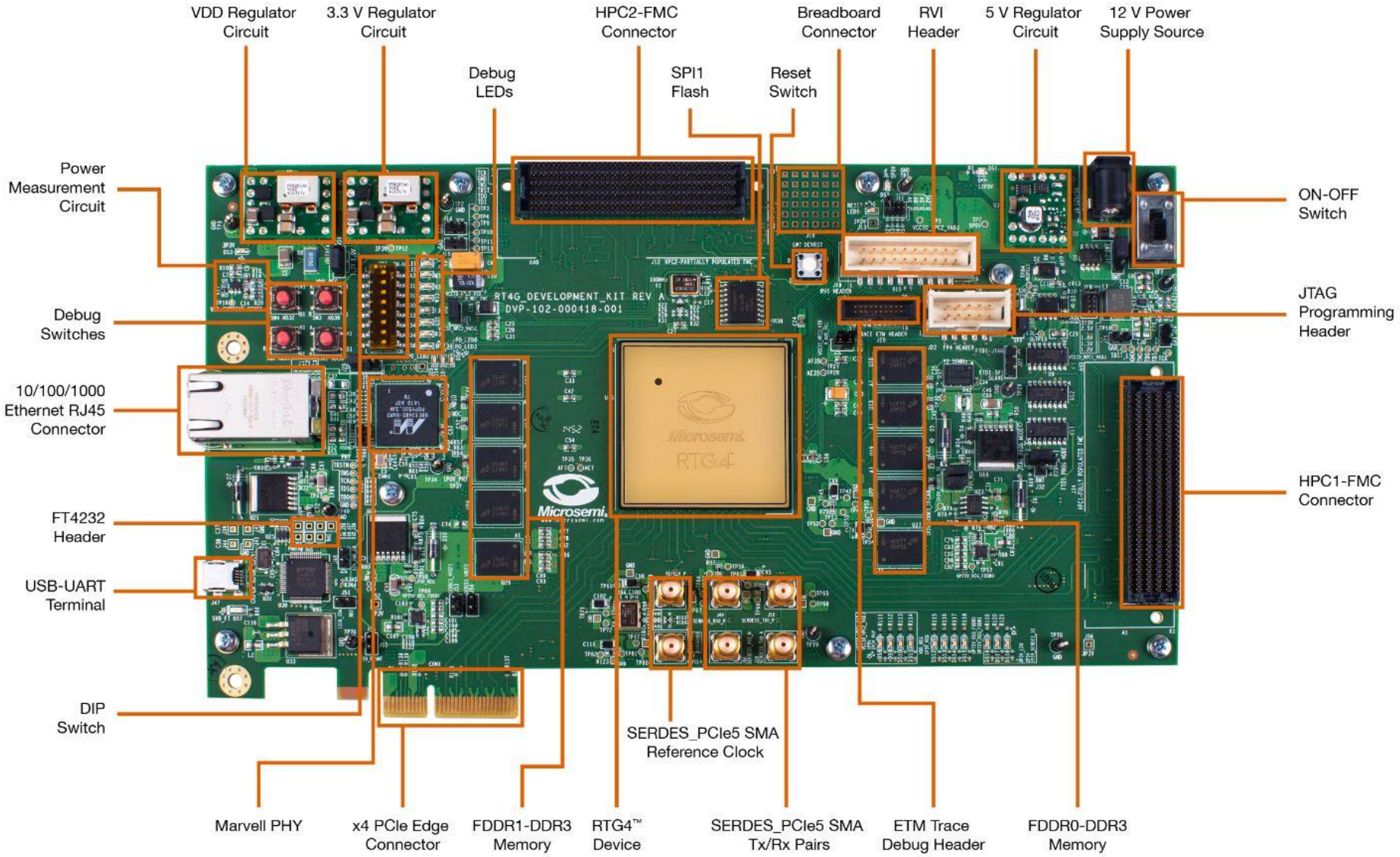
Mentor Graphics
ModelSim®

SYNOPSYS
Synplify Pro®
Synphony Model Compiler

MathWorks
MATLAB®
Simulink®

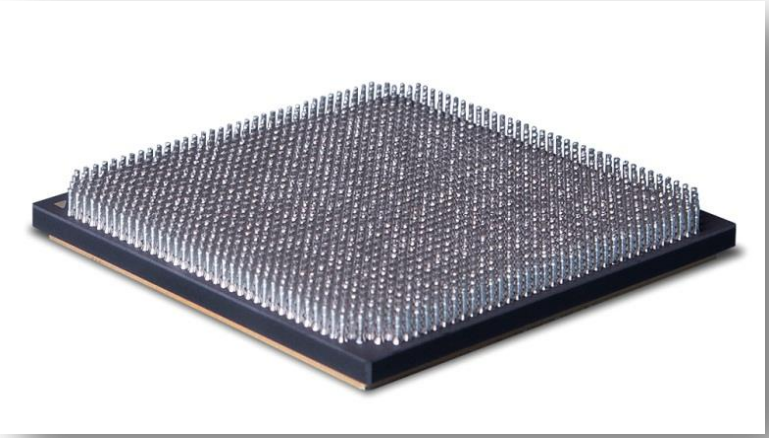
- Libero SoC Design Suite
  - Synplify Pro® synthesis
  - ModelSim® simulation
  - Power-driven place-and-route
  - SmartPower power analysis
  - SmartTime timing analysis
  - SmartDebug in-circuit FPGA debug
- Ease of Design Focus
  - Push button flow - Proceed from synthesis to programming in one click
  - Reduced learning curve
  - Rich IP library & user block support facilitates design reuse
  - Working with IP partners to expand the RTG4 Ecosystem

RTG4 Development Kit

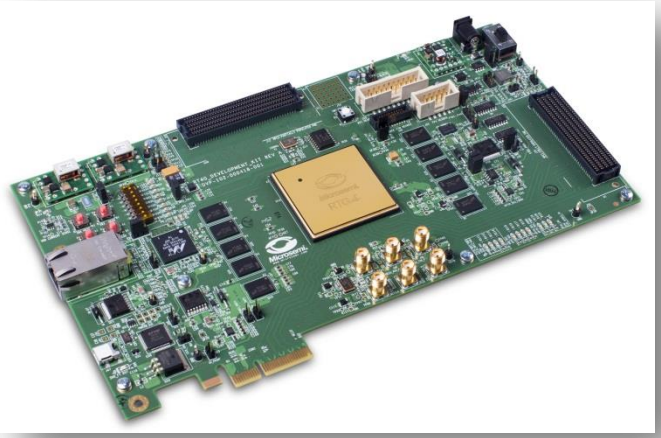


RTG4 Product Availability

- RTG4 devices for space flight applications
  - Engineering Silicon RT4G150 FPGAs: ***NOW***
  - Libero SoC Design Software: ***NOW***
  - RT4G150 development kit: ***NOW***
  - Daisy chain packages: ***NOW***
  - MIL-STD-883 class B flight units: First Half 2016
  - QML class Q qualification: End 2016 or Early 2017
  - QML class V qualification: Targeting Late 2017



Ceramic Column Grid Array Package

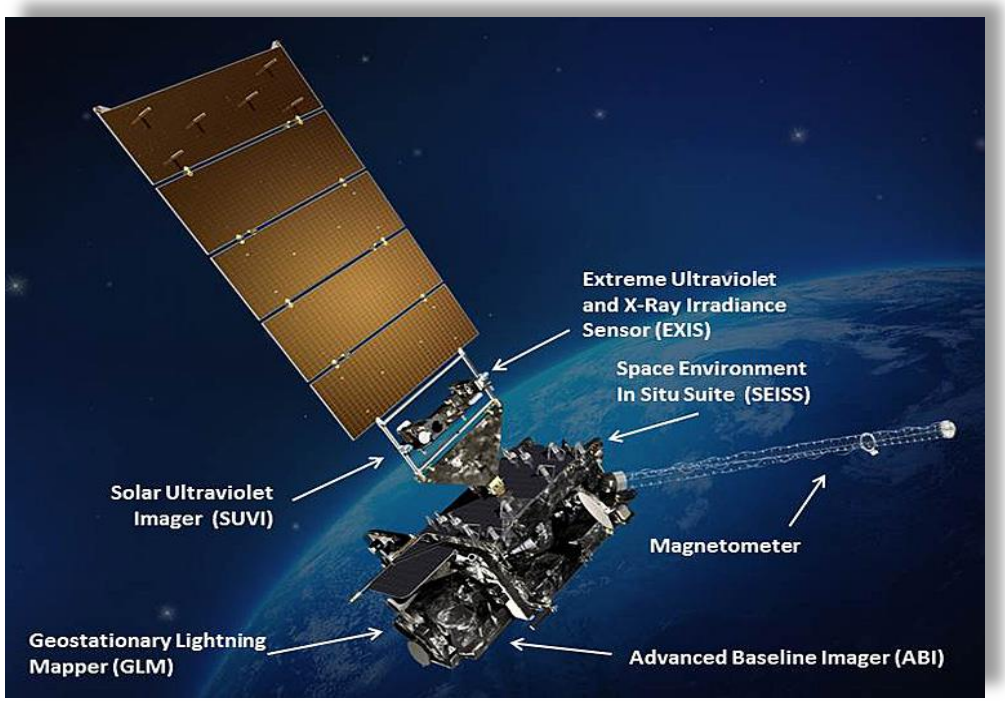


RT4G150 Development Kit

RTG4 in Satellite Applications

Where RTG4 Adds Value

- Roughly 100 remote sensing satellites > 50Kg each year
  - Each may have up to 8 payload instruments
  - Each instrument may require 1 to 12 RTG4 FPGAs

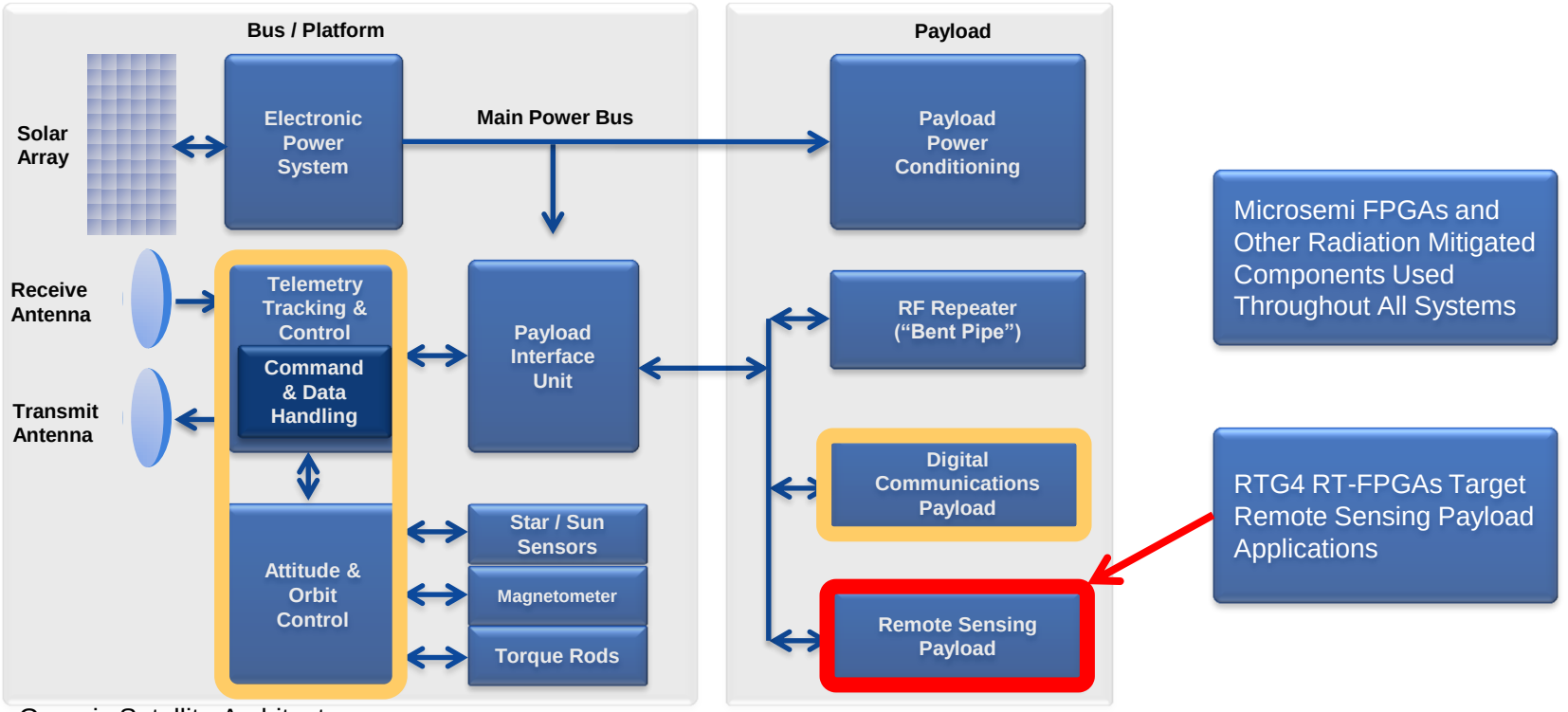


GOES-R Program: 4 satellites, each with 6 instruments

The number of payload instruments which need the flexibility and performance of RTG4 is growing

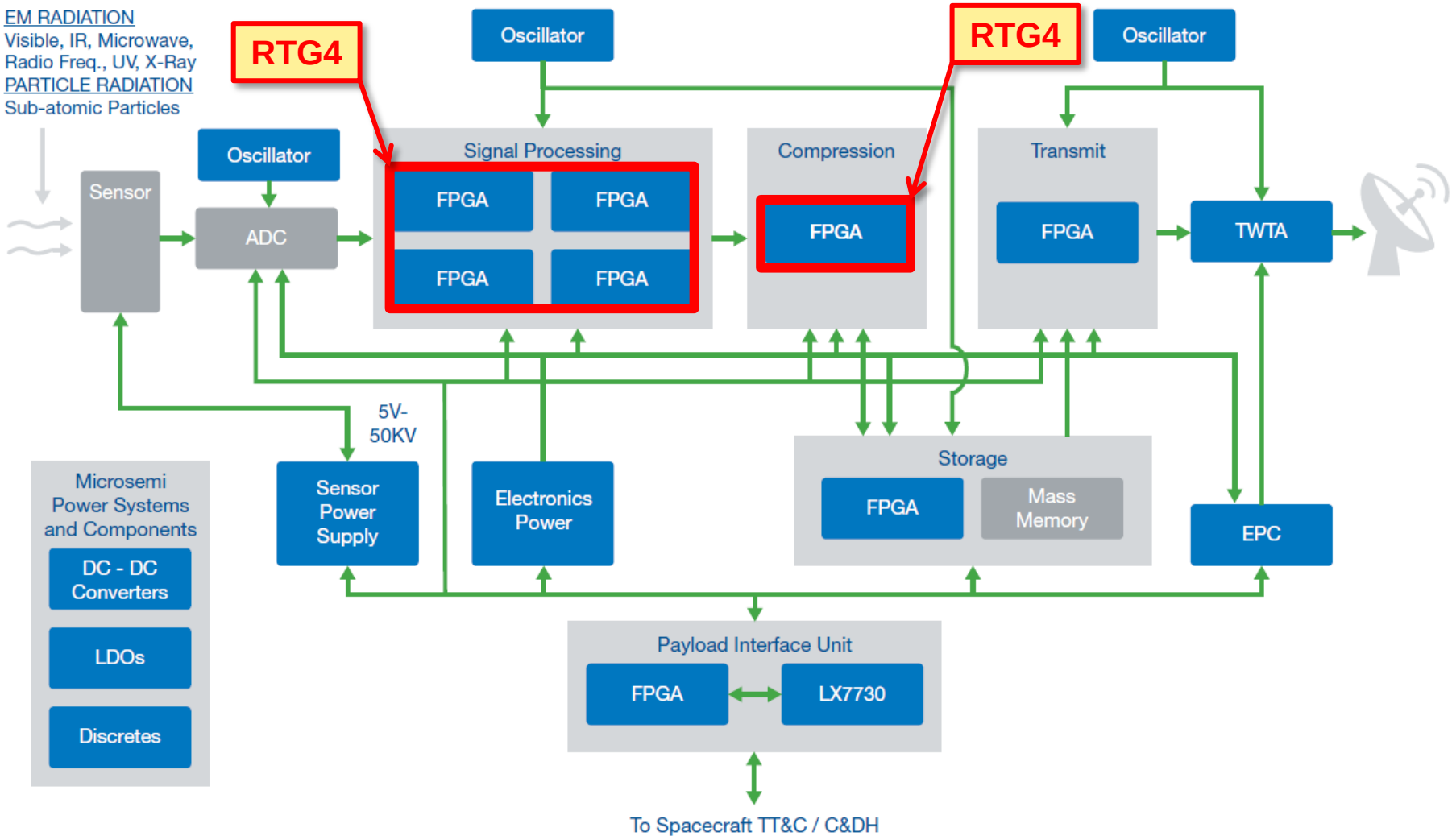
RTG4 Delivers High-Speed Signal Processing

- RTG4 satisfies needs primarily in remote sensing payloads
  - Also adds value in digital communication payloads, and in combined telemetry tracking & control (TT&C) and attitude & orbit control (A&OC) systems
- Microsemi products are found in every system on modern satellites



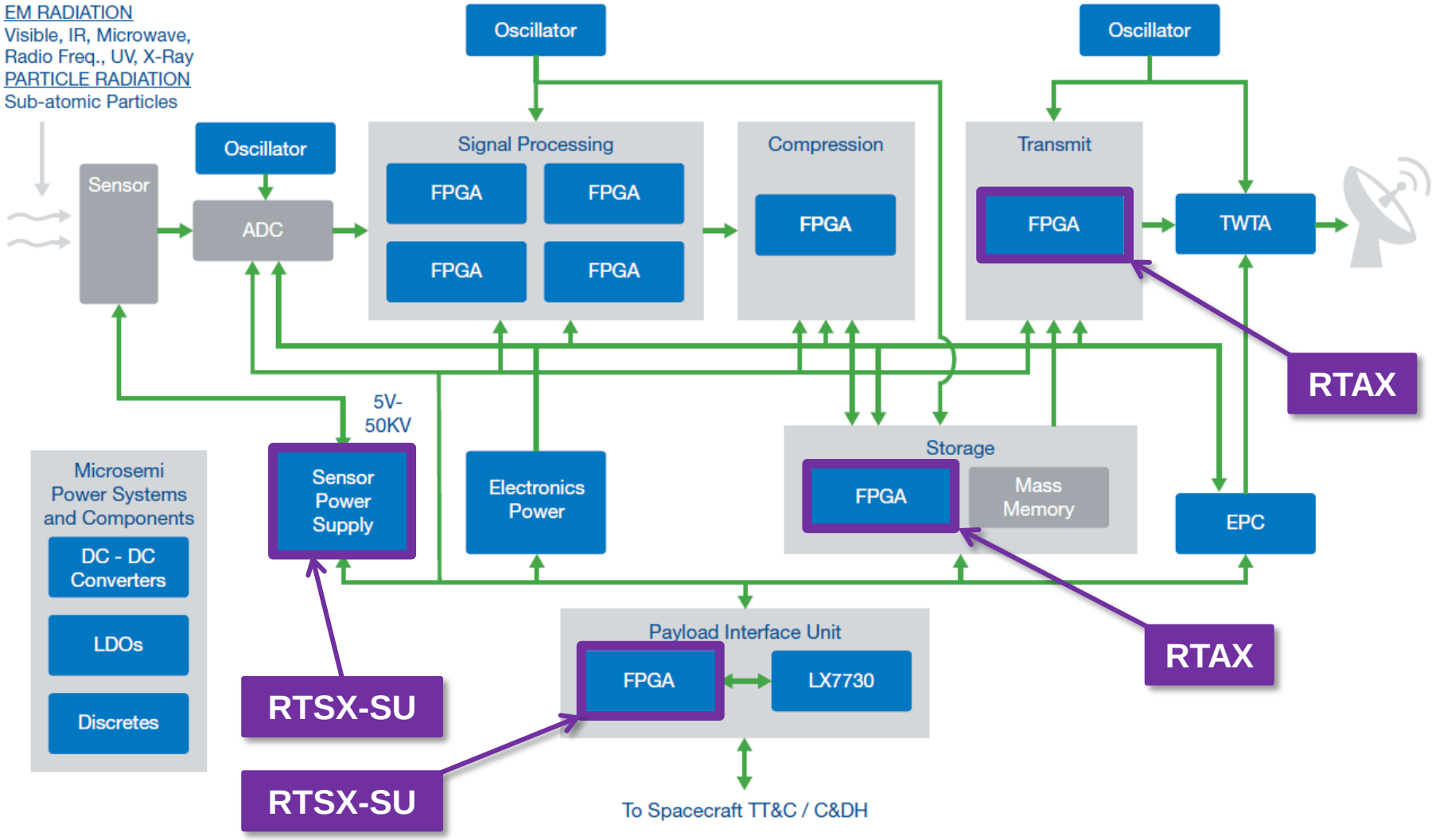
Generic Satellite Architecture

FPGAs in Remote Sensing Payload



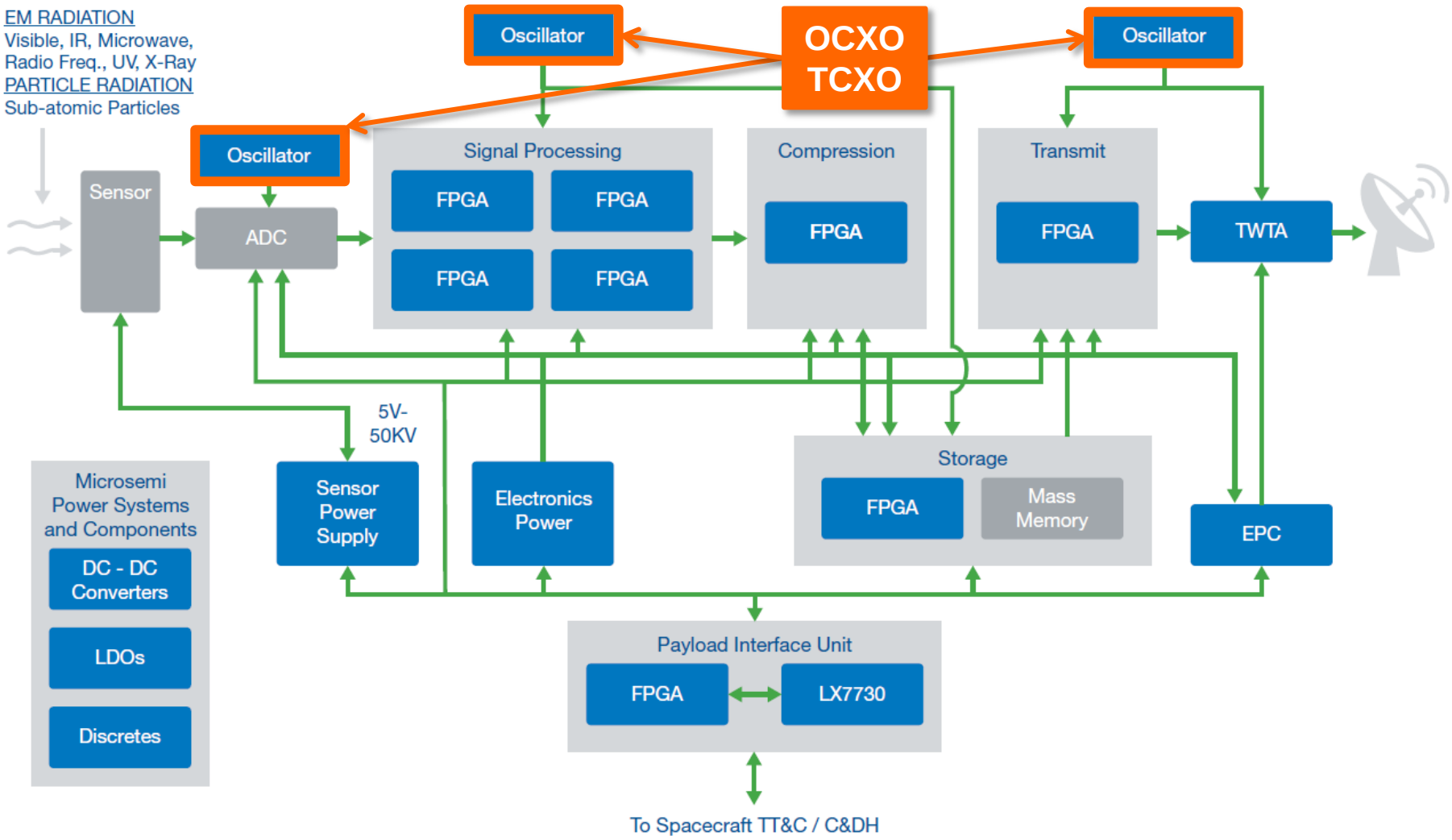
RTG4 complements existing Microsemi Radiation Tolerant FPGAs

FPGAs in Remote Sensing Payload



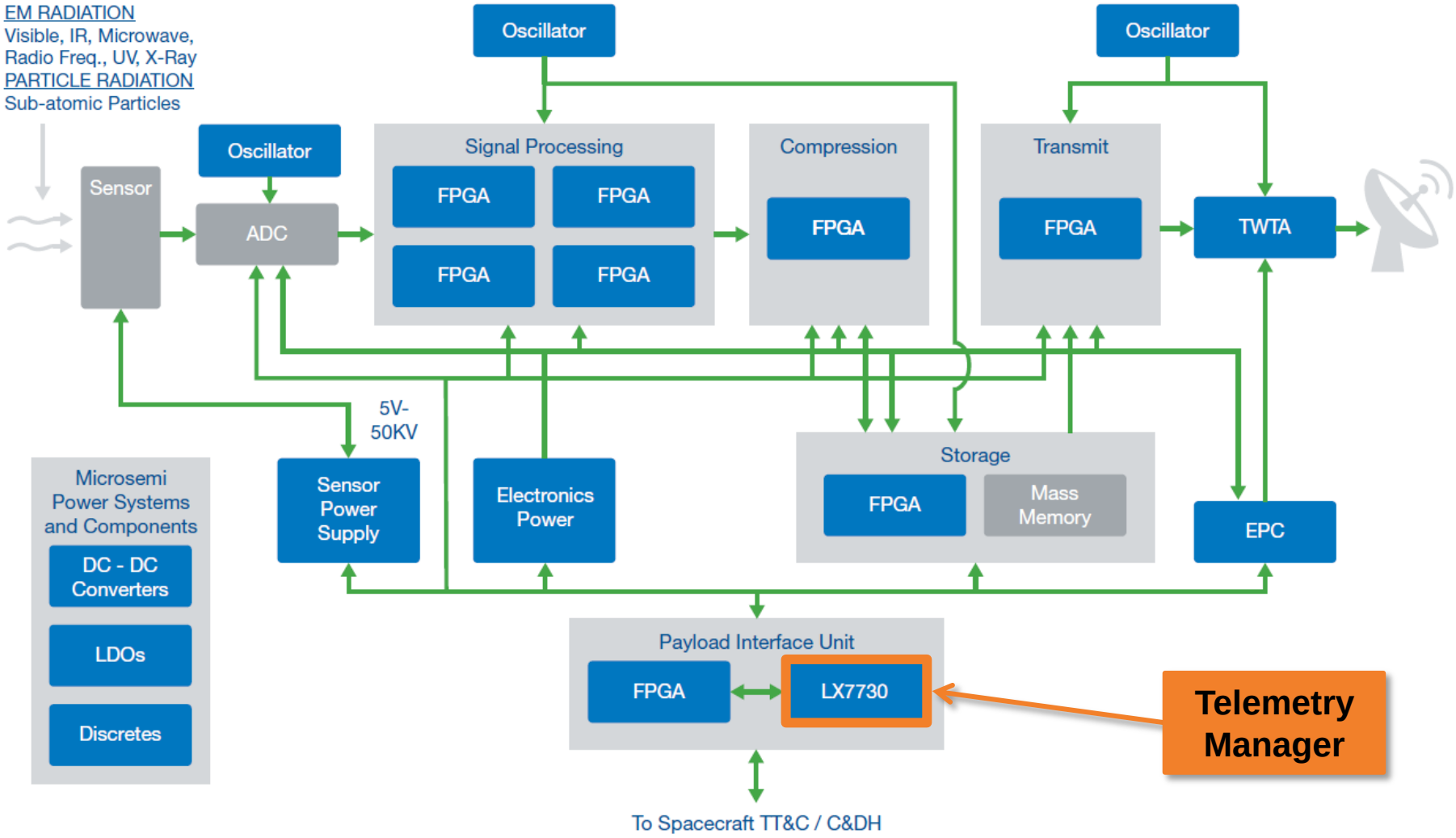
RTG4 complements existing Microsemi Radiation Tolerant FPGAs

Timing Products in Remote Sensing Payload



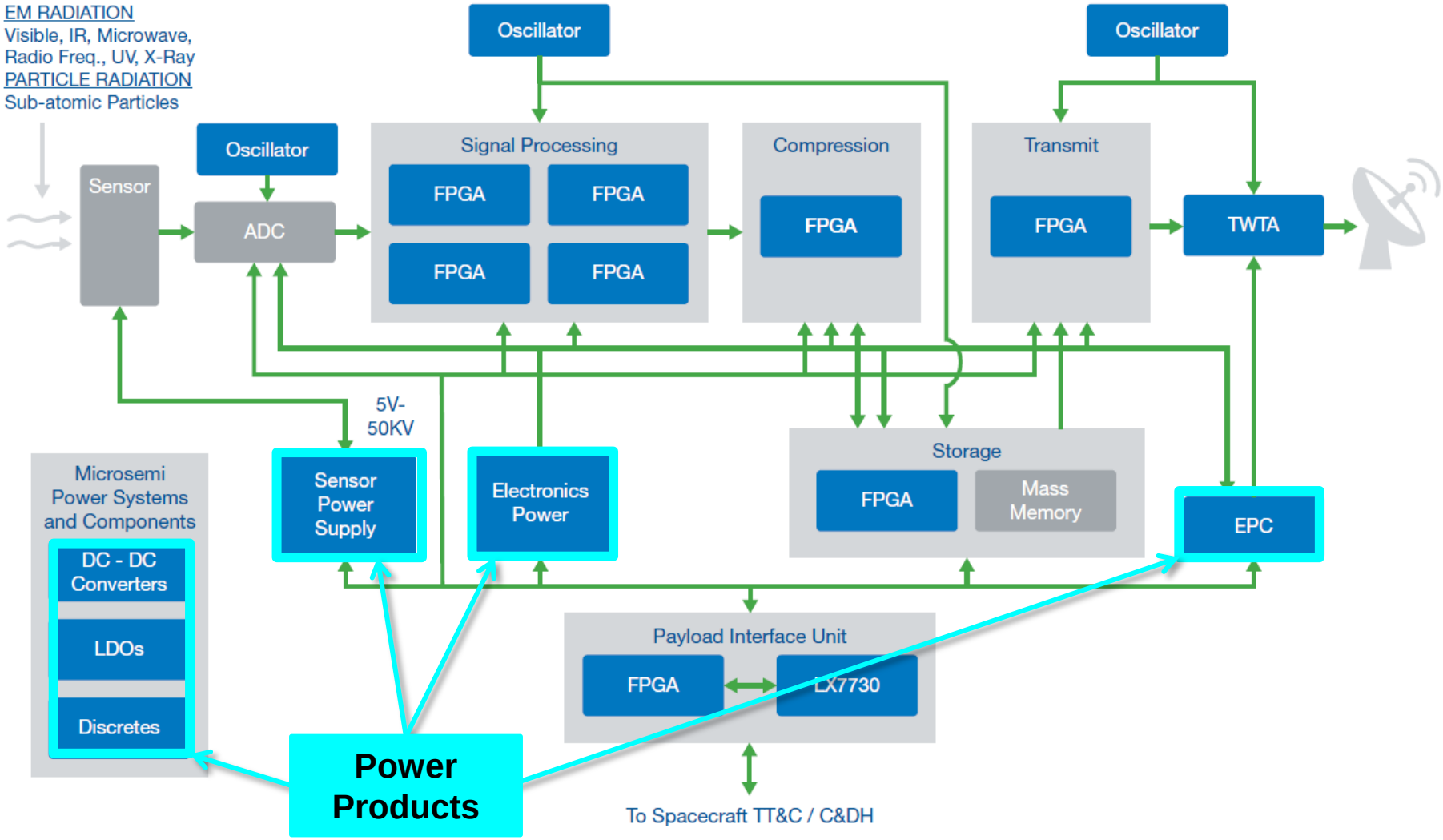
RTG4 complements other Microsemi space products

Space System Managers in Remote Sensing Payload



RTG4 complements other Microsemi space products

Power Products in Remote Sensing Payload

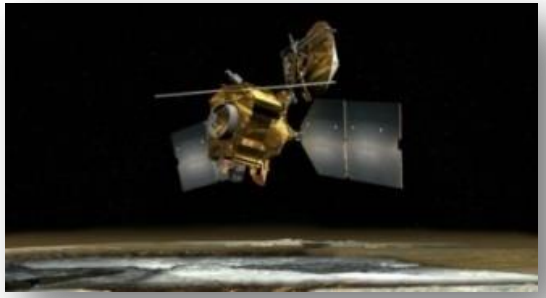


RTG4 complements other Microsemi space products

Microsemi FPGA Space Heritage

- Microsemi Space
  - Broad space portfolio since 1957
  - First FPGAs screened for space in 1992
  - First FPGAs with radiation hardening by process in 1996
  - First FPGAs with radiation hardening by design in 2001

RTSX-SU
(Introduced 2004)



Mars Reconnaissance Orbiter
RTSX-SU on board (2005)

RTAX-S/SL/DSP
(Introduced 2005)

Curiosity (Mars Science Lab)
RTAX on board (2011)

RT ProASIC3
(Introduced 2008)

NASA IRIS
RT ProASIC3 on board (2013)

Product Lifetime and Export Control

- Current RT FPGA products – RTAX, RTSX, RT ProASIC3
  - Recent investments in QML qualification of class V and EV-flow
  - Plan to maintain supply (No End Of Life) for *at least 10 years*

- Update on export control
  - RT FPGAs are no longer controlled under ITAR
  - Export Administration Regulations now apply
    - Managed by U.S. Dept of Commerce
    - All exports require End Use Statement (EUS)
    - An export license may or may not be required
      - Depends on end use and destination country,
  - New Export Control Classification Numbers (ECCNs)
    - RTSX-SU 3A001.a.2.c.
    - RTAX-S/SL/DSP 9A515.e
    - RT ProASIC3 3A001.a.2.c.
    - RTG4 9A515.e

Conclusion

RTG4 High-Speed RT FPGAs

- High-bandwidth signal and data processing in radiation applications
- Flexible and reliable alternative to ASICs
- Immune to radiation-induced configuration upsets
- Radiation enhancements suitable for earth orbits and deep space

Solving Signal Processing Congestion in Space Systems

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Thank You

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