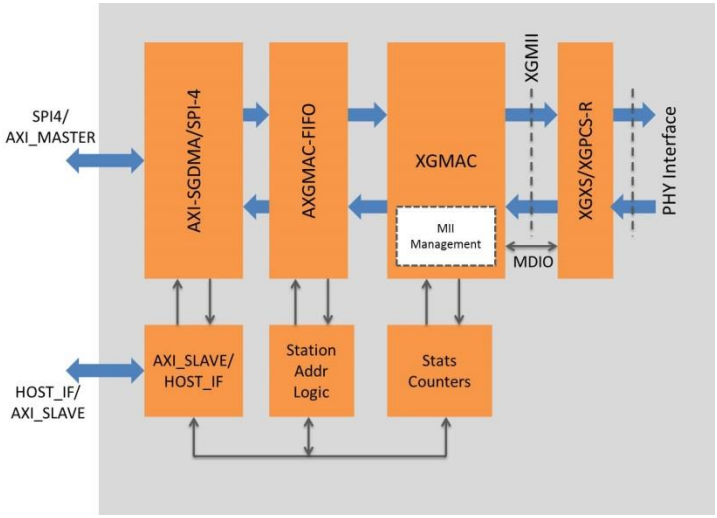
10G Ethernet Solution

Overview

The SI-XGMAC provides 10Gbps Ethernet Media Access Controller (MAC) with a XGMII (10 Gigabit Media Independent Interface) for incorporation in a customer's ASIC design. The inclusion of a XGMII means that several alternative PHY interfaces are readily supported, including XSBI (10 Gigabit Sixteen Bit Interface) and XAUI.

The MAC core along with FIFO-core and SPI4/AXI-DMA engines provides a complete solution for easy integration in Ethernet based applications. Optional core logic includes Statistics counters and destination address based frame filtering. There are many different possible applications for the SI-XGMAC, including network interface designs, Ethernet switching designs, and test equipment designs



Features

Ethernet XGMAC Core

- IEEE 802.3ae compliant MAC
- Supports IEEE 802.3x Full Duplex flow control
- Supports 802.3ae XGMII Interface
- Programmable Drop Receive frame filter with hash filtering
- Supports transmission and reception of odd-byte-size transfers.
- 33 Statistics counters supporting RMON and Ether-Stats applications
- SCAN insertion-friendly design for ASIC implementations.
- Programmable padding for minimum frame size
- Programmable VLAN aware padding
- Programmable VLAN ignore padding
- Programmable FCS insertion
- Separate external pipeline and configuration register reset signals
- Internal software-accessible module-specific resets
- Synchronous or asynchronous configuration register access
- Packet-aware real-time sub-module enabling and disabling
- Short pause mode on XOFF pause frame reception for test use
- CPU interface-forced XOFF pause frame transmission for test use
- Programmable valid length field checking
- IPG dithering for XGMII alignment and average minimum IPG maintenance
- Programmable MAC Station address
- Separate transmit and receive configurable maximum frame truncation values
- Programmable MII Management MDIO preamble suppression
- MII Management hardware polling on MMD status register
- MII Management hardware polling on MMD status register over multiple ports
- Programmable MII Management MDC frequency selection
- MII Management support of indirect addressing
- XGMII local and remote link fault detection
- XGMII local and remote link fault automatic or assisted generation
- SPI-4 Compatible interface supporting full XGMAC pipe and 10Gbps data rate
- Programmable depth receive/transmit FIFO buffer

Ethernet MAC-FIFO Core *(Optional add on DIP)*

- User-definable storage sizes

- Clock-frequency-independent I/O Ports
- Single- or multiple-word I/O data transfers
- Programmable high and low receive storage level indicators
- Automatic pause frame handshaking circuitry
- Programmable pause frame handshaking reassertion interval
- Programmable high transmit storage level indicator
- Graceful receive memory-full frame drop
- Graceful enable and disable
- Programmable transmit frame or word cut-through threshold
- Transmit storage underrun indication
- Full memory utilization
- Optional per-transmit-frame MAC configuration data
- Synchronous dual-port memories

Address Based Frame Filtering (Optional add on DIP)

- 128 bit hash table filtering
- Unicast Frame Filtering
- Multicast Frame Filtering

Back-end side SPI4/AXI interface *(Optional add on DIP)*

- AMBA AXI compliant Master ports for payload data transfer
- AMBA AXI compliant Slave port for core configuration
- Dual channel scatter gather DMA with linked list descriptor handling with interrupt coalescing support.
- IEEE Standard SPI-4 Interface.

Statistics Counters Core *(Optional add on DIP)*

- Total of 33 separate counters are implemented to count/accumulate conditions that occur as packets are transmitted and received
- Support RMON MIB group 1, RMON MIB group 2 if table counters, RMON MIB group 3, RMON MIB group 9, RMON MIB 2, and the dot 3 Ethernet MIB

10G Base-R PCS - XSBI PHY Interface *(Optional add on DIP)*

- Implements IEEE 802.3ae Clause 49: 10G full duplex PCS
- XGMII interface to MAC devices: 32bit DDR or 64bit SDR
- XSBI interface to PMA SerDes devices: 16-bit source synchronous interface at 644.53MHz
- Rate adaptation between the XGMII clocks and XSBI clocks
- 64B/66B block encoding/decoding
- Scrambling/de-scrambling
- PRBS31 test pattern generation/checking and BER checking
- Supports loopback
- Supports MDIO interface

XAUI-XGMII Extender *(Optional add on DIP)*

- IEEE 802.3ae- clause 45 MDIO interface
- IEEE 802.3ae- clause 48 state machines
- Pseudorandom idle insertion (PRBS Polynomial X7 + X3 + 1)
- Single-width Double Data Rate (DDR) or double-width Single Data Rate (SDR) XGMII interface
- Optional comma alignment function
- Low power mode
- PHY-XS and DTE-XS loopback
- IEEE 802.3ae- annex 48A jitter test pattern support
- IEEE 802.3 clause 36 8B/10B encoding compliance
- Tolerance of lane skew up to 16ns (50 UI)
- IEEE 802.3 PICs Compliance Matrix

Related products

- XAUI-XGMII Extender Design IP
- 10G Base-R PCS Design IP
- Verification IP for Ethernet 10Mbps to 400G Ethernet MAC with various PHY interfaces

For pricing, evaluation and additional information contact sales@sibridgetech.com