SPACE BRIEF

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Microsemi

From The Editors

Hello and welcome to this first edition of Microsemi's Space Newsletter. Our goal is to provide you with a round-up of the most recent news relating to Microsemi's space-flight FPGAs, and to give you some extra visibility of what we're working on.

Articles in this edition:

- **Updates on the qualification and reliability status of the two newest additions to the line-up of Microsemi space-flight FPGAs, RTAX-DSP and RT ProASIC3**
- **Latest developments in our selection of Intellectual Property (IP) cores**
- **Development tool update**

Industry's First Flash FPGAs for Space now Qualified

RT ProASIC3 completes Mil Std 883 Class B qualification

Providing designers of space systems with reprogrammability, single-chip form factor, and a complete absence of configuration upsets, RT ProASIC3 presents a unique combination of features and benefits. The reprogrammability provided by its 130nm Flash - based interconnect resources allows for easy and rapid prototyping, and also allows reprogramming of flight hardware without the need to disassemble the hardware or to remove the part from the flight board. This can save significant amounts of time and budget if late-breaking design changes occur. In fact it is possible to defer the final hardware design until after integration has been completed, allowing development teams extra time to enhance and refine signal-processing algorithms and control logic. The technique of assembling flight hardware with an unprogrammed FPGA can also be used to provide rapid customization of hardware that is already assembled, integrated and tested. Further, careful planning at the design stage can result in the

Industry-Standard Space FPGAs Just Got A Lot Bigger!

RTAX-DSP Has Enhanced Signal Processing Capabilities, Improved Radiation Performance

With up to 120 embedded multiply-accumulate blocks, the new RTAX-DSP parts can integrate complex DSP designs which previously would have consumed multiple RTAX-S/SL parts. The area-efficient Mathblocks which implement multiply-accumulate functions in the RTAX-DSP family are uniquely protected against radiation single-event effects in space. Further, the programmable logic gates have also been upgraded to provide a higher level of protection against single event transients (SETs) than the RTAX-S/SL family.

The RTAX-DSP family has now completed its Mil-Std 883 Class B qualification and flight units may now be ordered. Flight units are available with screening levels from Mil-Std 883 Class B to "EV" flow, which is fully compliant with the QML Class V screening flow. Prototype units, featuring reduced testing to minimize cost, are also available for non-flight purposes. Having met the requirement for Mil Std 883 class B qualification, the RTAX-DSP qualification units are going through further qualification tests, with the ultimate goal of achieving a full QML Class V certification for the product family.

The RTAX-DSP family uses the same tried-and-trusted architecture, wafer fabrication process, and programming technology as the industry-standard RTAX-S/SL family. Because of this, the reliability of RTAX-DSP is expected to be identical to the RTAX-S/SL parts.

Find out more:
http://www.actel.com/products/milaero/rtaxdsp/default.aspx

New IP Leverages On-Chip Mathblocks

Microsemi IP servicing high reliability and space applications have seen several new releases recently

possibility of reprogramming the FPGA on orbit to extend or enhance the mission of the spacecraft after it has been launched. The Flash cells used in the 130nm RT ProASIC3 FPGAs are different to the Flash cells that are used in commercial bulk memories. Their larger size gives them immunity to state changes due to heavy ion radiation. Such state changes in the configuration SRAM cells of SRAM-based FPGAs are the reason they require cumbersome and expensive triple-chip redundancy something Microsemi's Flash and antifuse FPGAs do not require.

RT ProASIC3 has recently completed its Mil-Std 883 Class B qualification, and all RT ProASIC 3 flight units are screened in compliance with Mil-Std 883Class B, so designers can feel secure that they are flying parts which have been stringently screened to the extent necessary for space flight.

Find out more:
http://www.actel.com/products/milaero/rtpa3/default.aspx

Enhanced Libero Tool Set

Recent updates and enhancements to the Libero IDE tool set supporting Microsemi FPGAs for space include an enhancement in Libero 9.1 to improve performance and utilization of designs targeting RTAX-DSP parts. Released in January 2011, Libero 9.1 includes an updated version of Synplify Pro which provides inference support to the cascade-chain and multiply-accumulate features of the 18x18 Mathblocks in the RTAX-DSP devices. This improvement is achieved from cascade chain inference support, which utilizes the hard-wired cascade option in the Mathblocks. Additionally, multiply-accumulate inference support utilizes the internal dedicated feedback loops inside the Mathblocks.

Microsemi has recently released an update to the Silicon Sculptor software which improves the post-programming test performed on RTAX FPGAs during the programming process.

Find out more:
http://www.actel.com/documents/PCN1019_Addendum.pdf

Microsemi Space Forum

Proceedings from the most recent Space Forum events, held in Los Angeles (December 2, 2010), Noordwijk (April 5,2011) and Moscow (April 7, 2011) are now posted on the Microsemi SOC Group web site at
http://www.actel.com/asf/postconference/welcome.aspx

The next events will take place in Bangalore and Ahmedabad, India, in July 2011.

leveraging the on-chip Mathblocks in Microsemi's RTAX-DSP devices.

In May 2010 CoreFFT v4.0 was released, implementing a Radix-2 Fast Fourier Transform filter generator. CoreFFT v4.0 enables custom user-configurable filter generation with selectable Forward and Inverse Complex FFT implementation, transform sizes from 32 to 8,192 points, 8 to 32 bits i/o real and imaginary data and twiddle coefficients, two's complement input/output data, bit-reversed or natural output order, and user selection of unconditional or conditional block floating point scaling. As FFTs are commonly used to process data bursts with gaps between the bursts, there is no need to maintain extensive memory buffering, and CoreFFT v4.0 allows configuration using a minimal buffering FFT mode to reduce the size of the generated RTL.

In March 2011 CoreFIR v7.0 was released, updating Microsemi's highly parameterizable, area-efficient, high performance multiplier-accumulator (MAC) Finite Impulse Response filter IP core. CoreFIR v7.0 implements a wide range of filter types including a single rate fully enumerated (parallel) filter, a single rate folded (semi-parallel) filter, a multi-rate interpolation filter and a multi-rate decimation filter. These MAC FIR filters compute their sum-of-products output using as many physical MACs as filter taps, providing the fastest input sample rate. CoreFIR v7.0 supports three filter coefficient modes - constant coefficients, multiple constant coefficient sets, and runtime reloadable coefficients. CoreFIR v7.0 supports configurable generation with 2 to 2^N taps (where N is the number of math blocks on the RTAX-DSP device selected, up to 1024 taps), 2 to 18 bits signed or unsigned input data precision, 2 to 18 bits signed or unsigned coefficient precision, full precision output, and coefficient symmetry optimization.

Both CoreFFT v4.0 and CoreFIR v7.0 are available now. For more information on any of the extensive portfolio of spaceflight proven Microsemi IP cores, visit the Microsemi website or contact your local Microsemi or distribution partner sales office.

Find out more:
http://www.actel.com/products/ip/search/detail.aspx?id=624
http://www.actel.com/products/ip/search/detail.aspx?id=618

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