ZL70251 Programmer User's Guide

Microsemi

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1 – Introduction

The ZL70251 Programmer User's Guide contains a comprehensive list of typical and required programming procedures for the various modes of operation and required calibrations of the ZL70251 Ultra-Low-Power Sub-GHz RF Transceiver. Complementing these procedures is a complete memory map defining all of the application registers, with detailed descriptions of their bit definitions including reset values and register access types.

For programming examples, example source code written in C is available to all users who complete a Source Code License Agreement (SCLA) with Microsemi. This source code provides proven examples of all procedures in this user's guide and therefore significantly reduces the development time for users. This source code runs on the ZL70251 Application Development Kit (ADK) boards, which is also available and recommended for users. The ZL70251 ADK provides users with a platform to observe the behavior of the procedures in a lab environment. The ZL70251 ADK also provides an example circuit, allowing users to evaluate the RF performance of the device. Please go to www.microsemi.com/cmpg for more information.

2 – Power-Up Initialization

2.1 General Initialization

After power-up, it is assumed that the external controller holds the ZL70251 chip in reset by driving the RESET_B pin low.

- All the registers are in their reset state when RESET_B is low (active low).
- When the reset is released (RESET_B goes high) all the registers stay in reset (except for the two bits *osc_en* and *clk_out_en*, which are in the CLK_ENS register, as stated below). The external controller has to send write commands to the ZL70251 chip through the control interface in order to enable its different blocks and functions.

The three internal signals *osc_en*, *sys_clk_en*, and *clk_out_en* are unique in that they are clocked by the SCL pin, whereas all other registers are clocked by the system clock (sys_clk). This provides limited control interface access when the system clock is not running while in the ultra-low-power state. Those three signals are used to enter and exit the different SLEEP states of the ZL70251 chip:

- The *osc_en* output signal controls the XTAL oscillator block:
  - During reset (where RESET_B is low), *osc_en* is low (disabled).
  - When RESET_B input signal goes high, *osc_en* goes high, too. That starts the XTAL oscillator block. This signal is then register controlled by writing to the CLK_ENS register.
- The *clk_out_en* output signal controls the frequency divider that generates the external clock CLK_OUT (for clocking external controller; optional):
  - During reset (where RESET_B is low), *clk_out_en* is low (disabled).
  - When RESET_B input signal goes high, *clk_out_en* goes high, too, generating the CLK_OUT signal to the external controller. This signal is then register controlled by writing to the CLK_ENS register.
- The *sys_clk_en* output signal controls the frequency divider that generates the system clock sys_clk (the default is the crystal frequency divided by 22) going to the ZL70251 MAC:
  - During reset (where RESET_B is low), *sys_clk_en* is low (disabled).
  - When RESET_B input signal goes high, *sys_clk_en* stays low. The frequency divider that generates the sys_clk stays disabled, keeping the system clock sys_clk that goes to the ZL70251 MAC inactive in order to save power. This signal is then register controlled by writing to the CLK_ENS register.

Note: When RESET_B signal goes high, the XTAL oscillator block starts. Its start-up time of about 5ms has to be taken into account before writing to the *sys_clk_en* bit that activates the ZL70251 MAC system clock sys_clk.

Recommended Initial Register Settings

The section "10 – System Memory Map" on page 60 summarizes the memory map of the ZL70251.

Recommended initial register settings are provided in the "Recommended Values" column of Table 10-1 on page 62. Write the recommended values to the appropriate registers after every chip reset (RESET_B pin low).

2.2 Using the Lower Data Rate (136.5kbit/s, 200-kHz channels)

The ZL70251 operational frequency range extends down to 779MHz. This lower range is intended to allow operation in the Chinese ISM band at 779–787MHz. The occupied bandwidth (OBW) allowed in this band is 200kHz, thus requiring a lower data rate.

Setup for the lower frequency band is largely the same as in other bands. The differences are listed below. Trimming and tuning must be performed after the setup.

- Set the SYS_CLK_DIV register value to 0x1E (decimal 30). This reduces the bit rate to approximately 136.5kHz for 200-kHz channels. Note that the modulation DAC must be trimmed for the desired modulation index (0.5), and the mod_phase_cnt value must be programmed for the modulation index chosen (24).
- Select an in-band channel frequency from those in the A and M value calculation spreadsheet (***ZL70251 Synthesizer Programming Table.xls***).
- Write the M value that was selected from the A and M value calculation spreadsheet to the SYNTH_CH_MDIV register. Note that the M value must be written before the A value.
- Write to SYNTH_CH_ADIV[7:0], where:
  - Bit [7] (*ch_lo_ctl*) determines whether to use high- or low-side LO injection. (The default is for low-side injection. If high-side injection is selected, the RX data must be inverted by setting the *rx_polarity_inv* bit in MAC_CTL2 to 1.)
  - Bit [6] (*vco_low_range*) is set to 1.
  - Bits [5:0] (*ch_a_div*) comprise the A value selected from the A and M value calculation spreadsheet.

  Writing to this register initiates the transfer of both the A value and the M value to the synthesizer.
- The input to the ZL70251's SCL pin, which is provided by the external controller via the ZL70251's control interface, must be at a baud rate less than or equal to 270kHz.

3 – Clock Generator

3.1 Default Clock Frequencies

With a 24.576-MHz crystal, when the clocks are enabled they run at the following frequencies by default:

- CLK_OUT = 24.576 MHz / 24 = 1.024 MHz
- PLL clock = 24.576 MHz / 81 = 303.4 kHz
- sys_clk = 24.576 / 22 = 1.117 MHz
- bit period = sys_clk / 6 = 186.167 kHz

3.2 Maximum and Minimum Divide Count Values

CLK_OUT_DIV can be changed within the range mentioned in Table 3-1. The resulting range for CLK_OUT is shown in Table 3-2.

***Table 3-1* • Minimum, Typical, and Maximum Values for Programmable Counter**

Register [bits]	Minimum	Typical	Maximum
CLK_OUT_DIV[4:0] (*clk_out_div*)	4	24	30

***Table 3-2* • CLK_OUT Frequency Range**

	Minimum div: 4	Typical div: 24	Maximum div: 30
24.576-MHz XTAL	6.144 MHz	1.024 MHz	819.2 kHz

Note: ***Warning***: For proper operation, SYS_CLK_DIV must not be changed from its default value (typical value), unless operating in the 200-kHz occupied bandwidth, in which case the recommended initialization value in "2.2 Using the Lower Data Rate (136.5 kbit/s, 200-kHz channels)" on page 10 should be used.

4 – Synthesizer Controller

4.1 A and M Value Calculation

The A and M registers must be programmed any time a different channel is desired.

The A value can be programmed through the system bus using *ch_a_div* in the SYNTH_CH_ADIV register.

The M value can be programmed through the system bus using SYNTH_CH_MDIV.

Note: The M value must be written before the A value.

LO control (high/low) can be programmed through the system bus using *ch_lo_ctl* in the SYNTH_CH_ADIV register.

A and M requirements

$A \geq 5, M \geq 16$ *EQ 4-1*

A and M calculation

The total number of PLL clock periods to be produced by the VCO in order to run through the PLL divide cycle is given by N_{tot}:

$N_{tot} = \text{int}(\text{carrier frequency} / \text{PLL clock})$ *EQ 4-2*

In the ZL70251 PLL implementation, the relation between N_{tot} and A and M is given by EQ 4-3 below:

$N_{tot} = 17 \times A + 16 \times M$ *EQ 4-3*

EQ 4-3 shows that A is the number of times the prescaler needs to count to 17 and M is the number of times the prescaler needs to count to 16.

$A = ((N_{tot} - 5) \bmod 16) + 5$ *EQ 4-4*

where: $4 < A < 21$

$M = (N_{tot} - A \times 17) / 16$ *EQ 4-5*

where: $139 < M < 193$ for 300-kHz channel spacing and
$220 < M < 295$ for 200-kHz channel spacing

EQ 4-2, EQ 4-4, and EQ 4-5 can be used for calculating A and M values to program registers SYNTH_CH_ADIV and SYNTH_CH_MDIV.

The ***ZL70251 Synthesizer Programming Table.xls*** spreadsheet implements the above formulas and can also be used to generate the A and M values for a particular target frequency or as a look-up table for all the synthesizable frequencies within the ZL70251 range.

A and M Programming Example

1. Determine the output frequency for the current channel being programmed. N_{tot} represents the number of counts that corresponds to the output frequency. From the table, look up the values for A and M. A is the number of times the prescaler divides by 17 and M is the number of times the prescaler divides by 16.
2. If a frequency of 915.985MHz is desired, this would equate to an N_{tot} value of 3019.
3. If N_{tot} of 3019 is chosen, the values in EQ 4-3 are $17 \times 11 + 16 \times 177 = 3019$, that is:
   – A is 11, with a binary representation of 6’b001011.
   – M is 177, with a binary representation of 8’b10110001.
4. For this example, *vco_low_range* remains at 0. If channels below 795MHz are being used, then program the *vco_low_range* bit in the SYNTH_CH_ADIV register to 1. Programming a 1 shifts the VCO trim range so that the PLL can take the VCO down to 779MHz. If this bit is set to 1 for low range, *kvco_ctl* in the RF_CTL7 register should be set to 0.
5. Program *ch_m_div* bits equal to 8’b10110001 (0xB1) in the SYNTH_CH_MDIV register.
6. Program SYNTH_CH_ADIV equal to 8’b00001011 (0x0B).

5 – Interrupt Controller

5.1 Interrupt Description

There is only one interrupt pin at the top level of the ZL70251 chip called IRQ, and the interrupt sources are determined by writing to the enable registers IRQ_EN1 and IRQ_EN2. More than one interrupt source per register can be enabled. In this case, when the IRQ pin is set high, it is necessary to read the interrupt registers IRQ1 and IRQ2 (with a control interface read command) to determine what the source(s) is.

When the corresponding interrupts are enabled, the outputs of the interrupt registers IRQ1 and IRQ2 create an interrupt on the IRQ pin (level high). If an interrupt is not enabled, the interrupt pulse in the interrupt registers IRQ1 and IRQ2 can still be latched but that does not generate an interrupt on the IRQ pin.

If an interrupt is enabled and it is set, the IRQ pin is set high until it is lowered either by reading the respective interrupt register or by writing to the appropriate enable register to disable the interrupt.

The RF_STAT returns the status as defined in the memory map when it is read, but a status can never generate an interrupt on the IRQ pin.

Registers IRQ1, IRQ2, and RF_STAT are read-only and registers IRQ1 and IRQ2 are clear-on-read (CoR). See Table 5-1 for a list of the individual ZL70251 interrupts.

***Table 5-1* • ZL70251 Interrupt Register Bit Definitions**

Register	Bit	Bit Definition	Description	Reset Value
IRQ1	7	–	<Reserved>	0
	6	sync_detect_irq	Synchronization detect interrupt	0
	5	trim_done_irq	Trim done interrupt	0
	4	trim_fail_irq	Trimming and tuning process failed interrupt	0
	3	adc_done_irq	ADC done interrupt	0
	2	rssi_nosig_irq	RSSI-RX no signal interrupt	0
	1	rssi_thresh_irq	Threshold interrupt for the RSSI output (rx_rssi)	0
	0	–	<Reserved>	0
IRQ2	7:4	–	<Reserved>	0000
	3	rx_done_irq	Receive complete interrupt	0
	2	tx_done_irq	Transmit complete interrupt	0
	1	pll_lock_err_irq	PLL error (not locked) at startup of TX/RX interrupt	0
	0	sync_err_irq	No synchronization pattern found during receive period interrupt	0

6 – Calibrations

6.1 Calibration[1] Summary

Registers (or parameters) that control analog circuit operation may be categorized into three classes:

- Preset: Registers whose values are defined during IC evaluation and are set to a constant value (ideally the default value). No calibration is required for such parameters. These registers are supplied for design flexibility and to reduce risk.
- Factory: Registers whose values must be determined in production calibration procedures requiring special equipment. These registers relate to parameters that may vary from device to device due to process variations, operation range selections, or external component values.
- Operation: Registers whose values must be determined in production and/or by operational calibration procedures executed by the chip independent of external equipment. These registers relate to parameters that may vary from device to device due to process variations, operation range selections, or external component values.

Parameters are typically stored in external nonvolatile memory and loaded into the transceiver after a reset. Disabling a block through the control interface (where en is 0) does not reset the registers holding the trim values or other parameters.

ZL70251 does not perform any trimming or tuning at power-up or at any other time without being commanded to do so over the control interface.

The calibration sequence should be executed in the order provided in Table 6-1 on page 15. Some of the trims can be omitted when conducting tests that do not involve a given block, but care should be taken because some seemingly unrelated blocks actually depend on each other. The crystal oscillator need not be trimmed for tests that do not involve transmitting, receiving, or clock frequencies. The current reference should always be trimmed first before any other trim. The safest approach is to follow the detailed procedures in the paragraphs that follow Table 6-1 on page 15. Only one of the calibrations at a time can be performed by the application software.

1. *The terms calibration, tuning, and trimming are used interchangeably throughout this document.*

***Table 6-1* • Trim and Tune Summary**

Order	Parameter Name	P (Preset) F (Factory) O (Operating)	Force and Sense Requirements	Notes
1	Current reference	O	None. Internal calibration.	
2	Crystal oscillator frequency	F	Frequency counter.	
3	SAR VCO frequency TXPAOFF mode and VCO amplitude	O	None. Internal calibration.	1
4	VCO frequency TXPAON mode (with increment/decrement tuning of the VCO frequency using internal counter providing adjustment pulse)	O	None. Internal calibration.	1
5	SAR VCO frequency RX mode	O	None. Internal calibration.	1
6	Peak detector offset	O	None. Internal calibration.	1
7	Antenna (with increment/decrement tuning of the VCO frequency using internal counter providing adjustment pulse and in the TXPAON mode)	O	None. Internal calibration.	2
8	LNA load	O	None. Internal calibration.	2
9	IF filter, FM detector, and Gaussian filter	O	None. Internal calibration.	
10	FSK frequency separation	F	A spectrum analyzer is needed.	
11	Transmitter output power	P, F	Calibrated antenna and power meter.	3
12	Enable automatic trimming of the VCO	O	None.	
13	LNA gain	P	None, based on application requirements.	3

Notes:

1. *It is recommended that these calibrations be performed anytime there is a frequency change.*
2. *Whenever the frequency changes, it may be necessary to run these calibrations to maintain optimum performance. It is recommended that this be determined during product characterization. These tests require that the TX and RX pins be connected together. Note that the antenna tune capacitors are only on the RX pins and that the LNA load tune requires a transmitted signal to be fed back to the receiver.*
3. *Preset trim values are determined during product characterization and should be the same for all devices.*

6.2 Tune and Trim Sequence

The calibration sequence should be executed in the order provided in Table 6-1 on page 15 and in the following paragraphs. At the end of most tune or trim procedures, the *trim_done_irq* interrupt is set. The IRQ1 register should then be read to see if the *trim_fail_irq* status bit is set. The IRQ1 register is cleared on the read operation.

Note: ***IMPORTANT***: In order to optimize the tune and trim procedure on the ZL70251 chip at the factory or after every power-up, the tune and trim sequence described in the following paragraphs assumes that the steps are performed in a contiguous manner. If a tune or trim has to be run independently, the settings performed before this particular tune or trim have to be taken into account.

6.3 Tune and Trim Setup

The tune and trim sequence can start only after setting up the basic functionality of the ZL70251 chip both at the factory and at power-up. Refer to Table 6-2.

Table 6-2 • **Procedure for Tune and Trim Setup**

1. Turn on the power supply.	
2. Raise the reset.	
3. Wait 5ms.	Wait for the crystal oscillator start-up time.
4. Write CLK_ENS[2]=1.	This sets the *sys_clk_en* bit to enable the frequency divider that generates the sys_clk going to the MAC.
5. Write IRQ_EN1[5]=1.	This enables the *trim_done_irq* interrupt.

6.4 Current Reference Trim

It is very important to trim the current reference before any other trimming or tuning because the current reference supplies current to almost all the analog circuits on the chip. If the reference is untrimmed then the other trims are not valid.

The ZL70251 uses an external resistor of 2% or better accuracy to set its internal current reference. The node attached to the external resistor is sensitive to noise that can be picked up by the exposed pin and trace runs. For this reason, internal resistors are used in the current reference and other reference circuits. Before they can be used, however, an internal resistor of the same type and value is compared with the external resistor and trimmed to match.

The current reference trimming procedure is described in Table 6-3. It assumes that the procedure in "6.3 Tune and Trim Setup" has already been completed.

Table 6-3 • **Procedure for Current Reference Trim**

1. Perform the following setup through the control interface:	
i. Write AUTO_TRIM_EN=0x01.	Setting the *iref_en_trim* bit launches the IREF trimming procedure. The AUTO_TRIM_EN register is cleared internally once the trim procedure is done.
2. Now that the automatic IREF trimming procedure is launched:	
i. Wait for the *trim_done_irq*.	Indicates that the trim has completed. The trim typically takes less than 700µs.
3. At the end of the IREF trimming procedure:	
i. Read IRQ1.	Read the IRQ1 register to clear interrupt(s) and ensure that the trim did not fail.

6.5 Crystal Oscillator Tune

The purpose of the crystal oscillator tuning is to improve the absolute accuracy of the system reference frequency. This tuning is done once during factory calibration.

Note: **IMPORTANT**: The crystal oscillator tuning depends on the selection of the crystal and the loading that is placed on the crystal pins. In order to save power, the crystal oscillator presents a 3-pF load instead of the typical 8-pF or 10-pF load. A slight frequency pull, on the order of 100 to 150 PPM, would result if using a standard crystal without additional external load capacitors. Such a deviation has no effect on the operation of the device and is generally not a problem for most applications, providing all ZL70251s have the same frequency pull (within trimmable range). If the deviation is not acceptable and power is critical, a special cut crystal may be used (that is, slightly slower to compensate for the pull). The crystal used on the BASE251 and REMOTE251 in the ZL70251 ADK (or equivalent) is recommended (Fox P/N 617-24.572675-1; call for specifications). Alternatively, if power is not as critical, external capacitors can be added, as shown in Figure 6-1, to bring the total load capacitance to the crystal load specification. For instance, for a crystal with an 8-pF load specification (C_L), C_{Lext} = 8 pF − 3 pF = 5 pF, so two 10-pF capacitors need to be added, one on each end of the crystal. It must be noted, however, that this results in a reduced trim range. The frequency tolerance should therefore be tighter to compensate.The ***ZL70251 Synthesizer Programming Table.xls*** spreadsheet can be used to determine the VCO frequency. The crystal frequency is the frequency on the CLK_OUT pin multiplied by 24 if using 300-kHz channel spacing or by 32 if using 200-kHz channel spacing. From there you can calculate the PPM pull of the crystal frequency, which can then be entered into the spreadsheet to determine the resulting VCO frequency. Also, as long as the transmitter and receiver devices are trimmed to match crystal frequencies, no degradation in system performance is noticeable.

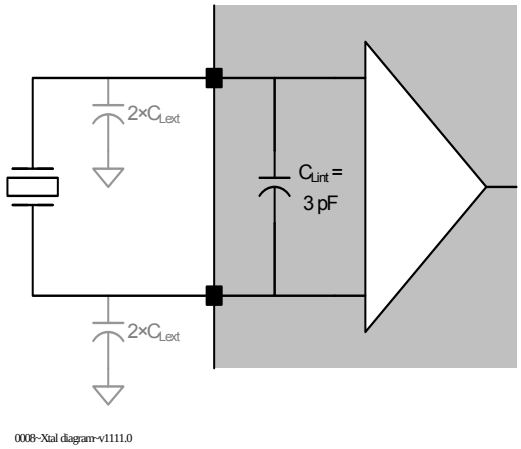


Figure 6-1 **• Crystal Oscillator with Optional Additional External Load Capacitors**

The crystal oscillator tuning procedure is described in Table 6-4 on page 18.

***Table 6-4* • Procedure for Crystal Oscillator Tune**

1. Calculate desired CLK_OUT frequency (F_{des}) using the equation $F_{des} = F_{xtal} \div CLK\_OUT\_DIV$.	The desired CLK_OUT frequency (F_{des}) is the crystal frequency (F_{xtal}) divided by CLK_OUT_DIV (see "3.1 Default Clock Frequencies" on page 11).
2. Measure actual CLK_OUT frequency (F_{meas}).	Use a frequency counter that has better than 1 PPM accuracy.
3. Compare desired frequency (F_{des}) to measured frequency (F_{meas}). i. If $F_{meas} < F_{des}$, then write XO_TRIM = XO_TRIM − 1. ii. Else: If $F_{meas} > F_{des}$, then write XO_TRIM = XO_TRIM + 1. iii. Else: If $F_{meas} = F_{des}$, then trim is complete.	Change the six-bit control word in the XO_TRIM register until the desired CLK_OUT frequency (F_{des}) is reached.
4. Check whether XO_TRIM is out of range. i. If XO_TRIM = 0x00 or if XO_TRIM = 0x3F, then the trim has failed. ii. Else: Repeat steps 2 and 3.	Repeat steps 2 and 3 until desired CLK_OUT frequency is reached or trim fails.
5. Store XO_TRIM value in nonvolatile memory.	Since the crystal oscillator trim is a factory trim, the trim value has to be stored in nonvolatile memory and loaded into the XO_TRIM register upon power-up of the device.

6.6 VCO Frequency and Amplitude Tuning

The terms "tuning" and "trimming" are used interchangeably in this section. Please read all the sections related to VCO trimming before starting programming.

Trimming the VCO frequency and amplitude keeps the VCO in the proper operating conditions. There are several steps to accomplish this and they should be done in the order shown:

1. Select the frequency band.
2. Perform SAR VCO frequency tuning TXPAOFF mode and VCO amplitude trimming (see "6.6.2 SAR VCO Frequency Tune TXPAOFF Mode and VCO Amplitude Trim" on page 21):
   i. Set the VCO amplitude to maximum.
   ii. Coarsely tune the TXPAOFF mode SAR frequency.
   iii. Trim the VCO amplitude.
   iv. Finely tune the TXPAOFF mode SAR frequency.
3. Perform the TXPAON mode frequency trim (see "6.6.3 VCO Frequency Tune TXPAON Mode" on page 23).
4. Perform the RX mode SAR frequency trim (see "6.6.4 SAR VCO Frequency Tune RX Mode" on page 25).

Detailed descriptions of the trim steps follow this section.

Note: **IMPORTANT**: Periodic retrimming of TXPAOFF and TXPAON modes may be required if the antenna impedance changes or operating conditions change drastically.

Note: **IMPORTANT**: Trim the VCO with the expected antenna in the nominal application condition.

The strategy outlined minimizes the spectral content of the TX signal when the power amplifier is turned on. During normal operation when the ZL70251 device changes from TXPAOFF mode to TXPAON mode, the power amplifier turns on, which changes the capacitive load on the VCO, thus pulling the frequency. The capacitance change is compensated, or cancelled out, by changing the VCO trim caps. This explains the reason for having two trim codes for transmit.

The VCO frequency can be trimmed for every channel and the resulting values stored in a table. When a channel is selected, the appropriate trim values can be written back to the VCO. We recommend doing all of the calibrations upon any change of frequency.

There are two methods for trimming the VCO: the successive approximation method (SAR) and the continuous tune method. The successive approximation method is normally used in a production environment to determine nominal values for the frequencies (channels) that the application will be using. It may also be used in the field to calibrate the VCO when power is first applied to the device. It is important to note that this method sweeps through many frequencies to get to the target frequency. To remain compliant with regulatory standards, the successive approximation method must ***never*** be used with the TX PA on since it would randomly transmit radio interference. It is highly recommended that steps 1–4 above always be followed. Once this calibration is completed, the continuous tuning method is recommended to allow for minor corrections to the VCO frequency that may occur from ambient temperature changes.

- Successive approximation method: The frequency tuning can be accomplished by setting up the synthesizer to generate a VCO frequency at the center of the range and then monitoring the VCO control voltage and changing the tuning capacitors until the VCO control voltage matches a reference voltage. This is done by successive approximation (SAR method) starting with *vco_frq[10]*. This method causes the VCO to jump over wide frequency steps and therefore is not used with the power amplifier turned on.
- Continuous tune method: Frequency tuning can also be done by a continuous tune method, used in the TXPAON section. In this method, the trim value is adjusted up or down by 1, depending on the state of the control voltage comparator. A timer causes this adjustment to occur once every 500µs (a little longer than the PLL settling time). The trim value moves one step at a time to reach the correct spot and then toggles between the two codes that cause the control voltage comparator to change state.

6.6.1 Frequency Band Selection

Before any automatic frequency tuning is initiated, the frequency range must be selected. The combinations of the *vco_low_range*, *vco_frq[13:11]*, and *half_band* bits are manual control bits that define the frequency ranges of operation. An initial, rough range setting for these bits can be found in Table 6-5. IC process variations affect these ranges. The application software must be able to change the range and retrim if a VCO trim value reaches the minimum of 0 or the maximum of 2047.

The first step is to pick the correct frequency range. There are two ranges, a low range and a high range. If you are using the device between 795MHz and 965MHz, set the *vco_low_range* bit to 0. If you are using the device between 779MHz and 795MHz, set the *vco_low_range* bit to 1.

The second step is to pick the frequency band. There are four bits used to select overlapping frequency bands. The second and third columns in Table 6-5 show the band settings. At the tops of these columns are the register names and bit positions in the registers. The frequencies vary with temperature, voltage and process so they are offered as guidance, not guaranteed. Select the band in which your frequency of operation is nearest to the center of the band or a little higher than center.

Table 6-5 **• Typical Frequency Range Selection**

SYNTH_CH_ADIV[6] *vco_low_range*	VCO_CTL[2:0] *vco_frq[13:11]*	RF_CTL7[5] *half_band*	Frequency (MHz)
0	0	1	789.7 – 815.4
0	1	0	800.3 – 827.0
0	1	1	812.6 – 840.5
0	2	0	822.9 – 851.9
0	2	1	836.2 – 866.7
0	3	0	848.4 – 880.2
0	3	1	862.9 – 896.7
0	4	0	860.4 – 893.2
0	4	1	875.8 – 910.7
0	5	0	888.1 – 924.5
0	5	1	905.3 – 943.9
0	6	0	919.3 – 959.6
0	6	1	938.3 – 965.0
1	2	0	779.0 – 793.6
1	2	1	780.8 – 805.6

Note: ***Warning***: Frequency Band Selection for Channels Near the Band Edge

Some difficulties with the trim failing may be encountered when trimming channels that are near the edge of the frequency band. A simple change to the next frequency range is all that is required and can be accomplished by setting the *vco_low_range*, *vco_frq[13:11]*, and *half_band* bits accordingly.

6.6.2 SAR VCO Frequency Tune TXPAOFF Mode and VCO Amplitude Trim

The tuning procedure for the SAR VCO frequency in TXPAOFF mode and for the VCO amplitude trim are described in Table 6-6.

***Table 6-6* • Procedure for SAR VCO Frequency Tune TXPAOFF Mode and VCO Amplitude Trim**

1. Perform the following setup through the control interface:	
i. Write SYNTH_CH_MDIV and SYNTH_CH_ADIV[5:0] per instructions in chapter "4 – Synthesizer Controller" on page 12.	Set the synthesizer A and M values to the operational frequency bank (for more details, refer to chapter "4 – Synthesizer Controller" on page 12).
ii. Write SYNTH_CH_ADIV[6] per Table 6-5 on page 20.	Writing to the *vco_low_range* selects the frequency range. (See "6.6.1 Frequency Band Selection" on page 20.)
iii. Write VCO_CTL[2:0] and RF_CTL7[5] per Table 6-5 on page 20.	Writing to the *vco_frq[13:11]* and *half_band* bits selects the frequency band. (See "6.6.1 Frequency Band Selection" on page 20.)
iv. Write RF_CTL7[2:0]=3'b000.	It is recommended that the *kvco_ctl* bits be set to 0 for automatic selection based on the coarse VCO tune value. See Note 1.
2. Write RF_EN1=0x04.	Setting the *man_pll_en* bit enables the PLL.
3. Write SYNTH_CTL=0x07.	Setting the *tx_mode_en* bit puts the synthesizer in transmit mode.
4. Write MAC_CTL1=0x00.	Clearing the *port_e*n bit performs a synchronous reset of the MAC.
5. Write RF_EN6=0x01.	Setting the *man_pa_en* bit and clearing the *man_pa_tx_en* bit turns on the PA buffer but not the PA.
6. Program the VCO amplitude:	
i. Write VCO_AMP_TRIM=0x3F.	
7. Write AUTO_TRIM_EN=0x02.	Setting the *vco_frq_en_trim* bit launches the automatic SAR VCO frequency tune TXPAOFF mode procedure. The AUTO_TRIM_EN register is cleared internally once the trim procedure is done.

Notes:

1. *Note that kvco_ctl may need to change if the channel frequency is near the edge of the frequency bands in Table 6-5 on page 20. If the selected channel frequency is between 779MHz and 795MHz, set kvco_ctl to 0.*
2. *If the trim_fail_irq status has been set, read the VFT_PAOFF_H and VFT_PAOFF_L registers. If they are at a minimum/maximum value, then adjust the band accordingly. For example, if VFT_PAOFF_H is 0x07 and VFT_PAOFF_L is 0xFF, then the VCO ran out of range during the auto trim and the band edge has to increase by one.*

   If the trim continues to fail, then adjustment may be needed to register VCO_CTL. If the trim resulted in a trim value of 0, then try a lower frequency band. If the trim resulted in a trim value of 2047, try a higher frequency band. See Table 6-5 on page 20 and change vco_frq[13:11] bits in the VCO_CTL register and the half_band bit in the RF_CTL7 register. Sometimes this frequency band change works fine for one of the three VCO frequency trims but results in one or two of the remaining VCO frequency trims being 0 or 2047. It is best to be away from the trim extremes so that the trim value has room to move with temperature. Note that trim movement with temperature is possible if bit incdec_modetrans_en is set in the CONT_TRIM_EN register.

***Table 6-6* • Procedure for SAR VCO Frequency Tune TXPAOFF Mode and VCO Amplitude Trim (continued)**

8. Now that the automatic SAR VCO frequency tuning procedure is launched:	
i. Wait for *trim_done_irq*.	Indicates that the trim has completed. This trim takes approximately 25ms for the 186-kbit/s data rate and 35ms for the 136.5-kbit/s data rate.
9. Write AUTO_TRIM_EN=0x04.	Setting the *vco_amp_en_trim* bit launches the automatic VCO amplitude trimming procedure. The AUTO_TRIM_EN register is cleared internally once the trim procedure is done.
10. Now that the automatic VCO amplitude trimming procedure is launched:	
i. Wait for *trim_done_irq*.	Indicates that the trim has completed. The trim typically takes less than 550µs.
11. At the end of the VCO amplitude trimming procedure:	
i. Read IRQ1.	Read to clear the IRQ1 register and to see whether the *trim_fail_irq* status bit has been set.
ii. If IRQ1[4]=1, then the trim has failed; check the setup.	If the *trim_fail_irq* status has been set by the trimming procedure, the setup may be incorrect.
12. Write AUTO_TRIM_EN=0x02.	Setting the *vco_frq_en_trim* bit launches the automatic SAR VCO frequency tune TXPAOFF mode procedure. The AUTO_TRIM_EN register is cleared internally once the trim procedure is done.
13. Now that the automatic SAR VCO frequency tuning procedure is launched:	
i. Wait for *trim_done_irq*.	Indicates that the trim has completed. This trim takes approximately 25ms for the 186-kbit/s data rate and 35ms for the 136.5-kbit/s data rate.
14. At the end of the procedure to tune the SAR VCO frequency TXPAOFF mode:	
i. Read IRQ1.	Read to clear the IRQ1 register and to see whether the *trim_fail_irq* status bit has been set.
ii. If IRQ1[4]=1, then the trim has failed; see Note 2.	If the *trim_fail_irq* status has been set by the tuning procedure, the trim has failed.
15. Write RF_EN6=0x00.	Clearing the *man_pa_en* bit turns off the manual buffer enable.

Notes:

1. *Note that kvco_ctl may need to change if the channel frequency is near the edge of the frequency bands in Table 6-5 on page 20. If the selected channel frequency is between 779MHz and 795MHz, set kvco_ctl to 0.*
2. *If the trim_fail_irq status has been set, read the VFT_PAOFF_H and VFT_PAOFF_L registers. If they are at a minimum/maximum value, then adjust the band accordingly. For example, if VFT_PAOFF_H is 0x07 and VFT_PAOFF_L is 0xFF, then the VCO ran out of range during the auto trim and the band edge has to increase by one.*

   If the trim continues to fail, then adjustment may be needed to register VCO_CTL. If the trim resulted in a trim value of 0, then try a lower frequency band. If the trim resulted in a trim value of 2047, try a higher frequency band. See Table 6-5 on page 20 and change vco_frq[13:11] bits in the VCO_CTL register and the half_band bit in the RF_CTL7 register. Sometimes this frequency band change works fine for one of the three VCO frequency trims but results in one or two of the remaining VCO frequency trims being 0 or 2047. It is best to be away from the trim extremes so that the trim value has room to move with temperature. Note that trim movement with temperature is possible if bit incdec_modetrans_en is set in the CONT_TRIM_EN register.

6.6.3 VCO Frequency Tune TXPAON Mode

The VCO frequency tuning procedure for TXPAON mode is described in Table 6-7 on page 23.

Note: It is important to note that when performing this procedure, the PA is enabled while the VCO is adjusting for the correct frequency. If the device is connected to an antenna, then the environment around the antenna is subject to emissions. For this reason, this procedure uses the "continuous trim" method, which slowly adjusts the VCO frequency until it reaches the desired frequency. When invoked, the "continuous trim" starts with the trim value stored in VFT_PAON_H and VFT_PAON_L. By initializing these registers (see step 1 in Table 6-7 on page 23) with the results of VFT_PAOFF_H and VFT_PAOFF_L, respectively, the "continuous trim" algorithm fine-tunes the VCO (PAON) within the bandwidth of the desired channel.

***Table 6-7* • Procedure for VCO Frequency Tuning, TXPAON Mode**

1. Initialize VCO frequency tune values: i. Write VFT_PAON_H=VFT_PAOFF_H. ii. Write VFT_PAON_L=VFT_PAOFF_L.	Use the trim values from the procedure to tune VCO frequency in TXPAOFF mode as starting values for the VCO frequency tune in TXPAON mode. This significantly reduces the trim time since these trim values are relatively close and do not result in unwanted emissions.
2. Write VCO_FRQ_CNT=0x8C.	This register controls the interval at which the VCO frequency adjustments are made. It also determines the update rate of the *vco_frq_cmp_out* status bit at RF_STAT[2].
3. Write RF_EN1=0x04.	Enables PLL globally; turns on all blocks related to the PLL.
4. Write RF_EN6=0x03.	Setting the *man_pa_en* and the *man_pa_tx_en* bits turns on the PA buffer and the PA.
5. Write SYNTH_CTL=0x07.	Setting the *tx_mode_en* bit puts the synthesizer in transmit mode.
6. Set a 1024-ms timeout in the processor.	The timeout functions as a fail-safe in case the tune procedure goes to the minimum or maximum trim value. The tuning should take about 500µs times the number of LSB trim steps needed to reach the correct trim code, or a maximum of 1024ms.
7. Write CONT_TRIM_EN[1]=1.	Setting the *incdec_cnt_en* bit enables the increment/decrement tuning of the VCO frequency using an internal counter providing the adjustment pulse. This launches the VCO frequency tune TXPAON mode procedure.

Note:

1. *If the trim_fail_irq bit has been set, then the trim has failed because the trim value has reached 0 (minimum) or 2047 (maximum) value.*

   If the trim_fail_irq status bit has been set by the tuning procedure, then verify that vco_frq[13:11] in the VCO_CTL register and the half_band bit in the RF_CTL7 register have been set correctly (see "6.6.1 Frequency Band Selection" under "6.6 VCO Frequency and Amplitude Tuning" on page 19). If the band is not set correctly or the tuning frequency is on the edge of the band, try going to the next closest band and re-run all VCO trims.

***Table 6-7* • Procedure for VCO Frequency Tuning, TXPAON Mode (continued)**

8. Read RF_STAT.	
i. If RF_STAT[2] has toggled, go to step 9.	Read the RF_STAT register and test bit [2] (*vco_frq_cmp_out*) for a bit toggle, signifying the trim is complete.
ii. Else: If timeout is reached, then read IRQ1[4]: a. If IRQ1[4]=1, then the trim has failed; go to step 9.	If the 1024-ms timeout is reached, read the IRQ1 register to see if the *trim_fail_irq* bit has been set. See Note 1.
9. Write CONT_TRIM_EN[1]=0.	Clearing the *incdec_cnt_en* bit disables the increment/decrement tuning of the VCO frequency using an internal counter providing the adjustment pulse.
10. Write RF_EN1=0x00.	Clearing the *man_xmtr_en* bit disables the power amplifier.
11. Write RF_EN6=0x00.	Clearing the *man_pa_en* and the *man_pa_tx_en* bits turns off the PA buffer and the PA.

Note:

1. *If the trim_fail_irq bit has been set, then the trim has failed because the trim value has reached 0 (minimum) or 2047 (maximum) value.*

   If the trim_fail_irq status bit has been set by the tuning procedure, then verify that vco_frq[13:11] in the VCO_CTL register and the half_band bit in the RF_CTL7 register have been set correctly (see "6.6.1 Frequency Band Selection" under "6.6 VCO Frequency and Amplitude Tuning" on page 19). If the band is not set correctly or the tuning frequency is on the edge of the band, try going to the next closest band and re-run all VCO trims.

6.6.4 SAR VCO Frequency Tune RX Mode

The tuning procedure for the SAR VCO frequency in RX mode is described in Table 6-8.

***Table 6-8* • Procedure for SAR VCO Frequency Tuning, RX Mode**

1. Write RF_EN1=0x02.	Setting the *man_rcvr_en* bit enables the receiver.
2. Write SYNTH_CTL=0x03.	Clearing the *tx_mode_en* bit puts the synthesizer in receive mode.
3. Write AUTO_TRIM_EN=0x02.	Setting the *vco_frq_en_trim* bit launches the automatic SAR VCO frequency tune RX mode procedure. The AUTO_TRIM_EN register is cleared internally once the trim procedure is done.
4. Now that the automatic SAR VCO frequency tune RX mode procedure is launched:	
i. Wait for *trim_done_irq*.	Indicates that the trim has completed. The trim typically takes less than 25ms.
5. At the end of the SAR VCO frequency tune RX mode procedure:	
i. Read IRQ1.	Read to clear the IRQ1 register and to see whether the *trim_fail_irq* status bit has been set.
ii. If IRQ1[4]=1, then the trim has failed; adjust the frequency range.	If the *trim_fail_irq* status has been set by the tuning procedure, it is likely that the frequency range needs to be adjusted up or down by one count. Adjust the range and try again.

6.7 Peak Detector Offset Trim

The trimming procedure for the peak detector offset is described in Table 6-9.

***Table 6-9* • Procedure for Peak Detector Offset Trim**

1. Write RF_EN1=0x04.	Setting the *man_pll_en* bit enables the PLL globally.
2. Write RF_TRIM_CTL=0x00.	For this procedure, the peak detector input range has to be 50 mV, which corresponds to the default value of 0 for the *pd_range* bit.
3. Write RF_EN5=0x82.	Setting both *man_pd_en* and *man_adc_ana_en* enables the peak detector block and the internal ADC analog block.
4. Write ADC_CTL1[7:5]=3'b010.	Programming the *adc_mux_in_sel* bits with this value sets up the ADC digital controller to select the peak detector output as the input to the ADC analog block.
5. Write AUTO_TRIM_EN=0x08.	Setting the *pd_en_trim* bit launches the peak detector offset trimming procedure. The AUTO_TRIM_EN register is cleared internally once the trim procedure is done.
6. Now that the automatic peak detector offset trim procedure is launched:	
i. Wait for *trim_done_irq*.	Indicates that the trim has completed. The trim typically takes less than 3 ms.
7. At the end of the peak detector offset trimming procedure:	
i. Read IRQ1.	Read to clear the IRQ1 register and to see whether the *trim_fail_irq* status bit has been set.
ii. If IRQ1[4]=1, then the trim has failed; check matching network and antenna impedance.	If the *trim_fail_irq* status has been set by the tuning procedure, verify that the matching network is configured properly and the antenna impedance is correct.

6.8 Antenna Tune

Antenna tuning is performed during manufacturing after the device is mated with an antenna, after any channel frequency bank switch, and after any power-up if the trim value is not stored[2]. The purpose of this trim is to select the capacitance, which peaks the antenna resonance at the required frequency. A peak detector in the RF receiver section stores the maximum voltage swing on the receiver input pins. The voltage is measured by the five-bit ADC block. An algorithm for finding the best capacitor value is implemented in the trim algorithms.

The antenna tuning procedure is described in Table 6-10 on page 27.

2. *It is best to store the known good trim value and restore it to the trim register at power-up.*

***Table 6-10* • Procedure for Antenna Tuning**

1. Write RF_TRIM_CTL=0x02.	Setting the set *pd_range* bit changes the peak detector input range to 100mV.
2. Write ADC_CTL1[7:5]=3'b010.	The *adc_mux_in_sel* bits should already have been programmed properly during the previous peak detector offset trim. For this procedure, the peak detector should be the input to the internal ADC.
3. Write LNA_GAIN=0x00.	Sets the lowest internal LNA gain.
4. Write RF_EN5=0x83.	Setting the *man_rf_en*, *man_pd_en*, and *man_adc_ana_en* bits enables the peak detector block, the internal ADC analog block, and the LNA.
5. Write RF_CTL4=0x40.	Sets the power amplifier to the lowest power setting by setting *dac_scale_dwn* equal to 1 and writing 000000 to *pa_pwr_ctl*.
6. Write RF_EN6=0x03.	Setting the *man_pa_en* and *man_pa_tx_en* bits enables the power amplifier.
7. Write RF_CTL2[0]=0.	For this procedure, the modulation should be off, which corresponds to the default value of 0 for bit *man_gaus_mod.*
8. Write VCO_FRQ_CNT=0x2A.	For this procedure, the counter value used for the tuning the VCO frequency should be the default value of approximately 150µs.
9. Write AUTO_TRIM_EN=0x20.	Setting the *ant_en_trim* bit launches the antenna tune procedure. The AUTO_TRIM_EN register is cleared internally once the trim procedure is done.
10. Now that the antenna tune procedure is launched:	
i. Wait for *trim_done_irq*.	Indicates that the trim has completed. The trim typically takes less than 25ms.
11. At the end of the antenna tune procedure:	
i. Read IRQ1.	Read to clear the IRQ1 register and to see whether the *trim_fail_irq* status bit has been set.
ii. If IRQ1[4]=1, then the trim ***may*** have failed; see Note 1.	The *trim_fail_irq* status has been set by the tuning procedure when the ANT_TRIM register is set to 0 (minimum) or 31 (maximum). See Note 1.

Note:

1. *If the trim_fail_irq status has been set by the tuning procedure:*
   - *If the tune frequency is at the high end of what the VCO can reach and the trim value is at the lowest trim value, then there is no failure.*
   - *If the tune frequency is at the low end of what the VCO can reach and the trim value is at the highest trim value, then there is no failure.*
   - *Check the value of the ADC during the trimming (the ANT_BEST_ADC register). If the value is below 5 or above 26 then adjust the transmitter output power or LNA gain accordingly.If the value in ANT_BEST_ADC is below 5, increase the transmitter output power by 1; if the value is over 26, decrease the LNA gain by 1. Then rerun this tune.*

6.9 LNA Load Tune

To get enough gain in the front-end amplifier without using much current, an inductive load is tuned to resonate at the receive frequency. The load tuning capacitance must change when the frequency bank changes, and the LNA load tune section of the tune and trim block is required to find the optimum tuning capacitance for a given channel. The tune block saves the setting with the largest peak detector response and restores that setting at the end of the routine.

In a base station this tune requires that enough of the transmitter output power gets back through the TX/RX switch to be in the range of the peak detector.

The LNA load tuning procedure is described in Table 6-11.

***Table 6-11* • Procedure for LNA Load Tune**

1. Write RF_TRIM_CTL=0x02.	The *pd_range* bit should already have been programmed during the previous antenna tune procedure. For this procedure, the peak detector input range should be 100 mV.
2. Write AUTO_TRIM_EN=0x10.	Setting the *lna_en_trim* launches the LNA load tuning procedure. The AUTO_TRIM_EN register is cleared internally once the trim procedure is done.
3. Now that the LNA load tune procedure is launched:	
i. Wait for *trim_done_irq*.	Indicates that the trim has completed. The trim typically takes less than 3 ms.
4. Write RF_EN6=0x00.	Clearing both *man_pa_en* and *man_pa_tx_en* bits disables the power amplifier.
5. Write LNA_GAIN=0x07.	Sets the internal LNA gain back to the default value of 27 dBm.
6. Write RF_CTL4=0x08.	Clearing the *dac_scale_dwn* bit and writing 6'b00 1000 to the *pa_pwr_ctl* bits sets the power amplifier back to the default power setting.
7. At the end of the LNA load tuning procedure:	
i. Read IRQ1.	Read to clear the IRQ1 register and to see whether the *trim_fail_irq* status bit has been set.
ii. If IRQ1[4]=1, then the trim ***may*** have failed; read PD_TRIM and see Note 1.	If the *trim_fail_irq* status has been set by the tuning procedure, read the trim value in the PD_TRIM register and see Note 1.

Note:

1. *If the trim_fail_irq status has been set by the tuning procedure, read the trim value in the PD_TRIM register:*
   - *If the selected frequency range is at the high end of what the VCO can reach and the trim value is at the lowest trim value, then there is no failure. The trim value is appropriate.*
   - *If the tune frequency selected is at the low end of what the VCO can reach and the trim value is at the highest trim value, then there is no failure. The trim value is appropriate.*
   - *Check the value of the ADC during the tuning (the LNA_BEST_ADC register at address 0x7A). If the value is below 5 or above 26 then adjust the transmitter output power or LNA gain accordingly. If the value in LNA_BEST_ADC is below 5, increase the transmitter output power by 1; if the value is over 26, decrease the LNA gain by 1. Then rerun this tune.*

6.10 IF Filter, FM Detector, and Gaussian Filter Tune

The IF filter is critical to rejection of adjacent channel interference and must be tuned to achieve acceptable performance. The frequency discriminator in the FM detector must also be tuned such that its phase shift at IF is 90 degrees. The Gaussian filter characteristics are critical for low-side lobes in the transmitter output spectrum. The IF filter, the FM detector, and the Gaussian filter are designed with a similar topology, with component trimming scaled so that they can be tuned in parallel. The synthesizer programmable divider IF output is enabled and converted to an analog input to the FM detector. This IF signal is as accurate as the crystal oscillator tuning, ±5PPM. The FM detector is then tuned such that the integrated level out of the post-detection filter is zero. The tune register values are at the same time used for the IF filter and Gaussian filter, ensuring that the IF filter's center frequency is at the IF and the Gaussian filter characteristics are as designed. This trim also handles the process, temperature, and voltage variation for the FM detector by determining and then writing an optimal value to the RF_DC_CNTR_TRIM register. This trim value provides the starting point for the FM detector adjustments that are made automatically during the preamble of an incoming data packet.

The tuning procedure is described in Table 6-12.

***Table 6-12* • Procedure for IF Filter, FM Detector, and Gaussian Filter Tune**

1. Calculate the temporary A and M values for generating the IF reference. Refer to the A and M programming example for generating IF reference on page 31. i. Store current values of A and M in temporary memory, where: M=SYNTH_CH_MDIV and A=SYNTH_CH_ADIV[5:0]. ii. Calculate the total divide used in normal operating mode, as follows: $N_{tot}=17 \times A + 16 \times M$ ***EQ 6-1*** iii. Divide N_{tot} by 4 and round to the nearest integer, as follows: $N_{IfDivTot} = Round(N_{tot} / 4)$ *EQ 6-2* iv. Calculate the A and M values for the IF reference mode, as follows: $A_{IfRef}= ((N_{IfDivTot} - 4) \bmod 16) + 4$ *EQ 6-3* $M_{IfRef}=(N_{IfDivTot} - A \times 17) / 16$ *EQ 6-4*	The total divide used in normal operating mode can be found using this formula, copied from EQ 4-3 on page 12.
2. Write SYNTH_CH_MDIV=M_{IfRef}.	The synthesizer A and M values must be temporarily changed to the A_{IfRef} and M_{IfRef} values calculated in step 1iv above.
3. Write SYNTH_CH_ADIV[5:0]=A_{IfRef}.	The A counter should be written after the M value. When the A value is written, both the A and M values are sent to the synthesizer simultaneously.
4. Write RF_EN5=0x20.	Setting the *man_fm_det_en* bit enables the FM detector analog block.
5. Write RF_TRIM_EN=0x01.	Setting the *man_fm_det_en_trim* bit enables the generation of the IF frequency (606kHz). See Note 1.

Note:

1. *When the programmable divider is set to IF reference mode by the man_fm_det_en_trim bit, an additional divide by 4 is introduced in the divide from the VCO frequency down to the phase comparison frequency. The A and M values for the programmable divider must be adjusted such that the VCO runs as close as possible to the frequency to which it was tuned in normal operation so that the PLL can lock. Steps 1i through 1iv can be used to calculate the new A and M values.*

***Table 6-12* • Procedure for IF Filter, FM Detector, and Gaussian Filter Tune (continued)**

6. Wait 2ms.	Wait for the PLL to settle.
7. Write AUTO_TRIM_EN=0x40.	Setting the *fm_det_en_trim* bit launches the IF filter, FM detector, and Gaussian filter tuning procedure. This also enables the PDF (digital block) and the pdf_clk signal coming from clk_gen_a. The AUTO_TRIM_EN register is cleared internally once the trim procedure is done.
8. Now that the IF filter, FM detector, and Gaussian filter tuning procedure is launched:	
i. Wait for *trim_done_irq*.	Indicates that the trim has completed. The trim typically takes less than 505µs at 1.117MHz (i.e., 564 sys_clk clock cycles).
9. Write RF_EN1=0x00.	Clearing the *man_pll_en* bit disables the PLL.
10. Reset A and M values from temporary memory: i. Write SYNTH_CH_MDIV=M. ii. Write SYNTH_CH_ADIV[5:0]=A.	Reset the A and M values to the values that generate the operational frequency bank to be used on the application. The A counter should be written after the M value. When the A value is written, both the A and M values are sent to the synthesizer simultaneously.
11. Write RF_EN5=0x00.	Clearing the *man_fm_det_en* bit disables the FM detector analog block.
12. Write RF_TRIM_EN=0x00.	Clearing the *man_fm_det_en_trim* bit disables the generation of the IF frequency (606kHz).
13. Write IRQ_EN1[5:4]=00.	Clearing the *trim_done_irq_en* and *trim_fail_irq_en* bits disables the *trim_done_irq* and *trim_fail_irq* interrupts, respectively.
14. At the end of the IF filter, FM detector, and Gaussian filter tuning procedure:	
i. Read IRQ1.	Read to clear the IRQ1 register and to see whether the *trim_fail_irq* status bit has been set.
ii. If IRQ1[4]=1, then the trim has failed; check the setup.	If the *trim_fail_irq* status bit has been set by the tuning procedure, the setup may be incorrect.

Note:

1. *When the programmable divider is set to IF reference mode by the man_fm_det_en_trim bit, an additional divide by 4 is introduced in the divide from the VCO frequency down to the phase comparison frequency. The A and M values for the programmable divider must be adjusted such that the VCO runs as close as possible to the frequency to which it was tuned in normal operation so that the PLL can lock. Steps 1i through 1iv can be used to calculate the new A and M values.*

A and M Programming Example for Generating IF Reference

The following example calculation of A and M values for generating the IF reference corresponds to steps 1i through 1iv in Table 6-12 on page 29.

1. Assume the channel frequency is 915.985MHz with a total divide value (N_{tot}) of 3019 (using existing A and M values of 11 and 177 respectively).
2. Divide 3019 by 4 and round to nearest integer using EQ 6-2 on page 29, where $N_{IfDivTot}$ is given by Round(3019 / 4), which equals 755.
3. Find the A value for generating the IF reference, by applying EQ 6-3 on page 29.
   A_{IfRef}=((755 − 4) mod 16) + 4
   =(751 mod 16) + 4
   =15 + 4
   =19
4. Find M value for generating the IF reference, by applying EQ 6-4 on page 29.
   M_{IfRef}=(755 − (19 × 17)) / 16
   =(755 − 323) / 16
   =432 / 16
   =27
5. The VCO frequency is 755 × 4 × 303,407.407Hz = 916.2903691MHz.

6.11 FSK Frequency Separation Trim

The gain of the direct modulating signal must correspond to the frequency bank being used. The modulation DAC must initially be trimmed to achieve the required frequency separation.

The FSK frequency separation trimming procedure is described in Table 6-13.

***Table 6-13* • Procedure for FSK Frequency Separation Trim**

1. Write SYNTH_CTL=0x07.	Setting the *tx_mode_en* bit puts the synthesizer in transmit mode.
2. Program the 40-bit synchronization word: i. Write SYNC_PAT1=0x00. ii. Write SYNC_PAT2=0x00. iii. Write SYNC_PAT3=0x0F. iv. Write SYNC_PAT4=0xFF. v. Write SYNC_PAT5=0xFF.	Set the frame synchronization word to output twenty 0's followed by twenty 1's.
3. Program the radio to transmit the synchronization pattern continuously:	
i. Write MAC_CTL3=0x02.	Setting the *sync_always* bit enables the sync pattern to be sent continuously in transmit operation.
ii. Write MAC_CTL2=0x10.	Setting the *tx_always* bit enables continuous TX of packets, with no TXRX_CMD activity.
iii. Write MAC_CTL1=0x65.	Setting the *port_en*, *transmit_en*, *auto_txrx_en*, and *multi_pkt_en* bits enables the MAC, enables transmit operations, enables auto TX_RX RF control, and enables multipacket mode.
4. Measure the separation between the two peaks with a spectrum analyzer.	A spectrum analyzer with either an antenna or cabled solution can be used to measure the deviation, since the spectrum peaks are separated by two times the frequency deviation.
5. Compare measured frequency separation (FS_{meas}) to 93kHz. i. If $FS_{meas} \leq$ 93kHz, then write MOD_DAC_TRIM=MOD_DAC_TRIM+1 ii. Else: If FS_{meas} is above and as close to 93kHz as possible, then trim is complete. Go to step 7. iii. Else: Write MOD_DAC_TRIM=MOD_DAC_TRIM−1.	Adjust the MOD_DAC_TRIM register until the separation between the two peaks is above and as close to 93kHz as possible. See Note 1.
6. Repeat steps 4 and 5.	
7. Store MOD_DAC_TRIM value in nonvolatile memory.	Since the FSK frequency separation trim is a factory trim, the trim value has to be stored in nonvolatile memory and loaded into the MOD_DAC_TRIM register upon power-up of the device.

Note:

1. *The frequency separation (2×deviation) of 93kHz is for the 186-kbit/s data rate with a modulation index of 0.5 (0.5=93kHz/186kHz). If the lower data rate is used, the frequency separation should be 86kHz to maintain the recommended modulation index of 0.5.*

6.12 Restore Register Values

After completing calibrations from sections "6.1 Calibration Summary" on page 14 through "6.11 FSK Frequency Separation Trim" on page 32, be sure to restore registers that were used to perform calibrations to the original values that were stored prior to performing the calibrations. This, of course, does not include the registers with the newly updated trim values. The registers that should be restored include (but may not be limited to) the registers listed in Table 6-14.

***Table 6-14* • Restoring Register Values**

Register	Address	Recommended Restore Value After Calibrations
CLK_ENS	0x04	0x05
IRQ_EN1	0x07	Restore to previous value, as needed for customer application
ADC_CTL1	0x08	0x01
MAC_CTL1	0x09	0x00 (default)
MAC_CTL2	0x0A	0x40 (default)
RF_EN1	0x0B	0x00 (default)
RF_EN5	0x0F	0x00 (default)
RF_EN6	0x10	0x00 (default)
RF_CTL2	0x12	0x04 (default)
RF_CTL4	0x14	0x08 (default) or restore to previous value as needed for customer application
RF_CTL7	0x17	0x08
RF_TRIM_CTL	0x18	0x00 (default)
RF_TRIM_EN	0x1F	0x00 (default)
LNA_GAIN	0x2F	0x0F (note that this is not the default value)
MAC_CTL3	0x3B	0x00 (default)
SYNC_PAT1	0x4B	0x9A (default)
SYNC_PAT2	0x4C	0x29 (default)
SYNC_PAT3	0x4D	0x8F (default)
SYNC_PAT4	0x4E	0x4D (default)
SYNC_PAT5	0x4F	0xB1 (default)
SYNTH_CH_MDIV	0x5F	Set to value that was calculated for operational frequency per "4.1 A and M Value Calculation" on page 12
SYNTH_CH_ADIV	0x60	Set to value that was calculated for operational frequency per "4.1 A and M Value Calculation" on page 12
SYNTH_CTL	0x61	0x07 (default)
CONT_TRIM_EN	0x6E	0x01 to enable *incdec_modetrans_en* bit after calibrations (note that is not the default value); see "6.14 Enable Automatic Trimming of the VCO" on page 34
VCO_FRQ_CNT	0x77	0x2A (default)
VCO_CTL	0x7C	Set to value that was calculated for operational frequency per Chapter "6.6.1 Frequency Band Selection" on page 20

6.13 Transmitter Output Power Trim

The transmitter output power trim settings are available for adjusting the power level. A programmable binary code selects the transmitter output power level. See the ZL70251 datasheet for transmit power versus PA trim code.

The transmitter output power trimming procedure is described in Table 6-15. Users may determine that the transmitter output power does not need to be trimmed on a part-by-part basis. Instead, a predetermined value can be programmed into every part. If a very accurate output power level is desired, then individual trimming may be necessary. Trim the current reference before any individual trimming is performed.

***Table 6-15* • Procedure for Transmitter Output Power Trim**

1. Determine desired value ($PA_{desired}$) for transmitter output power level. i. In the ZL70251 Datasheet refer to "Figure 3-1 • TX Power vs. PA Trim Value". ii. Choose the PA trim value associated with the desired TX output power.	See Note 1.
2. Write RF_CTL4 = $PA_{desired}$.	Write the desired value (not necessarily the default value) to the RF_CTL4 register.
3. Output a carrier. i. Write RF_EN1 = 0x01.	
4. Measure the transmitter output power with a power meter or spectrum analyzer.	It is recommended that the PA trim value be selected during the design or manufacturing phase when a power meter or spectrum analyzer can be used to measure the transmitter output power. See Note 1; steps 1 through 4 may need to be repeated to ensure that regulatory standards are met.
5. Store RF_CTL4 value in nonvolatile memory.	Since the transmitter output power trim is a factory trim, the trim value has to be stored in nonvolatile memory and loaded into the RF_CTL4 register upon initialization of the device. Alternatively, the power can be preset or even dynamically adjusted based on link conditions.

Note:

1. *Attention must be paid to the second and third harmonics of the transmitted signal when selecting the PA output power so that regulatory standards are not violated. The transmitter output level can be adjusted such that the standards are not met without a SAW filter or a low-pass filter.*

6.14 Enable Automatic Trimming of the VCO

After all calibrations are completed, enable the automatic trimming of the VCO frequency by one bit after each transmitted or received packet (refer to Table 6-16). VCO amplitude trims are not automatically initiated by the device.

***Table 6-16* • Procedure for Enabling Automatic Trimming of VCO**

1. Write CONT_TRIM_EN[0] = 1.	Setting the *incdec_modetrans_en* bit enables the automatic trimming of the VCO frequency by one bit after each transmitted or received packet.

6.15 LNA Gain

The LNA gain is controlled by register LNA_GAIN. Typically, this setting is determined during product development. A value of 0x0F is recommended for maximum sensitivity. If an external LNA is used, then lower gain is recommend. This is to prevent overloading the LNA internal to the ZL70251. In the case of the external LNA, the optimum gain setting can be determined by monitoring the sensitivity while increasing the gain. At some gain setting, the sensitivity begins to crown, which means that the noise figure is limiting the sensitivity. At this point, users may consider backing off the gain by one code to reduce the risk of overloading the internal LNA.

7 – Packet Reception

The ZL70251 offers two modes for receiving packets: preamble detection and RSSI threshold.

- If the RSSI threshold mode is selected, then users must periodically monitor the ambient noise floor and, if necessary, adjust the RSSI threshold accordingly. Refer to "7.1 RSSI Threshold" for recommended usage of this mode.

  The RSSI threshold mode is also recommended for monitoring a channel as in performing a Listen-Before-Talk (LBT) operation. This is described in "8.1 Listen Before Talk (LBT)" on page 40.
- If the preamble detection mode is selected, the receiver searches for the preamble pattern before enabling the search for a valid frame sync. This mode does not require monitoring of the ambient noise floor, allowing operation in environments with a varying noise floor. Refer to "7.2 Preamble Detection" on page 39 for recommended usage of this mode.

7.1 RSSI Threshold

When using the RSSI threshold mode, it is important to know that this threshold level effectively sets the receiver sensitivity. The threshold level is determined by measuring the channel RSSI noise floor and then adding four to that measurement. This guarantees that the signal strength at the receiver is strong enough for the receiver to receive a packet. This threshold level must be sampled periodically so that it stays current with the level of ambient noise in its environment.

During the reception of a packet, the ZL70251 monitors the RSSI level against a predetermined threshold and performs the following two functions based on the receive state of the device:

- If the RSSI level reaches the threshold level, the receiver is enabled to receive a packet.
- If the RSSI level drops below the threshold level for a minimum of 100µs, typically the packet reception is terminated; however, there are variations to this behavior as can be seen in the state machine diagram in Figure 7-1 on page 38.

Paragraphs "7.1.1 Dynamic Calibration of the RSSI Threshold" below and "7.1.2 Searching for Packet (above threshold)" on page 37 give a detailed description for these two functions.

7.1.1 Dynamic Calibration of the RSSI Threshold

The value in the RX_RSSI_THRESH register must be set to a value that allows for the best receiver sensitivity but not too low as to allow false triggering on noise. A noise floor measurement on a channel in use is periodically required to maintain the optimum RSSI threshold setting. Some examples of when this calibration should be performed are:

- At time of initialization or channel selection.
- At random intervals.
- After a packet transmission while waiting for an acknowledgement.
- After detecting link quality issues (for example, several missing acknowledgments).

Follow the procedure in "8.2 RSSI Measurement" on page 41 to determine the noise floor for the channel in use. Once the noise floor has been found, set the threshold above this value by four counts. For example, if a manual RSSI measurement is performed for a desired channel and the result is an average value of 8, then the value in the RX_RSSI_THRESH register should be set to a value of 12. This threshold represents the signal-to-noise ratio required to successfully receive a packet.

7.1.2 Searching for Packet (above threshold)

When the receiver is enabled (see Figure 9-2 on page 44), the ZL70251 receiver state machine enters the **RSSI_SEARCH** state, initiates continuous monitoring of the average RSSI level, and compares this value to the value set in the RX_RSSI_THRESH register (see "7.1.1 Dynamic Calibration of the RSSI Threshold" on page 36). If the average (register ADC_RSSI_AVG) RSSI ADC result is equal to or above the value set in the RX_RSSI_THRESH register, the receiver is enabled and begins searching for a valid frame sync. The ZL70251 stays in this state unless the RSSI ADC result drops below the RX_RSSI_THRESH for more than 100µs as described in "7.1.3 Terminating Packet (below threshold)".

7.1.3 Terminating Packet (below threshold)

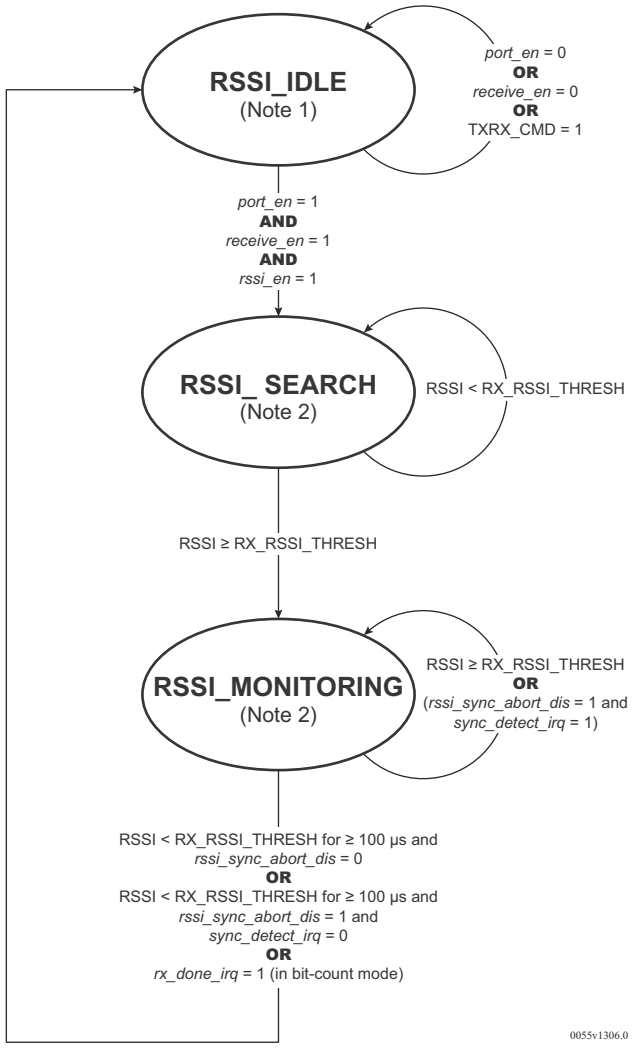
After the receiver is enabled as a result of an RSSI ADC value that is equal to or greater than the RX_RSSI_THRESH as described in "7.1.1 Dynamic Calibration of the RSSI Threshold" on page 36, the ZL70251 device continues to perform ADC samples on the RSSI signal. If the average ADC result falls below the RSSI threshold for a period longer than what is defined by the RSSI_LOST_CNT register (default and recommended value is 100µs) at any point in the receive operation (even during bit-count mode), then the receiver is disabled and the *rx_done_irq* status bit is set. If the RF signal falls below the RSSI threshold before a valid sync pattern is detected, the threshold logic is reset and the *sync_err_irq* status bit is set in the IRQ2 register.

There are four methods for terminating a packet; two are automatic and two are manual. They are:

1. RSSI threshold – After a valid frame sync has been detected, the receiver state machine continuously monitors the RSSI level and compares this level to the value in the RX_RSSI_THRESH register. If at any time, the RSSI level falls below the level set in RX_RSSI_THRESH for greater than 100µs (the default and recommended value for RSSI_LOST_CNT), the packet is terminated and the receiver state machine is reset to the **RSSI_SEARCH** state. This method is typically used in non-bit-count mode to automatically terminate the reception of a packet. This feature may be disabled by setting the *rssi_sync_abort_dis* bit in the MAC_CTL4 register. Users my choose this to allow for the best possible receiver sensitivity by allowing the application to determine whether or not the received packet is valid. If this feature is disabled, then the user must use one of the two methods below to terminate the packet.
2. TXRX_CMD – Raising and then lowering the TXRX_CMD output terminates the packet, thus resetting the receiver state machine to the **RSSI_SEARCH** state. This method is typically used if the application does not receive the *rx_done_irq* in the expected amount of time (usually invoked by a software timeout in the application) and the application needs to resume monitoring for a new packet.
3. MAC_CTL1 – The receiver can be disabled by clearing *receive_en* (bit [1] of the MAC_CTL1 register). This method is typically used if the application does not receive the *rx_done_irq* in the expected amount of time (usually invoked by a software timeout in the application) and no other packets are expected, thus disabling the receiver.
4. Bit-count mode – In bit-count mode, the packet is automatically terminated when the bit count is reached, as indicated by an *rx_done_irq*.

7.1.4 RSSI-RX Mode 1 State Machine

Figure 7-1 is a state machine diagram illustrating the behavior of operation for RSSI-RX Mode 1.



Notes:

1. *If the multi_pkt_en bit is 0, the port_en and receive_en bits have to be cleared and then set to move to the **RSSI_SEARCH** state.*
2. *In this state, the continuous ADC samples of the RSSI level are monitored at the programmed LNA gain.*

Figure 7-1 **• RSSI-RX Mode 1 State Machine**

7.2 Preamble Detection

Preamble detection is alternative option for packet reception. This option detects a valid preamble sequence and uses this detection to enable the AFC/DC settling function. The preamble detector delays starting the AFC and DC-restore settling function until a valid preamble is detected, helping to ensure that the AFC/DC settling function is performed on a valid signal and not on interference or other RF transmissions. Once preamble detection has occurred, the receiver starts searching for frame sync. Once frame sync is detected, the ZL70251 asserts the SPI_SEL_B and begins clocking out the received data bits onto the SPI bus. In the event that frame sync is not detected, usually due to too many bit errors, the use of an 11-ms timer is recommended to abort the "search for frame sync" state and return to the "search for preamble" state. This timer begins counting after preamble detection has occurred. The default value for this register is 11 ms, which is the recommended value to reduce the possibility of a false preamble detect due to a preamble detection that was the result of noise and not a valid preamble. During normal packet exchanges, a false preamble detect is not likely to happen due to the relatively short duration that the receiver is on before a preamble is detected. Where a false timeout is more likely to happen is when a hub in a star network is monitoring transmissions from several nodes in a system. In this case, the hub may be in receive for long periods without a transmission from a node, resulting in several "false preamble detections." This causes the hub to miss "good packet transmissions" from nodes and is therefore not recommended for this case. Alternatively, a node in a star network is normally in receive only in response to a packet transmission (e.g., acknowledge), in which case the device is in receive only for a short period. The node can benefit by improved RX sensitivity.

The procedure for setting up preamble detection mode is described in Table 7-1.

***Table 7-1* • Preamble Detection Mode Setup**

1. Write RX_RSSI_THRESH = 0x00.	Programming the threshold to a minimum in the *rssi_thresh_val* bits disables the RSSI threshold option.
2. Write MAC_CTL4[5] = 1.	Setting the *pream_det_mode* bit enables the preamble detect option.

8 – Channel Monitoring

8.1 Listen Before Talk (LBT)

Typically, in Carrier Sense Multiple Access (CSMA) protocols, a listen-before-talk (LBT) operation is used to avoid collisions with other transmissions or interference on a specified channel. Additionally, for ultra-low-power networks, the "nonpersistent" CSMA access mode is recommended for optimal power conservation at the expense of latency. A common wait time used during an LBT is 5ms, which is therefore used in the programming example in Table 8-1.

***Table 8-1* • Programming Example: Listen Before Talk**

1. Select a channel for operation.	Select the frequency band (see "6.6.1 Frequency Band Selection" on page 20) and program the A and M values (see "4 – Synthesizer Controller" on page 12).
2. Write IRQ_EN1[1]=1.	Setting the *rssi_thresh_irq_en* bit enables the *rssi_thresh_irq* interrupt.
3. Perform a manual RSSI measurement per Table 8-2 on page 41.	Determine the noise floor for the channel in use.
4. Write RX_RSSI_THRESH=ADC_AVG[4:0]+4.	Once the noise floor has been found, set the threshold above this value by four counts, in accordance with section "7.1.1 Dynamic Calibration of the RSSI Threshold" on page 36.
5. Start bidirectional operation with receive first per Table 9-11 on page 58.	Refer to section "9.5.3.3 Start Bidirectional Operation, Receive First (link slave)" on page 58.
6. Set a 5-ms timeout in the processor.	
7. Wait for *rssi_thresh_irq.*	
i. If *rssi_thresh_irq* is asserted, then: a. Wait a random time, b. Go to step 6 if another LBT is desired.	If the *rssi_thresh_irq* occurs within the 5-ms period, wait for a random time before attempting another LBT.
ii. If timeout is reached, then start transmitting.	If timeout occurs before receiving an *rssi_thresh_irq*, transmit a packet.
8. Clean up after procedure:	
i. Write IRQ_EN1[1]=0.	

8.2 RSSI Measurement

The procedure in Table 8-2 describes the programming steps required in performing a manual RSSI measurement. Ensure all calibrations have been performed (refer to section "6 – Calibrations" on page 14) prior to making an RSSI measurement.

***Table 8-2* • Procedure for Manual RSSI Measurement**

1. Write RF_EN1[1] = 0x02.	Setting the *man_rcvr_en* bit manually enables the receiver.
2. Write ADC_CTL1[7:5] = 3'b100.	Writing this value to the *adc_mux_in_sel* bits selects the RSSI as the input to the ADC.
3. Write SYNTH_CTL[2] = 0.	Clear the *tx_mode_en* bit.
4. Write ADC_CTL2[6:2] = 0x1A.	Bits [6:3] set the sample size for the number of sequential RSSI conversions to eight (recommended value) and bit [2] initiates the ADC conversions. Three results are obtained from this sample size: an average RSSI, a peak RSSI, and a last RSSI (see step 5 below). Each ADC conversion takes approximately 10 µs. After all eight conversions are complete, bit [2] is cleared internally.
5. Read ADC_AVG[4:0] and ADC_PEAK[4:0].	These result registers give the average RSSI over eight samples and the peak over eight samples, respectively.
6. Clean up after procedure: i. Restore RF_EN1 value. ii. Restore ADC_CTL1 value. iii. Restore SYNTH_CTL value. iv. Restore ADC_CTL2 value. v. Restore IRQ_EN1 value.	Be sure to restore these registers to the original values that were stored before this procedure began.

9 – MAC

9.1 Power States

Table 9-1 shows the power states of the ZL70251. Refer to the descriptions in "9.2 MAC Bit Descriptions" for the bits that control each state.

***Table 9-1* • Power States and Operational Conditions**

Power State	XTAL Oscillator	sys_clk	PLL	TX Blocks	RX Blocks	Isup (typical)
SLEEP						<500nA
STANDBY	✓					91µA
IDLE	✓	✓				160µA
ACTIVE TX	✓	✓	✓	✓		2.4mA (see Note 1)
ACTIVE RX	✓	✓	✓		✓	2.3mA

Note:

1. *Based on pa_pwr_ctl equal to 8 and a load of 1kΩ.*

9.2 MAC Bit Descriptions

1. *osc_en:* Set high to enable crystal oscillator.
2. *sys_clk_en:* Set high to enable the frequency divider that generates the system clock sys_clk going to the MAC.
3. *auto_txrx_en*: Set high to allow the MAC to control the RF section for configuring for transmit and receive. For transmit, selecting *auto_txrx_en* allows the MAC to enable the power amplifier and the RF transmitter and to set the VCO frequency. For receive, selecting *auto_txrx_en* allows the MAC to enable the RF receiver and to set the VCO frequency.
4. *port_en*: Set high to enable the MAC. Setting *port_en* low is a synchronous reset to all MAC counters and state machines. Setting *port_en* low does not reset the values in the MAC control interface registers.
5. *receive_en*: Set high to enable the receiver. It is used in conjunction with the TXRX_CMD pin to start a receive operation.
6. *transmit_en*: Set high to enable the transmitter. When *auto_txrx_en* is also high, setting *transmit_en* high also allows the MAC to enable the power amplifier, enable the RF modulator, and control opening the PLL loop when in transmit mode.
7. *auto_off*: Set high to enable auto shutdown of the ZL70251. When selected, the RX controller resets MAC_CTL1 when there is no RSSI level detected. By clearing *auto_txrx_en* and *port_en*, the MAC is disabled and the analog/RF section is powered down, including the PLL. Only the crystal oscillator remains active. For the power-down to be effective, it is required that nothing in the RF/MAC section be manually enabled.
8. *tx_first*: Determines whether the first operation is transmit or receive in bidirectional operation. When set high, the first operation is transmit.
9. *rssi_retry_en*: Set high to allow the MAC to stay in receive when the wanted signal goes below the RSSI threshold during a receive in bidirectional mode, instead of switching to transmit. The retry can also occur on pream_timeout if enabled. In both cases, the retry can occur only if the

trigger condition occurs before frame sync is found. If *rssi_sync_abort_dis* is set high in the MAC_CTL4 register, then the radio does not restart on a loss of RSSI after the frame sync is detected.

10. *multi_pkt_en*: Set high to allow the MAC to transfer multiple packets in either receive or transmit. This bit is set low for single packet transmit or single packet receive. This bit must be high for bidirectional operation.
11. *tx_cnt_en* and *rx_cnt_en*: Used to enable termination of transmit and receive operations using the bit-count registers. If these bits are set high, then the termination of transmit or receive occurs when the correct number of bits is transmitted from or to the external controller. If these bits are set low, then transmit or receive is terminated with the *transmit_en* or *receive_en* controls going low, or with a change to the TXRX_CMD pin input from the external controller.
12. *rx_polarity_inv*: Set high to invert the polarity of the received data.
13. *pream_sel[1:0]*: Selects the preamble pattern and the integration period for restoring DC. The transmitter responds only to *pream_sel[0]*. If *pream_sel[0]* is set low, the pattern transmitted is 8'b10101010. If *pream_sel[0]* is set high, the pattern transmitted is 8'b11001100. In receive mode, both bits of *pream_sel* are relevant. Setting *pream_sel[1:0]* equal to 00 selects the preamble pattern 8'b01010101 and the integration period of 12 sys_clk. Setting *pream_sel[1:0]* equal to 01 selects the preamble pattern 8'b11001100 and the integration period of 24 sys_clk.
14. *white_en*: Set high to allow the MAC to whiten data after the sync pattern during transmit, and to dewhiten the data after the sync pattern during receive.

9.2.1 Notes on MAC Control Registers

When programming the MAC control registers MAC_CTL1 and MAC_CTL2, please note that:

- The *transmit_en* bit is used to enable the transmit operation. If *receive_en* is also true (enabling receive operation), then the operation switches to receive mode at the completion of the transmit operation. For bidirectional operation, both *transmit_en* and *receive_en* must be high, as well as *multi_pkt_en*. In bidirectional mode, set the *tx_first* signal high to transmit first. For unidirectional TX-TX operation when *receive_en* is low, the TXRX_CMD pin input from the external controller is used to start and stop transmit operations without entering into receive mode. The transmit operation is always started by 0-to-1 transition on the TXRX_CMD pin after the delay defined by the TX_DELAY register.
- There are four ways to end a transmit operation. If *tx_cnt_en* is set high, then the transmit operation ends when the TX bit counter has decremented to zero. If *tx_cnt_en* is low, then the transmit operation ends when the TXRX_CMD pin goes low. The transmit operation is always ended when *transmit_en* or *port_en* goes low.
- The *receive_en* bit is used to enable the receive operation. If *transmit_en* is set low, then a receive operation is started by *receive_en* high. In this case, when the TXRX_CMD pin goes high, transmit mode is not entered. A receive operation may also be started when both *receive_en* and *transmit_en* go high while *tx_first* is low. In bidirectional mode, the receive operation is started at the end of the transmit operation.
- There are four ways to end a receive operation. If *rx_cnt_en* is high, then the receive operation ends when the RX bit count is complete. If *rx_cnt_en* is low, then the receive operation ends when the TXRX_CMD pin goes high. The receive operation is always terminated if *receive_en* or *port_en* goes low. Finally, if the RSSI level goes low (signal lost) for more than 100 µs, then the receive process restarts and waits for the RSSI level to return. This is always true before frame sync is detected. After frame sync is detected, it is true only if *rssi_sync_abort_dis* is low.
- The *auto_txrx_en* bit is used to enable the MAC to control the RF/analog section during transmit and receive operations. When *auto_txrx_en* is high, the same enables are set as in *man_pll_en*. When *auto_txrx_en* is high, a change from transmit mode to receive mode causes the MAC to turn off the RF TX section, to change the VCO frequency to RX, and to turn on the RF RX section. Conversely, a change from receive to transmit causes the MAC to turn off the RF RX section, to change the VCO frequency to TX, and to turn on the RF TX section (again, when *auto_txrx_en* is high).

9.3 Timing Delays

There are several registers that control the timing in the ZL70251. This timing relates to the sequence of internal operations required to transmit or receive packets. Microsemi recommends using either the default values or the values listed in Table 10-1 on page 62, which were tested and chosen for optimal system performance.

Figure 9-1 illustrates the start-up sequence for a single transmit operation. When the *transmit_en* bit is set in MAC_CTL1, the *pll_delay* delays the start of the transmit state machine. Figure 9-2 illustrates the start-up sequence of a single receive operation. Similarly, if the *receive_en* bit is set, the *pll_delay* delays the start of the receive state machine. In a multipacket operation, this delay is active only on the first packet.

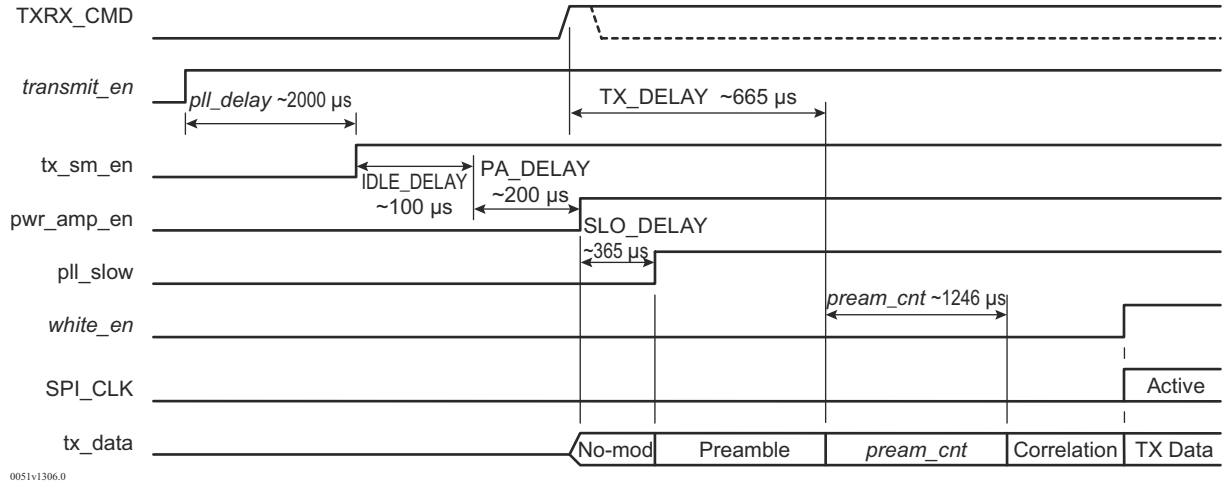


***Figure 9-1* • ZL70251 Transmit Startup**

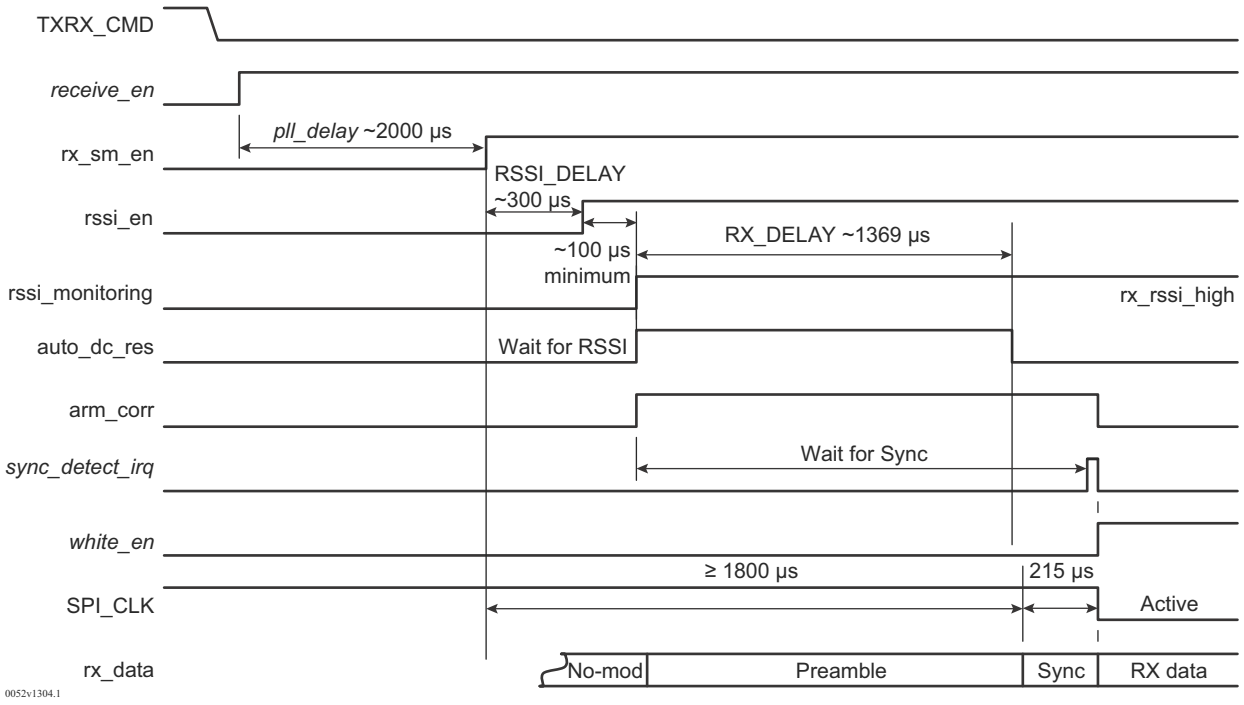


***Figure 9-2* • ZL70251 Receive Startup**

9.4 Use of TXRX_CMD

The TXRX_CMD input is used to control packet transfers in the ZL70251. The behavior of the ZL70251 relative to TXRX_CMD depends on the mode of operation. This section describes the use of TXRX_CMD for various modes of operation. The minimum pulse width requirement on the ZL70251 is 2µs.

9.4.1 Transmit Startup in Bit-Count Mode

In bit-count mode, TXRX_CMD is used to control the beginning of the packet transfer with extended or minimum preamble.

- To extend the preamble, delay the assertion of TXRX_CMD until after the *pll_delay*. TXRX_CMD must be held high for a minimum of 2µs. See Figure 9-3.
- To use the minimum preamble length, assert TXRX_CMD high prior to enabling transmit. TXRX_CMD must be held high until at least 2µs after *pll_delay*. See Figure 9-4 on page 46. The minimum preamble length is the value programmed in *pream_cnt*.

  Note that TXRX_CMD cannot be brought low until 2002µs after enabling transmit. This delay is applicable only for the first packet in multiple-packet transfers. The actual start of the packet, as well as the length of the preamble, can be controlled when TXRX_CMD is pulsed high.

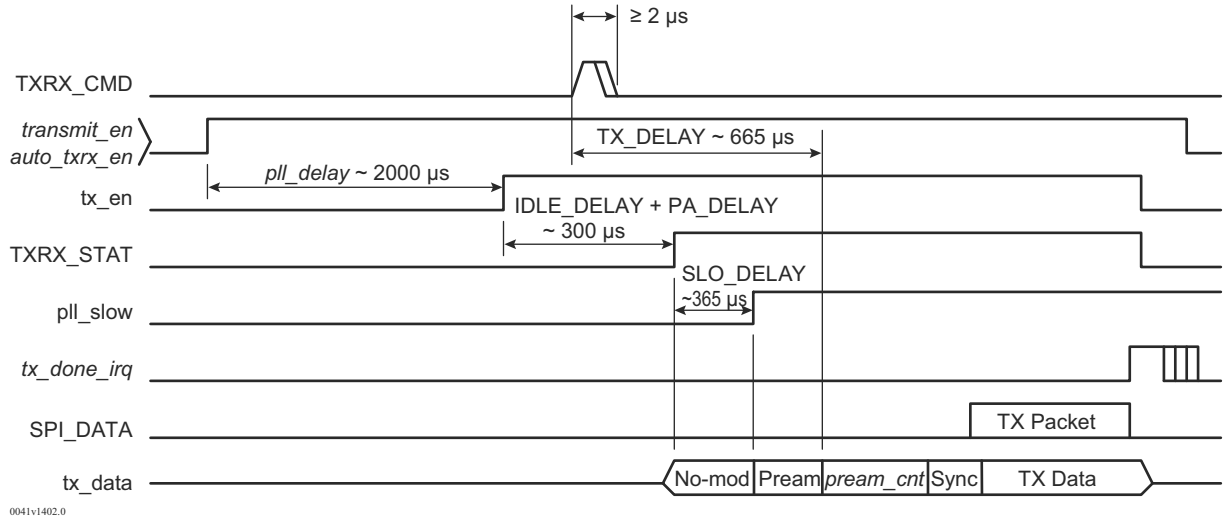


***Figure 9-3* • Start of Transmit in Bit-Count Mode with Pulsed TXRX_CMD**

Figure 9-4 on page 46 shows an example of the second case, where TXRX_CMD is initialized high. In this case, the length of the preamble is controlled solely by *pream_cnt*, and the start of the packet is determined by the series of programmable timers that sequence the start of the packet. The TXRX_CMD pin can be lowered either: any time after 2002µs (the 2000-µs PLL delay plus 2µs), after TXRX_STAT is asserted, or after *tx_done_irq* is asserted.

If the ZL70251 is set up in bidirectional mode such that the next operation is a receive operation, TXRX_CMD must be low before the internal signal rssi_en is asserted. If the ZL70251 is not in bidirectional mode and is set up to transmit only, TXRX_CMD can be left high until another packet needs to be transmitted (pulsing TXRX_CMD low and then back high).

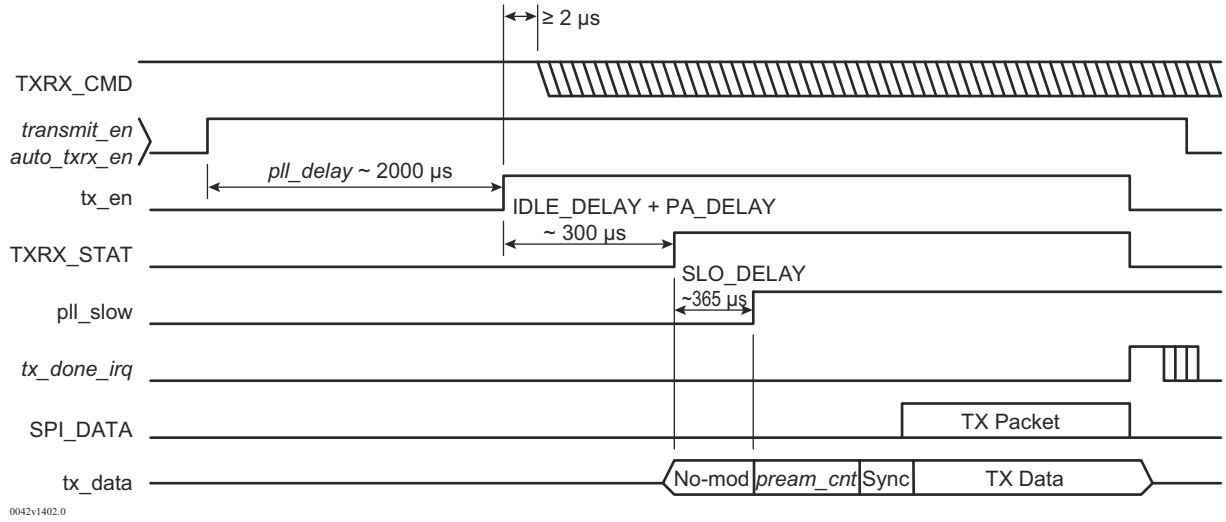


Figure 9-4 **• Start of Transmit in Bit-Count Mode with TXRX_CMD Initialized High**

9.4.2 Transmit Startup in Non-Bit-Count Mode

To start a transmit operation in non-bit-count mode, TXRX_CMD is initialized high and remains high for the duration of the packet. When TXRX_CMD goes low, the packet is terminated. See Figure 9-5. In this mode, TXRX_CMD can also be used to delay the start of the packet or increase the length of the preamble. In this case, TXRX_CMD is initialized low and then raised when sufficient time has elapsed for the desired preamble length and/or start of packet time.

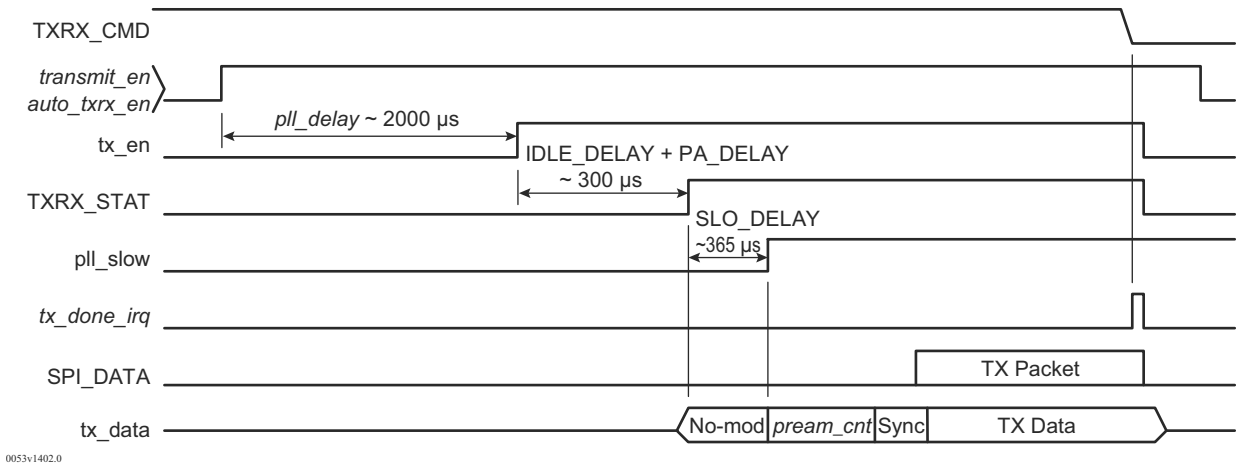


Figure 9-5 **• Start of Transmit in Non-Bit-Count Mode**

9.4.3 Bidirectional Streaming in Bit-Count Mode

Figure 9-6 shows the use of TXRX_CMD in bidirectional streaming operation. TXRX_CMD is pulsed high to start a transmit packet. The rate or interval at which TXRX_CMD is pulsed controls the bit rate of the session. The major limitation of this mode is that TXRX_CMD cannot be pulsed before *rx_done_irq* is asserted at the end of the receive operation. If TXRX_CMD goes high during the receive operation, the receive packet is terminated early.

For bit-count mode, TXRX_CMD can be pulsed high after the *rx_done_irq* is asserted. TXRX_CMD can be pulsed before or after *rx_done_irq* is cleared, but the time at which it is pulsed determines when the next transmit packet starts.

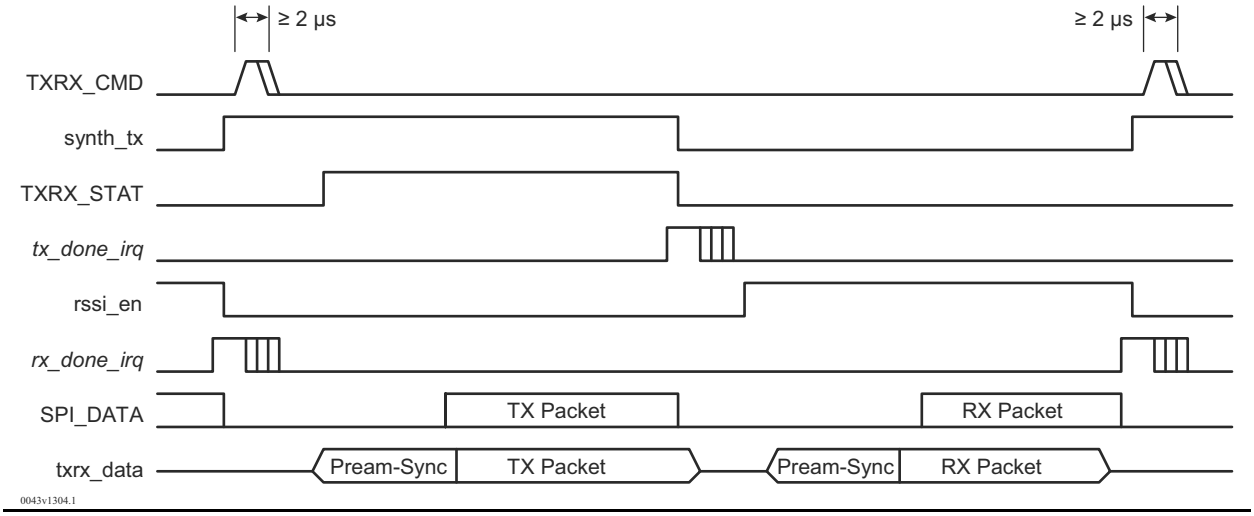


***Figure 9-6* • Bidirectional Streaming in Bit-Count Mode**

9.4.4 Bidirectional Streaming in Non-Bit-Count Mode

The use of TXRX_CMD in bidirectional non-bit-count mode is shown in Figure 9-7. In this mode, TXRX_CMD is set high to transmit a packet, and set low to receive a packet. To control the data rate, the raising of TXRX_CMD must be delayed, which prolongs the receive packet. In this case, extra receive data is sent across the SPI bus and has to be discarded.

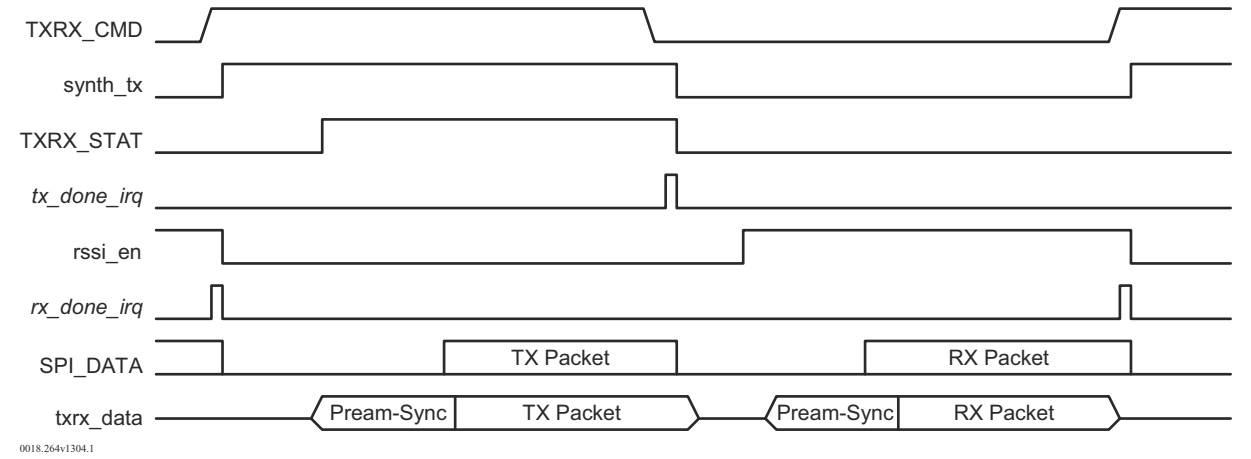


***Figure 9-7* • Bidirectional Streaming in Non-Bit-Count Mode**

9.4.5 Bidirectional Streaming with Mixed Bit-Count Mode

In some cases, such as CSMA (aka LBT) on the link master, it may be necessary to have the transmit side operate in bit-count mode while the receive side operates in non-bit-count mode.

Figure 9-8 shows the use of TXRX_CMD in mixed bit-count mode. In this mode, TXRX_CMD is set high to terminate the receive packet and to start the transmission of the next packet. Like the non-bit-count mode, the only way to control the data rate is to delay raising TXRX_CMD, causing the receive operation across the SPI bus to increase.

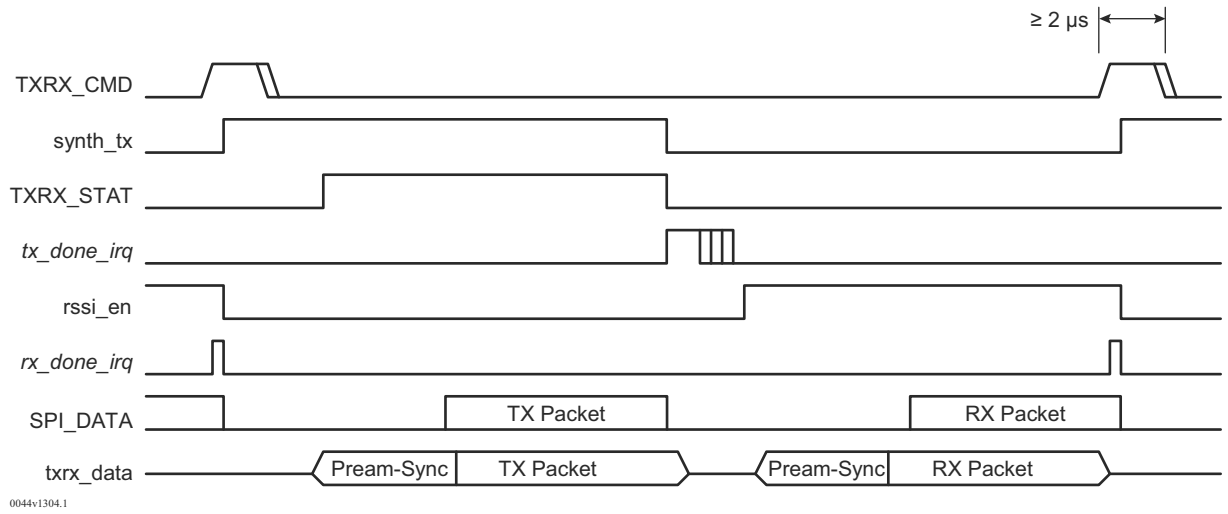


***Figure 9-8* • Bidirectional Streaming in Mixed Bit-Count Mode**

9.4.6 Bidirectional Streaming Startup in Bit-Count Mode

Figure 9-9 shows the use of TXRX_CMD for starting a bidirectional streaming session in bit-count mode, with transmit first. In this case, TXRX_CMD can be pulsed any time after the PLL delay to start the first transmit packet. To start the next transmit packet, TXRX_CMD can be pulsed high at any time after the completion of the receive packet.

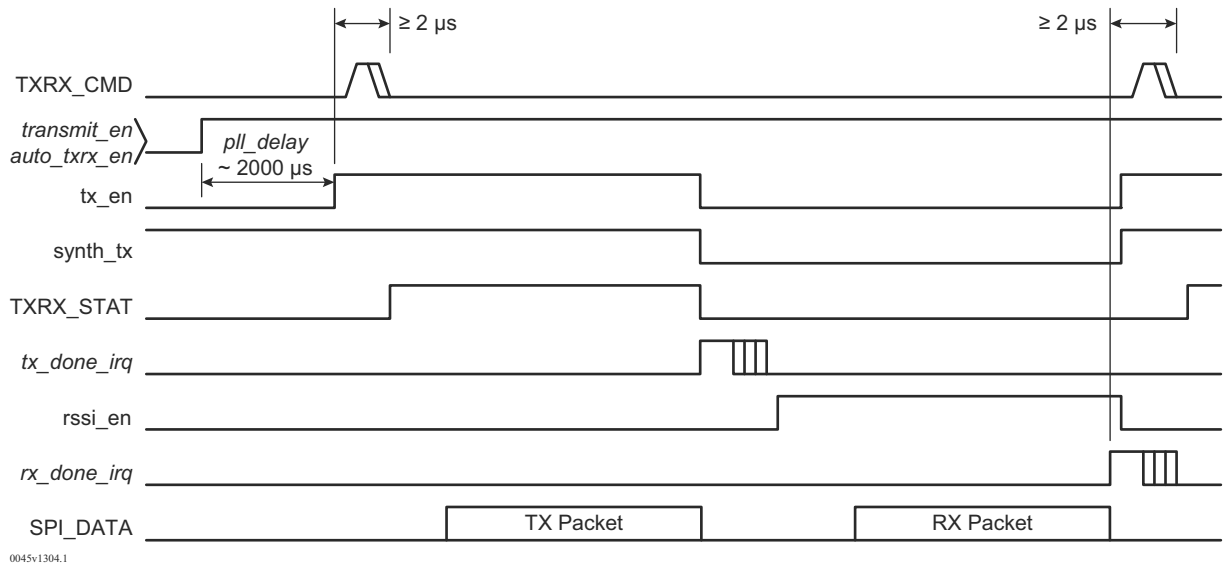


***Figure 9-9* • Bidirectional Streaming Startup in Bit-Count Mode**

Figure 9-10 shows the alternative use of TXRX_CMD to start a bidirectional streaming session in bit-count mode. In this case, TXRX_CMD is initialized high and then lowered some time after the PLL delay. The options for setting TXRX_CMD low after the first packet are: (1) wait for 2002µs (the 2000-µs PLL delay plus 2µs), or (2) wait for TXRX_STAT to go high.

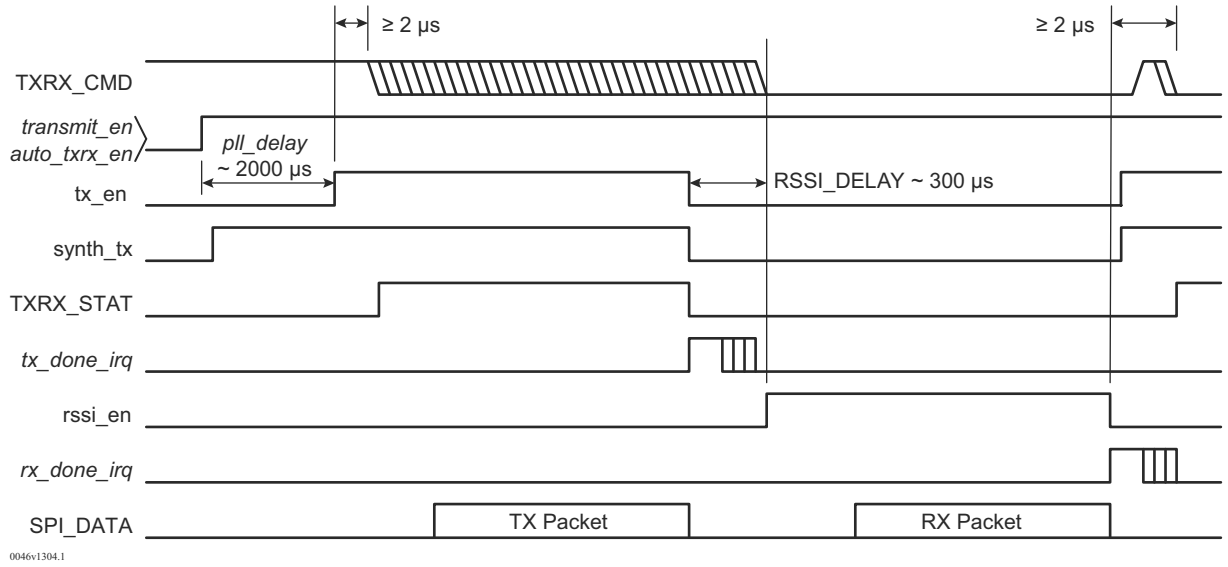


***Figure 9-10* • Bidirectional Streaming Startup in Bit-Count Mode, with TXRX_CMD High**

9.4.7 One-Direction Streaming TX-TX Startup in Bit-Count Mode

Figure 9-11 below and Figure 9-12 on page 50 show the use of TXRX_CMD for one-direction transmit operation in bit-count mode. Like the other transmit cases, TXRX_CMD can either be pulsed high after the PLL delay on the first packet or it can be initialized high. Figure 9-11 shows the first case, with TXRX_CMD pulsed high on the first packet after the PLL delay.

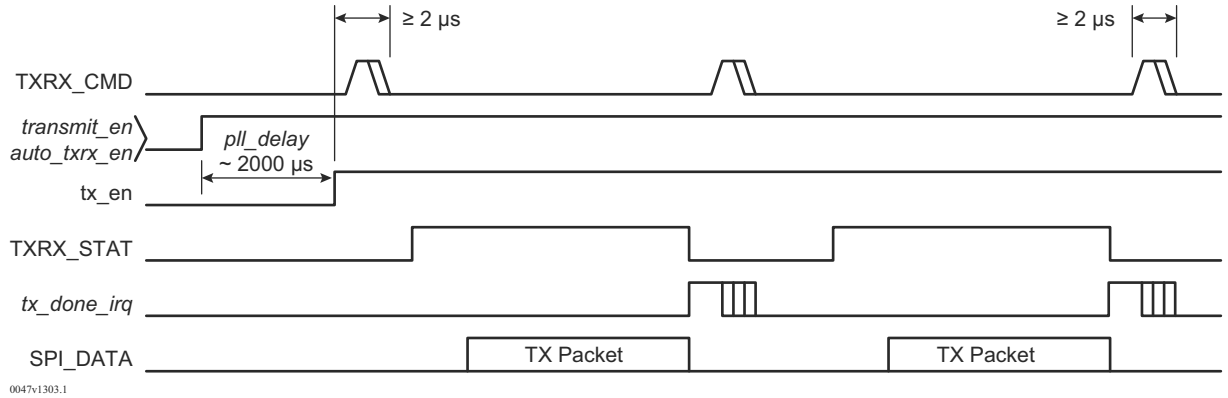


***Figure 9-11* • One Direction Streaming TX-TX Startup in Bit-Count Mode**

Figure 9-12 shows the preferred method of pulsing TXRX_CMD low and back high to start a new transmit packet. In this case, the pulse can be delayed to lengthen the preamble and/or delay the next transmit packet for controlling the data rate.

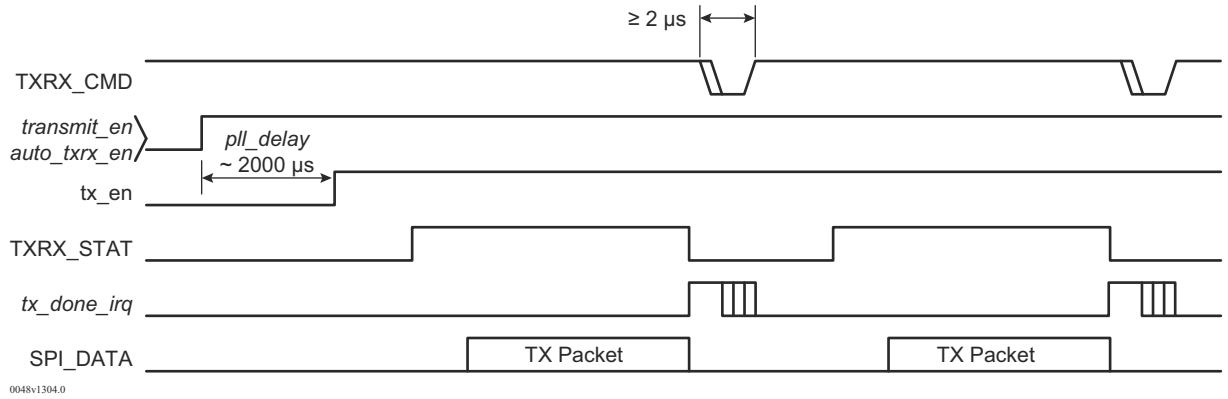


***Figure 9-12* • One Direction Streaming TX-TX Startup in Bit-Count Mode**

9.4.8 One-Direction Streaming TX-TX Startup in Non-Bit-Count Mode

Figure 9-13 shows the use of TXRX_CMD in one-way streaming transmit operation in non-bit-count mode. TXRX_CMD is set low to terminate the transmit packet, and set high again to start the next transmit packet. Setting TXRX_CMD high can be delayed to lengthen the preamble and/or delay the next transmit packet for controlling the data rate.

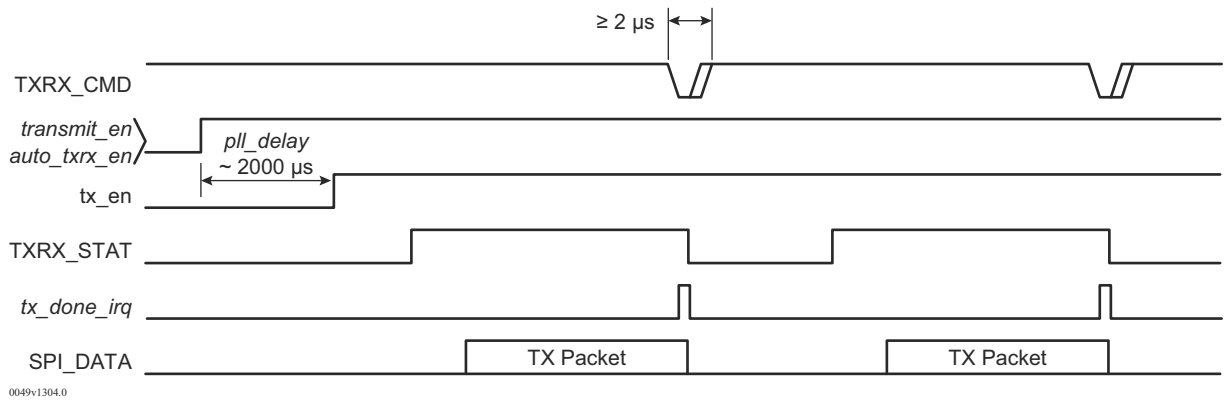


***Figure 9-13* • One Direction Streaming TX-TX Startup in Non-Bit-Count Mode**

9.4.9 One-Direction Streaming RX-RX Startup in Bit-Count Mode

Figure 9-14 shows the use of TXRX_CMD for one-direction streaming receive operation in bit-count mode. In bit-count mode, TXRX_CMD can be initialized low and left low for the entire session.

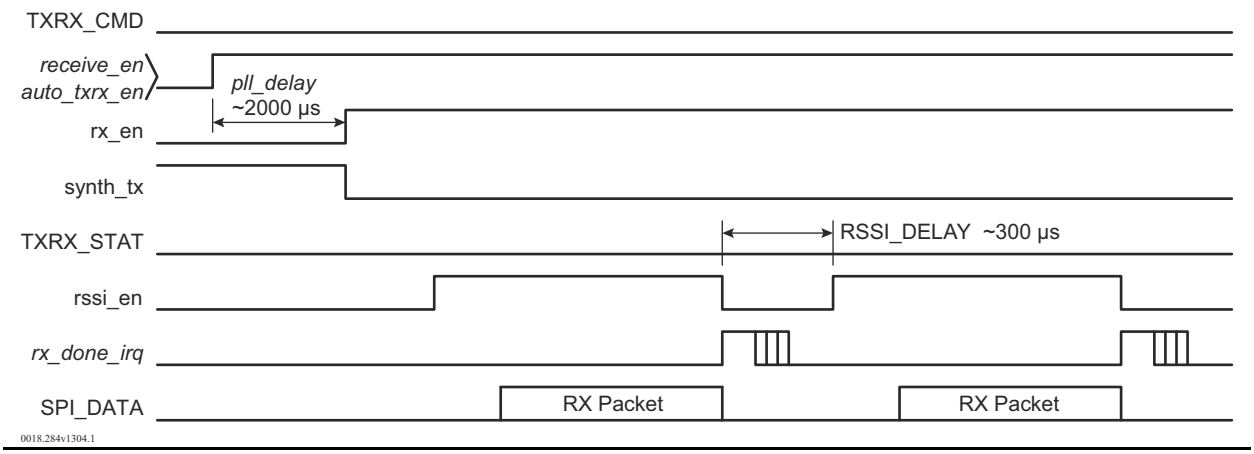


***Figure 9-14* • One Direction Streaming RX-RX Startup in Bit-Count Mode**

9.4.10 One-Direction Streaming RX-RX Startup in Non-Bit-Count Mode

Figure 9-15 shows the use of TXRX_CMD for one-direction streaming receive operation in non-bit-count mode. In this mode, TXRX_CMD must be pulsed high to terminate the receive packet. The time that TXRX_CMD is high is limited to the RSSI delay.

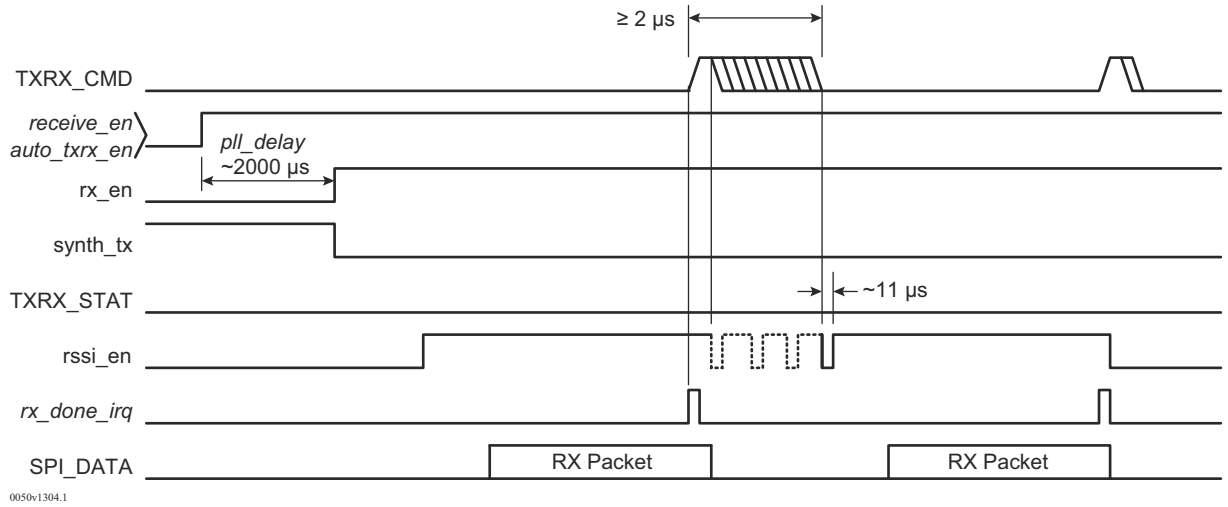


***Figure 9-15* • One Direction Streaming RX-RX Startup in Non-Bit-Count Mode**

9.5 Packet Transfer Operations

There are two options for setting up packet transfer operations:

- Bit-count mode, where transmissions are automatically terminated when a counter reaches a predetermined number of bits.
- Non-bit-count mode, which uses RSSI threshold to determine when a packet transmission is complete.

The option is determined during the design phase. If non-bit-count mode is being used, the user must ensure during design and factory testing that the setup is in accordance with section "7 – Packet Reception" on page 36.

9.5.1 Transmit Operations

9.5.1.1 Setup for Transmit

The procedure to set up for transmit operation is described in Table 9-2.

***Table 9-2* • Procedure to Set Up for Transmit**

1. Write IRQ_EN2[2]=1.	Setting the *tx_done_irq_en* bit enables the *tx_done_irq* interrupt in the IRQ2 register.
2. Set up preferences for transmit operations:	
i. If using bit-count mode, then:	
- Write *tx_cnt*=transmit bit count (bit count is user-defined).	The *tx_cnt* bit word is in the TX_CNT1 (LSB) and TX_CNT2 (MSB) registers.
- Write MAC_CTL2[0]=1.	Setting the *tx_cnt_en* bit enables bit-count mode for transmit operations.
- If whitening data, then write MAC_CTL2[7]=1.	Sets the *white_en* bit.
ii. Else if using non-bit-count mode, then:	Note: If using non-bit-count mode, the user must ensure during design and factory testing that the setup is in accordance with section "7 – Packet Reception" on page 36.
- Write MAC_CTL2[0]=0.	Clear *tx_cnt_en*.
- If whitening data, then write MAC_CTL2[7]=1.	Sets the *white_en* bit.

9.5.1.2 Transmit One Packet

After setting up for transmit, perform the sequence described in Table 9-3 to transmit a single packet.

***Table 9-3* • Procedure to Transmit a Single Packet**

1. Set up for transmit operation per Table 9-2 on page 52.	
2. Initialize the TXRX_CMD pin.	See Note 1.
3. Write MAC_CTL1=0x25.	Sets bits *auto_txrx_en*, *transmit_en*, and *port_en*.
4. Wait for a period greater than or equal to *pll_delay*.	
5. If the TXRX_CMD pin is low, set the TXRX_CMD pin high.	See Note 1. A transmit operation is started by a 0-to-1 transition on the TXRX_CMD pin.
6. Wait for *tx_done_irq*.	Wait for the packet to be transmitted.
7. Clean up after procedure:	
i. Write MAC_CTL1=0x00.	Places the chip in the IDLE power state.
ii. Set the TXRX_CMD pin low.	
iii. Read IRQ2.	The IRQ2 register is cleared on a read operation. This clears the *tx_done_irq* interrupt.

Note:

1. *The TXRX_CMD pin can be initialized high or low, depending on desired preamble length. For details regarding the use of TXRX_CMD to control the beginning of the packet transfer with extended or minimum preamble, refer to "9.4.1 Transmit Startup in Bit-Count Mode" on page 45 and "9.4.2 Transmit Startup in Non-Bit-Count Mode" on page 46.*

9.5.1.3 Transmit Multiple Packets

After setting up for transmit, perform the sequence described in Table 9-4 to transmit multiple packets.

***Table 9-4* • Procedure to Transmit Multiple Packets**

1. Set up for transmit operation per Table 9-2 on page 52.	
2. Initialize the TXRX_CMD pin.	See Note 1.
3. Write MAC_CTL1=0x65.	Sets bits *multi_pkt_en*, *auto_txrx_en*, *transmit_en*, and *port_en*.
4. Wait for a period greater than or equal to *pll_delay*.	
5. If the TXRX_CMD pin is low, set the TXRX_CMD pin high.	See Note 1. A transmit operation is started by a 0-to-1 transition on the TXRX_CMD pin.
6. Wait for *tx_done_irq*.	Wait for the transmission to be complete.
7. Read IRQ2.	The IRQ2 register is cleared on a read operation. This clears the *tx_done_irq* interrupt.
8. Set the TXRX_CMD pin low for a minimum of 2µs.	TXRX_CMD can be held low longer than 2µs, for example to delay the next packet (for controlling the data rate).
9. If all packets have been transferred, then: i. Go to step 10. ii. Else, Go to step 5.	
10. Clean up after procedure: i. Write MAC_CTL1=0x00.	Places the chip in the IDLE power state.

Note:

1. *The TXRX_CMD pin can be initialized high or low, depending on desired preamble length. For details regarding the use of TXRX_CMD to control the beginning of the packet transfer with extended or minimum preamble, refer to "9.4.1 Transmit Startup in Bit-Count Mode" on page 45 and "9.4.2 Transmit Startup in Non-Bit-Count Mode" on page 46.*

9.5.2 Receive Operations

9.5.2.1 Setup for Receive

The procedure to set up for receive operation is described in Table 9-5.

***Table 9-5* • Procedure to Set Up for Receive**

1. Write IRQ_EN2[3]=1.	Setting the *rx_done_irq_en* bit enables the *rx_done_irq* interrupt in the IRQ2 register.
2. Set up preferences for receive operations:	
i. If using bit-count mode, then:	
- Write *rx_cnt*=receive bit count (bit count is user-defined).	The *rx_cnt* bit word is in the RX_CNT1 (LSB) and RX_CNT2 (MSB) registers.
- Write MAC_CTL2[1]=1.	Setting the *rx_cnt_en* bit enables bit-count mode for receive operations.
- If whitening data, then write MAC_CTL2[7]=1.	Sets the *white_en* bit.
ii. Else if using non-bit-count mode, then:	Note: The user must ensure during design and factory testing that the setup is in accordance with section "7 – Packet Reception" on page 36.
- Write MAC_CTL2[1]=0.	Clear *rx_cnt_en*.
- If whitening data, then write MAC_CTL2[7]=1.	Sets the *white_en* bit.
3. Write ADC_CTL1[1:0]=2'b01.	Ensures that RSSI-RX Mode 1 is selected.

9.5.2.2 Receive One Packet

After setting up for receive, perform the sequence described in Table 9-6 to receive a single packet.

***Table 9-6* • Procedure to Receive a Single Packet**

1. Set up for receive operation per Table 9-5.	
2. Write MAC_CTL1=0x23.	Sets bits *auto_txrx_en*, *receive_en*, and *port_en*.
3. Wait for *rx_done_irq*.	Wait for the packet to be received.
4. Clean up after procedure:	
i. Write MAC_CTL1=0x00.	Places the chip in the IDLE power state.
ii. Read IRQ2.	The IRQ2 register is cleared on a read operation. This clears the *rx_done_irq* interrupt.

9.5.2.3 Receive Multiple Packets

After setting up for receive, perform the sequence described in Table 9-7 to receive multiple packets.

***Table 9-7* • Procedure to Receive Multiple Packets**

1. Set up for receive operation per Table 9-5 on page 55.	
2. Write MAC_CTL1=0x63.	Sets bits *multi_pkt_en*, *auto_txrx_en*, *receive_en*, and *port_en*.
3. If MAC_CTL2[1]=0, then:	Steps 3i through 3iv are unnecessary in bit-count mode.
i. Wait for *rx_done_irq*.	Wait for a packet to be received.
ii. Read IRQ2.	The IRQ2 register is cleared on a read operation. This clears the *rx_done_irq* interrupt.
iii. Toggle the TXRX_CMD pin high for a minimum of 2µs.	A transmit operation is started by a 0-to-1 transition on the TXRX_CMD pin.
iv. Set the TXRX_CMD pin low.	TXRX_CMD must be set low to receive a packet.
4. If all packets have been received, then:	
i. Go to step 5.	
ii. Else, Go to step 3.	
5. Clean up after procedure:	
i. Write MAC_CTL1=0x00.	Places the chip in the IDLE power state.
ii. Read IRQ2.	The IRQ2 register is cleared on a read operation. This clears the *rx_done_irq* interrupt.

9.5.2.4 Start Up Asynchronous Receive Session and Resume Receive

The method described in Table 9-8 is used when a packet is expected to be received without a long preamble, so the receiver may come up in the middle of a packet. This method allows resynchronization to the beginning of the next packet. This can be used by a receiver to jump into a one-way audio session for example.

***Table 9-8* • Method to Start Up Asynchronous Receive Session and Resume Receive**

1. Write MAC_CTL1=0xE3.	Sets bits *rssi_retry_en*, *multi_pkt_en*, *auto_txrx_en*, *receive_en*, and *port_en*. Also clears *auto_off*, which sets up for receive operation with the receiver *not* in auto-turn-off mode. See "9.5.2.2 Receive One Packet" on page 55.

With RSSI-RX Mode 1 operation, the following functionality is automatically performed:

1. If there is no RSSI, then continue monitoring for an RSSI.
2. If the RSSI goes away, then restart the RX controller and RSSI-RX Mode 1 returns to monitoring for an RSSI.

9.5.3 Bidirectional Operation

9.5.3.1 Setup for Bidirectional Operation

To set up for bidirectional operation, follow the procedure described in Table 9-9.

***Table 9-9* • Procedure to Set Up for Bidirectional Operation**

1. Write IRQ_EN2[3:2]=2'b11.	Setting the *rx_done_irq_en* and *tx_done_irq_en* bits enables the *rx_done_irq* and *tx_done_irq* interrupts in the IRQ2 register.
2. Set up preferences for bidirectional operations:	
i. If using bit-count mode, then:	
- Write *tx_cnt*=transmit bit count (bit count is user-defined).	The *tx_cnt* bit word is in the TX_CNT1 (LSB) and TX_CNT2 (MSB) registers.
- Write *rx_cnt*=receive bit count (bit count is user-defined).	The *rx_cnt* bit word is in the RX_CNT1 (LSB) and RX_CNT2 (MSB) registers.
- Write MAC_CTL2[1:0]=2'b11.	Setting the *rx_cnt_en* and *tx_cnt_en* bits enables bit-count mode for both receive and transmit operations.
- If whitening data, then write MAC_CTL2[7]=1.	Sets the *white_en* bit.
ii. Else if using non-bit-count mode, then:	Note: The user must ensure during design and factory testing that the setup is in accordance with section "7 – Packet Reception" on page 36.
- Write MAC_CTL2[1:0]=2'b00.	Clear *rx_cnt_en* and *tx_cnt_en*.
- If whitening data, then write MAC_CTL2[7]=1.	Sets the *white_en* bit.
3. Write ADC_CTL1[1:0]=2'b01.	Ensures that RSSI-RX Mode 1 is selected.

9.5.3.2 Start Bidirectional Operation, Transmit First (link master)

After setting up for bidirectional operation, perform the sequence described in Table 9-10 to start bidirectional operation by sending a packet.

***Table 9-10* • Procedure to Start Bidirectional Operation, Transmit First (link master)**

1. Set up for bidirectional operation per Table 9-9 on page 57.	
2. Set the TXRX_CMD pin low.	
3. Write MAC_CTL1=0xF7.	Sets bits *rssi_retry_en*, *multi_pkt_en*, *auto_txrx_en*, *tx_first*, *transmit_en*, *receive_en*, and *port_en*.
4. Wait for a period greater than or equal to *pll_delay*.	
5. Toggle the TXRX_CMD pin high for 2µs.	A transmit operation is started by a 0-to-1 transition on the TXRX_CMD pin.
6. Wait for *rx_done_irq*.	Wait to receive the next packet.
7. Read IRQ2.	The IRQ2 register is cleared on a read operation. This clears both the *tx_done_irq* and *rx_done_irq* interrupts.
8. If all packets have been transferred, then: i. Go to step 9. ii. Else, Go to step 5.	
9. Clean up after procedure: i. Write MAC_CTL1=0x00.	Places the chip in the IDLE power state.

9.5.3.3 Start Bidirectional Operation, Receive First (link slave)

After setting up for bidirectional operation, perform the sequence described in Table 9-11 to start bidirectional operation by receiving a packet.

***Table 9-11* • Procedure to Start Bidirectional Operation, Receive First (link slave)**

1. Set up for bidirectional operation per Table 9-9 on page 57.	
2. Set the TXRX_CMD pin low.	
3. Write MAC_CTL1=0xE7.	Sets bits *rssi_retry_en*, *multi_pkt_en*, *auto_txrx_en*, *transmit_en*, *receive_en*, and *port_en*.
4. Wait for *rx_done_irq*.	Wait for a packet to be received.
5. Set the TXRX_CMD pin high.	A transmit operation is started by a 0-to-1 transition on the TXRX_CMD pin.
6. Wait for *tx_done_irq*.	Wait for a packet to be transmitted.
7. Set the TXRX_CMD pin low.	TXRX_CMD must be set low to receive a packet.
8. If all packets have been transferred, then: i. Go to step 9. ii. Else, Go to step 4.	
9. Clean up after procedure: i. Write MAC_CTL1=0x00.	Places the chip in the IDLE power state.

9.5.4 Transmit or Receive Operation Abort

To manually abort a receive or transmit operation, follow the procedure described in Table 9-12.

***Table 9-12* • Procedure to Manually Abort Receive or Transmit**

1. Write MAC_CTL1=0x00.	Clearing all bits in MAC_CTL1 resets the MAC state machines and counters, and places the chip in the IDLE power state.

9.6 Data Formats

The setup of the MAC and interrupts is the same for PCM operation as it is for SPI operation. The internal operations of ZL70251 behave the same for both modes of operation, with the only difference being in the operation of the external signals on the SPI/PCM bus.

Table 9-13 defines the signals for the different modes of operation on the SPI/PCM bus.

***Table 9-13* • ZL70251 Data Signal Cross-Reference**

	Data Formats		
ZL70251 Pin Name	**SPI**	**PCM**	**I2S**
SPI_CLK	SCK	PCM_CLK	SCK
SPI_SEL_B	SS_n	PCM_SYNC	WS
SPI_DATA_IN	SOMI	PCM_IN	SDI
SPI_DATA_OUT	SIMO	PCM_OUT	SDO

The registers PCM_CTL and FRM_SIZE control the mode of operation on the SPI/PCM bus. In PCM mode, when wide sync is selected, the frame size defines the number of bits between the PCM_SYNC/WS transitions. When wide sync is not selected, the frame size defines the number of bits between the PCM_SYNC/WS pulses. See the memory map for the definition of the control bits.

For detailed timing information, refer to the ZL70251 Datasheet.

10 – System Memory Map

The ZL70251 system memory map (in Table 10-1 on page 62, and in Table 10-2 through Table 10-94 on pages 66 through 87) contains the address for each register, the bit definitions for the register contents, and some programming notes when appropriate. If not all bits are used, the unused bits are read-only and always return a value of zero. All writable bits can be read back at the same address and bit location as written. For values that are longer than eight bits, multiple register addresses are used and the LSB is in the lowest address register.

The register bits fall into the following categories.

- Write and Read (R/W). These bits can be written from the control interface and read back.
- Read only (R). These bits are read-only from the control interface and are not cleared on read.
- Clear on Read (CoR). These bits are cleared to zero when read from the control interface.
- Write, Read, Clear on Done (R/W/CoD). These are command bits that are set to start a command. The current state of the bit can be read any time without affecting the bit value. The bit is cleared automatically when the operation of the command is complete.

Figure 10-1 shows examples of two major types of registers in the ZL70251 memory map. Although these registers are all the same in hardware terms, they have different logical properties and thus require different application programming methods.

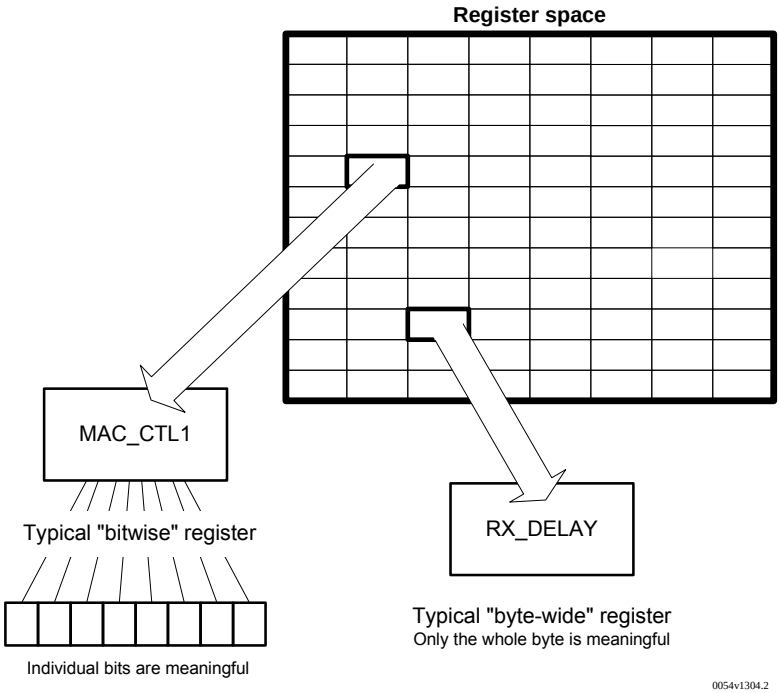


***Figure 10-1* • Major Types of Registers**

- Bitwise registers

  As shown in the detailed memory map (in Table 10-2 through Table 10-94 on pages 66 through 87), many registers contain bits that have logically separate functions, so each bit needs to be considered and programmed individually. When writing to a bitwise register, be careful to modify only the targeted bits and to preserve all others.

When modifying a register that contains reserved bits, always set the reserved bits to the value given in the register description (refer to sections 10.3 through 10.12), or to 0 if no value is given.

In the example shown in Figure 10-1 on page 60, MAC_CTL1 is an eight-bit register where each bit has a separate function:

- MAC_CTL1[7], or *rssi_retry_en*, is RSSI retry mode for RX bidirectional mode, which enables RX controller to stay in receive operation when the RSSI is lost in bidirectional mode.
- MAC_CTL1[6], or *multi_pkt_en*, enables auto multiple packets and enables bidirectional and streaming unidirectional operation.
- MAC_CTL1[5], or *auto_txrx_en*, enables auto TX-RX RF control and allows the MAC to control the analog section for automatic packet transfers.
- MAC_CTL1[4], or *tx_first*, enables transmit first in bidirectional mode.
- MAC_CTL1[3], or *auto_off*, enables auto shutdown and enables autoreset of the MAC if no RSSI is present.
- MAC_CTL1[2], or *transmit_en*, enables transmit operations.
- MAC_CTL1[1], or *receive_en*, enables receive operations.
- MAC_CTL1[0], or *port_en*, enables the MAC when 1 and acts a synchronous reset to the MAC when 0.

• Byte-wide registers

The only difference between a byte-wide register and a bitwise register is that the contents of a byte-wide register are meaningful only as a whole byte. Byte-wise registers can be programmed with a simple write operation.

In the example shown in Figure 10-1 on page 60, RX_DELAY is the register that stores the RX DC restore off delay. For this register, only the whole byte is meaningful.

10.1 Address Space

Table 10-1 • **Memory Map**

Address (Decimal)	Address (Hexadecimal)	Name	R/W	Reset Value (Hexadecimal)	Recommended Value (Note 1)
0	0x00	DEV_ID	R/W	0x45	
1	0x01	APP_ID	R/W	0xFF	
2	0x02	CHIP_IDL	R	0x16	
3	0x03	CHIP_IDH	R	0x0E	
4	0x04	CLK_ENS	R/W	0x23	
5	0x05	SSI_CTL	R/W	0x03	
6	0x06	IRQ_EN2	R/W	0x00	
7	0x07	IRQ_EN1	R/W	0x00	
8	0x08	ADC_CTL1	R/W	0x00	0x01
9	0x09	MAC_CTL1	R/W	0x00	
10	0x0A	MAC_CTL2	R/W	0x40	
11	0x0B	RF_EN1	R/W	0x00	
15	0x0F	RF_EN5	R/W	0x00	
16	0x10	RF_EN6	R/W	0x00	
18	0x12	RF_CTL2	R/W	0x04	0x06
20	0x14	RF_CTL4	R/W	0x08	
23	0x17	RF_CTL7	R/W	0x0D	0x08
24	0x18	RF_TRIM_CTL	R/W	0x00	
31	0x1F	RF_TRIM_EN	R/W	0x00	
32	0x20	IREF_TRIM	R/W	0x0F	
33	0x21	XO_TRIM	R/W	0x26	
34	0x22	INTERNAL34	R/W	0x02	0x01
35	0x23	MOD_DAC_TRIM	R/W	0x0F	
36	0x24	GAUS_TRIM	R/W	0x62	
37	0x25	VCO_AMP_TRIM	R/W	0x3F	
38	0x26	ANT_TRIM	R/W	0x16	
39	0x27	PD_TRIM	R/W	0x09	
40	0x28	LNA_TRIM1	R/W	0x16	
41	0x29	LNA_TRIM2	R/W	0x05	

Notes:

1. *Use this recommended initial register setting by writing this value after every chip reset. Device characterization has shown that the recommended value gives better system performance.*
2. *It is recommended that the default value (or reset value) be used. Do not write to this register.*
3. *For use with 200-kHz occupied bandwidth and/or 200-kHz channelization, please see recommended initialization values in "2.2 Using the Lower Data Rate (136.5kbit/s, 200-kHz channels)" on page 10.*

Table 10-1 **• Memory Map (continued)**

Address (Decimal)	Address (Hexadecimal)	Name	R/W	Reset Value (Hexadecimal)	Recommended Value (Note 1)
42	0x2a	RF_DC_CNTR_TRIM	R/W	0x62	
44	0x2C	ADC_CTL2	R/W/CoD	0x00	
46	0x2E	RSSI_LOST_CNT	R/W	0x14	
47	0x2F	LNA_GAIN	R/W	0x07	0x0F
49	0x31	INTERNAL49	R/W	0x07	0x0F
50	0x32	INTERNAL50	R/W	0x07	0x0F
51	0x33	INTERNAL51	R/W	0x08	0x1F
52	0x34	RX_RSSI_THRESH	R/W	0x08	
53	0x35	ADC_RESULT	R	0x00	
55	0x37	RX_RSSI_RESULT	R	0x00	
56	0x38	ADC_PEAK	R	0x00	
57	0x39	ADC_AVG	R	0x00	
59	0x3B	MAC_CTL3	R/W	0x00	
60	0x3C	PCM_CTL	R/W	0x00	
61	0x3D	FRM_SIZE	R/W	0x20	
63	0x3F	PLL_DELAY1	R/W	0x74 (Note 2)	
64	0x40	PLL_DELAY2	R/W	0x01 (Note 2)	
65	0x41	IDLE_DELAY	R/W	0x13 (Note 2)	
66	0x42	PA_DELAY	R/W	0x25 (Note 2)	
67	0x43	TX_DELAY	R/W	0x7C (Note 2)	
68	0x44	SLO_DELAY	R/W	0x44 (Note 2)	
69	0x45	RSSI_DELAY	R/W	0x38 (Note 2)	
70	0x46	RX_DELAY	R/W	0xFF	
71	0x47	TX_CNT1	R/W	0xFF	
72	0x48	TX_CNT2	R/W	0xFF	
73	0x49	RX_CNT1	R/W	0xFF	
74	0x4A	RX_CNT2	R/W	0xFF	
75	0x4B	SYNC_PAT1	R/W	0x9A	
76	0x4C	SYNC_PAT2	R/W	0x29	
77	0x4D	SYNC_PAT3	R/W	0x8F	
78	0x4E	SYNC_PAT4	R/W	0x4D	

Notes:

1. *Use this recommended initial register setting by writing this value after every chip reset. Device characterization has shown that the recommended value gives better system performance.*
2. *It is recommended that the default value (or reset value) be used. Do not write to this register.*
3. *For use with 200-kHz occupied bandwidth and/or 200-kHz channelization, please see recommended initialization values in "2.2 Using the Lower Data Rate (136.5kbit/s, 200-kHz channels)" on page 10.*

Table 10-1 **• Memory Map (continued)**

Address (Decimal)	Address (Hexadecimal)	Name	R/W	Reset Value (Hexadecimal)	Recommended Value (Note 1)
79	0x4F	SYNC_PAT5	R/W	0xB1	
81	0x51	PREAM_CNT	R/W	0x1A	
82	0x52	PREAM_LOCK_CNT	R/W	0x12 (Note 2)	
93	0x5D	MAC_DOUT0	R/W	0x00	
94	0x5E	MAC_DOUT1	R/W	0x00	
95	0x5F	SYNTH_CH_MDIV	R/W	0xB5	
96	0x60	SYNTH_CH_ADIV	R/W	0x07	Note 3
97	0x61	SYNTH_CTL	R/W	0x07	
99	0x63	MOD_PHASE_CNT	R/W	0X17	Note 3
101	0x65	SYS_CLK_DIV	R/W	0x16	Note 3
102	0x66	CLK_OUT_DIV	R/W	0x18	
105	0x69	IRQ1	CoR	0x00	
107	0x6B	IRQ2	CoR	0x00	
108	0x6C	RF_STAT	R	0x00	
109	0x6D	AUTO_TRIM_EN	R/W/CoD	0x00	
110	0x6E	CONT_TRIM_EN	R/W	0x00	
111	0x6F	VFT_RX_L	R/W	0xFF	
112	0x70	VFT_RX_H	R/W	0x04	
113	0x71	VFT_PAOFF_L	R/W	0xFF	
114	0x72	VFT_PAOFF_H	R/W	0x04	
115	0x73	VFT_PAON_L	R/W	0xFF	
116	0x74	VFT_PAON_H	R/W	0x04	
117	0x75	VFT_L	R	0xFF	
118	0x76	VFT_H	R	0x04	
119	0x77	VCO_FRQ_CNT	R/W	0x2A	
122	0x7A	LNA_BEST_ADC	R	0x00	
123	0x7B	ANT_BEST_ADC	R	0x00	
124	0x7C	VCO_CTL	R/W	0x06	
127	0x7F	MAC_DOUT2	R/W	0x00	

Notes:

1. *Use this recommended initial register setting by writing this value after every chip reset. Device characterization has shown that the recommended value gives better system performance.*
2. *It is recommended that the default value (or reset value) be used. Do not write to this register.*
3. *For use with 200-kHz occupied bandwidth and/or 200-kHz channelization, please see recommended initialization values in "2.2 Using the Lower Data Rate (136.5kbit/s, 200-kHz channels)" on page 10.*

Table 10-1 **• Memory Map (continued)**

Address (Decimal)	Address (Hexadecimal)	Name	R/W	Reset Value (Hexadecimal)	Recommended Value (Note 1)
128	0x80	MAC_CTL4	R/W	0x00	
130	0x82	STATUS_REG	R	0x00	
131	0x83	ADC_CTL5	R/W	0x00	0x0B
132	0x84	ADC_RSSI_AVG	R	0x00	

Notes:

1. *Use this recommended initial register setting by writing this value after every chip reset. Device characterization has shown that the recommended value gives better system performance.*
2. *It is recommended that the default value (or reset value) be used. Do not write to this register.*
3. *For use with 200-kHz occupied bandwidth and/or 200-kHz channelization, please see recommended initialization values in "2.2 Using the Lower Data Rate (136.5kbit/s, 200-kHz channels)" on page 10.*

10.2 Control Interface Registers

Table 10-2 **• DEV_ID (Address 0x00)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	dev_id	Control interface device ID	R/W	01000101

Table 10-3 **• APP_ID (Address 0x01)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	app_did	Application ID	R/W	11111111

Table 10-4 **• CHIP_IDL (Address 0x02)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	chip_idl	Identifies the chip revision (low byte)	R	00010110

Table 10-5 **• CHIP_IDH (Address 0x03)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	chip_idh	Identifies the chip revision (high byte)	R	00001110

Table 10-6 **• CLK_ENS (Address 0x04)**

Bit	Bit Definition	Description	Type	Reset Value
7:6	–	<Reserved>	R	00
5	osc_en_stat	Read-only status of XTAL oscillator enable output	R	1
4	clksel_pd_dis	Disable CLKSEL pull-down: • 1: disable • 0: enable	R/W	0
3	ext_osc_en	Enable external control for *osc_en* from CLKSEL pin	R/W	0
2	sys_clk_en	Enable the frequency divider that generates the system clock sys_clk going to the MAC	R/W	0
1	clk_out_en	Enable the frequency divider that generates the external clock	R/W	1
0	osc_en	Enable XTAL oscillator	R/W	1

Table 10-7 **• SSI_CTL (Address 0x05)**

Bit	Bit Definition	Description	Type	Reset Value
7:2	–	<Reserved>	R	000000
1	wr_auto_incr	Write autoincrement	R/W	1
0	rd_auto_incr	Read autoincrement	R/W	1

10.3 Global Enables Register

Table 10-8 **• RF_EN1 (Address 0x0B)**

Bit	Bit Definition	Description	Type	Reset Value
7:3	–	<Reserved>	R	00000
2	man_pll_en	Enable PLL globally; turns on all blocks related to PLL	R/W	0
1	man_rcvr_en	Enable receive channel globally; turns on all blocks needed for receiver operation	R/W	0
0	man_xmtr_en	Enable transmit channel; turns on all blocks needed for transmitter operation	R/W	0

10.4 Analog Enables Registers

Table 10-9 **• RF_EN5 (Address 0x0F)**

Bit	Bit Definition	Description	Type	Reset Value
7	man_adc_ana_en	Enable ADC analog block	R/W	0
6	–	<Reserved>	R	0
5	man_fm_det_en	Enable FM detector	R/W	0
4:2	–	<Reserved>	R	000
1	man_pd_en	Enable peak detector	R/W	0
0	man_rf_en	Enable mixer and enable LNA	R/W	0

Table 10-10 **• RF_EN6 (Address 0x10)**

Bit	Bit Definition	Description	Type	Reset Value
7:2	–	<Reserved>	R	000000
1	man_pa_tx_en	Enable transmit mode of power amplifier	R/W	0
0	man_pa_en	Enable power amplifier	R/W	0

Table 10-11 **• RF_TRIM_EN (Address 0x1F)**

Bit	Bit Definition	Description	Type	Reset Value
7:1	–	<Reserved>	R	0000000
0	man_fm_det_en_trim	Set blocks for trimming the FM detector in manual mode	R/W	0

10.5 Analog Control Registers

Table 10-12 **• RF_CTL2 (Address 0x12)**

Bit	Bit Definition	Description	Type	Reset Value
7:1	–	<Internal bits; always write binary 0000011 to these bits>	R/W	0000010
0	man_gaus_mod	The Gaussian filter shapes the modulating signal going from the modulation DAC to the VCO so that the output spectrum is reduced in bandwidth	R/W	0

Note: For recommended initial register setting, see "Recommended Value" column of Table 10-1 on page 62.

***Table 10-13* • RF_CTL4 (Address 0x14)**

Bit	Bit Definition	Description	Type	Reset Value
7	–	<Reserved>	R	0
6	dac_scale_dwn	Enable DAC scale down by one half	R/W	0
5:0	pa_pwr_ctl	Sets the transmitter output power level; see Note	R/W	001000

Note: ***Warning:*** *Power output depends on the impedance of the load. The power amplifier is designed for current output into a tuned load of approximately 1kΩ. Care must be taken that the output voltage does not clip.*

***Table 10-14* • RF_CTL7 (Address 0x17)**

Bit	Bit Definition	Description	Type	Reset Value
7:6	–	<Reserved>	R	00
5	half_band	Allows the VCO to shift a half band for the VCO calibrations. This bit should be set or cleared if the VCO calibration results are near a band edge.	R/W	0
4:3	–	<Internal bits; always write binary 01 to these bits>	R/W	01
2:0	kvco_ctl	VCO tuning bridge control. *kvco_ctl* is used to select the gain of the varactor in the VCO. The higher the VCO frequency, the higher this control should be set. If *kvco_ctl* is 0, the varactor gain is automatically selected by the VCO frequency trim bits.	R/W	101

Note: For recommended initial register setting, see "Recommended Value" column of *Table 10-1 on page 62**.*

***Table 10-15* • RF_TRIM_CTL (Address 0x18)**

Bit	Bit Definition	Description	Type	Reset Value
7:2	–	<Reserved>	R	000000
1	pd_range	Peak detector control in trim mode: • 0: Peak detector input range of 50mV. • 1: Peak detector input range of 100mV. Peak detector range is specified as the voltage into the peak detector after LNA gain. The full-scale voltage out of the peak detector is always 700mV, full scale for the ADC.	R/W	0
0	–	<Reserved>	R	0

***Table 10-16* • RF_DC_CNTR_TRIM (Address 0x2A)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	dc_cntr_trim	Center point of DAC transfer function. This value, written by the FM detector trim function, represents the trimming needed to take out process variations but not offsets due to transmitter carrier frequency.	R/W	01100010

10.6 Trim Registers

***Table 10-17* • IREF_TRIM (Address 0x20)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	iref_trim	IREF trimming code for the resistor for PTAT and constant current generator; a higher trim code means a higher resistor value (and lower current)	R/W	01111

***Table 10-18* • XO_TRIM (Address 0x21)**

Bit	Bit Definition	Description	Type	Reset Value
7:6	–	<Reserved>	R	00
5:0	xo_trim	Trimming code for crystal oscillator (0 for minimum frequency; maximum value is 63)	R/W	100110

***Table 10-19* • INTERNAL34 (Address 0x22)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	–	<Internal register; always write binary 00000001 to this register> *Note: For recommended initial register setting, see "Recommended Value" column of Table 10-1 on page 62.*	R/W	00000010

***Table 10-20* • MOD_DAC_TRIM (Address 0x23)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	mod_dac_trim	Modulation index trimming code; a higher trim value means wider VCO modulation (higher modulation index)	R/W	01111

***Table 10-21* • GAUS_TRIM (Address 0x24)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	gaus_gm_trim	Tuning value of the Gaussian filter. The trim and tune block writes this register with the same trim value used for the IF filter and FM detector (after the FM detector trim function), but the trim value should be set to 0xFF for best system performance that still meets the 300-kHz channel restrictions. A higher trim value means wider bandwidth.	R/W	01100010

***Table 10-22* • VCO_AMP_TRIM (Address 0x25)**

Bit	Bit Definition	Description	Type	Reset Value
7:6	–	<Reserved>	R	00
5:0	vco_amp_trim	Coarse tuning value of the VCO. Higher trim value means a larger amplitude of oscillations in the VCO. The default is at the highest level to make sure the VCO starts. The trim and tune block should be used to trim the amplitude to 300 mV, 350 mV, 400 mV, or 450 mV.	R/W	111111

***Table 10-23* • ANT_TRIM (Address 0x26)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	ant_trim	Adjustment value of capacitive load to center frequency of antenna; higher trim value means larger capacitance and lower tuning frequency for the antenna	R/W	10110

***Table 10-24* • PD_TRIM (Address 0x27)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	pd_trim	Peak detector trimming code. This trim is for the peak detector DC offset. Higher values cause positive offset. The trim and tune block should be used to automatically trim this block.	R/W	01001

***Table 10-25* • LNA_TRIM1 (Address 0x28)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	lna_frq_trim	LNA load tune code. The LNA load is an inductor that should be tuned to obtain the highest gain from the LNA. Higher trim values represent higher capacitance and therefore lower resonant frequency. Use the trim and tune block to automatically trim.	R/W	10110

***Table 10-26* • LNA_TRIM2 (Address 0x29)**

Bit	Bit Definition	Description	Type	Reset Value
7:4	–	<Reserved>	R	0000
3:2	lna_bias_trim	LNA bias tune code. LNA biases can be set higher to get more gain on the receiver front-end, but more current is used. The default is recommended when trying to stay below 2.4 mA supply current consumption.	R/W	01
1:0	mix_bias_trim	Mixer bias tune code. Mixer biases can be set higher to get more gain on the receiver front-end, but more current is used.	R/W	01

10.7 ADC Registers

Table 10-27 **• ADC_CTL1 (Address 0x08)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	adc_mux_in_sel	In ADC mode, ADC input selection: • 000: None of the inputs are selected (analog mux output floats). • 001: AMX2 is selected. This should be used for the mixer offset trim. The VDDTEST pin must be connected to VDD or 3.5V to allow the analog test bus to be used properly. • 010: Peak detector output is selected. • 100: RSSI output (rx_rssi) is selected. • Others: If more than one bit is set, more than one switch is turned on according to the input selection. That is an illegal operation. In RSSI-RX mode, these bits are ignored as the ADC input selection is automatically controlled internally.	R/W	000
4:2	–	<Reserved>	R	000
1:0	rssi_rx_mode	Select RSSI-RX mode: • 01: Mode 1. Run until the RSSI detected, without gain adjust (manual gain control). See Note.	R/W	00

Note: For recommended initial register setting, see "Recommended Value" column of Table 10-1 on page 62. It is recommended that bits [4:0] always use the recommended initialization setting.

***Table 10-28* • ADC_CTL2 (Address 0x2C)**

Bit	Bit Definition	Description	Type	Reset Value
7	–	<Reserved>	R	0
6:3	pow_n_conv	In ADC mode, determine the number of conversions before updating the peak value (ADC_PEAK) and the average value (ADC_AVG). It also determines when the ADC interrupt pulses (ADC complete and ADC threshold interrupts) are generated. See Note 1. • 0000: 1 conversion • 0001: 2 conversions • 0010: 4 conversions • 0011: 8 conversions • 0100: 16 conversions • 0101 32 conversions • 0110: 64 conversions • 0111: 128 conversions • 1000: 256 conversions • 1001: 512 conversions • 1010: 1024 conversions • 1011 to 1111: 2048 conversions	R/W	0000
2	–	<Reserved>	R	0
1	single_conv	Start single ADC conversion mode if set high. The first conversion is automatically followed by $2^{pow\_n\_conv} - 1$ other conversions in a row for the average value. Then no more conversions take place. See Note 2.	R/W/CoD	0
0	cont_conv	Start continuous ADC conversions mode if set high. Single ADC conversions are continuously running. See Note 2.	R/W	0

Notes:

1. *A single ADC conversion takes six cycles of the sys_clk; 6 / 1.117MHz ≈ 5.371µs.*
2. *The continuous ADC conversions mode has priority over the single ADC conversion mode, in the case where they are both active. The RSSI-RX mode has priority over both continuous conversions mode and single conversion mode.*

***Table 10-29* • RSSI_LOST_CNT (Address 0x2E)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	rssi_lost_cnt	The value of this register times the bit period defines the amount of time that the RSSI level has to be below the RSSI threshold to automatically reset the receiver	R/W	00010100

***Table 10-30* • LNA_GAIN (Address 0x2F)**

Bit	Bit Definition	Description	Type	Reset Value
7:4	–	<Reserved>	R	0000
3:0	lna_gain	Internal LNA gain. The approximate gain for each code is as follows: • 1111: 30 dBm • 0111: 27 dBm (default) • 0011: 24 dBm • 0001: 20 dBm • 0000: 16 dBm	R/W	0111

Note: For recommended initial register setting, see "Recommended Value" column of Table 10-1 on page 62.

***Table 10-31* • INTERNAL49 (Address 0x31)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	–	<Internal register; always write binary 00001111 to this register> *Note: For recommended initial register setting, see "Recommended Value" column of Table 10-1 on page 62.*	R/W	00000111

***Table 10-32* • INTERNAL50 (Address 0x32)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	–	<Internal register; always write binary 00001111 to this register> *Note: For recommended initial register setting, see "Recommended Value" column of Table 10-1 on page 62.*	R/W	00000111

***Table 10-33* • INTERNAL51 (Address 0x33)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	–	<Internal register; always write binary 00011111 to this register> *Note: For recommended initial register setting, see "Recommended Value" column of Table 10-1 on page 62.*	R/W	00001000

***Table 10-34* • RX_RSSI_THRESH (Address 0x34)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	rssi_thresh_val	Threshold value for the RSSI	R/W	01000

***Table 10-35* • ADC_RESULT (Address 0x35)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	adc_result	ADC result after each conversion. The result depends on which input is selected from the ADC_CTL1 register (see "7.1 RSSI Threshold" on page 36).	R	00000

***Table 10-36* • RX_RSSI_RESULT (Address 0x37)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	rssi_result	ADC result after conversion of the RSSI output (rx_rssi) in RSSI-RX Mode 1 (see "7.1 RSSI Threshold" on page 36)	R	00000

***Table 10-37* • ADC_PEAK (Address 0x38)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	adc_peak	ADC peak value over the last $2^{pow\_n\_conv}$ conversions in ADC mode	R	00000

***Table 10-38* • ADC_AVG (Address 0x39)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	adc_avg	ADC average value over the last $2^{pow\_n\_conv}$ conversions in ADC mode	R	00000

***Table 10-39* • ADC_CTL5 (Address 0x83)**

Bit	Bit Definition	Description	Type	Reset Value
7:4	–	<Reserved>	R	0000
3	skip_pd_search	In RSSI-RX Mode 1, setting this bit high disables the peak detector measurement in the **RSSI_SEARCH** state. This option is disabled by default.	R/W	0
2:0	rssi_pow_n_conv	Used in RSSI-RX mode. Determines the number of conversions used for averaging the RSSI measurements in the **RSSI_SEARCH** state and **RSSI_MONITOR** state in RSSI-RX Mode 1. • 000: 1 conversion • 001: 2 conversions • 010: 4 conversions • 011: 8 conversions • 100: 16 conversions • 101: 32 conversions • 110: 64 conversions • 111: 128 conversions	R/W	000

Note: For recommended initial register setting, see "Recommended Value" column of Table 10-1 on page 62.

***Table 10-40* • ADC_RSSI_AVG (Address 0x84)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	rssi_avg	Used in RSSI-RX mode. At the completion of the DC restore process when auto_dc_res goes low in RSSI-RX Mode 1, the last RSSI measurement stored in the RX_RSSI_RESULT register is saved into *rssi_avg*. The value saved is the average RSSI calculated in the **RSSI_MONITOR** state; in the application the auto_dc_res signal goes low only in the **RSSI_MONITOR** state.	R	00000

10.8 MAC Registers

***Table 10-41* • MAC_CTL1 (Address 0x09)**

Bit	Bit Definition	Description	Type	Reset Value
7	rssi_retry_en	RSSI retry enable.When set, the MAC stays in receive when the wanted signal goes below the RSSI threshold in bidirectional mode, instead of switching to transmit. The retry can also occur on pream_timeout if enabled. In both cases, the retry can occur only if the trigger condition occurs before frame sync is found. If *rssi_sync_abort_dis* is set high in the MAC_CTL4 register, then the radio does not restart on a loss of RSSI after the frame sync is detected. (Refer to Figure 7-1 on page 38 for details.)	R/W	0
6	multi_pkt_en	Enable multipacket mode. When set, the MAC transfers multiple packets in either receive or transmit. This bit is set low for single packet transmit or single packet receive. This bit must be high for bidirectional operation.	R/W	0
5	auto_txrx_en	Enable auto TX-RX RF control; allows the MAC to control the analog section for automatic packet transfers	R/W	0
4	tx_first	Transmit first in bidirectional mode	R/W	0
3	auto_off	Enable auto shutdown; enables autoreset of the MAC if no RSSI is present	R/W	0
2	transmit_en	Enable transmit operations	R/W	0
1	receive_en	Enable receive operations	R/W	0
0	port_en	Enable the MAC; when 0, performs a synchronous reset to the MAC	R/W	0

***Table 10-42* • MAC_CTL2 (Address 0x0A)**

Bit	Bit Definition	Description	Type	Reset Value
7	white_en	Enable whitening in TX operation and dewhitening in RX operation	R/W	0
6	pream_sel[0]	LSB of *pream_sel[1:0]*; together bits [1:0] determine expected received preamble toggle rate divider (that is, 1, 1/2, 1/4) relative to the post-detection filter bit rate. • 00: 0101010101010101 • 01:0011001100110011 • 10: Not supported • 11: Not supported The upper bit is not connected to the transmitter. The bit *pream_sel[1]* is located in register MAC_CTL4. For TX: • 0: preamble pattern of 8'b01010101 and integration period of 12 sys_clk • 1: preamble pattern of 8'b00110011 and integration period of 24 sys_clk	R/W	1
5	rx_polarity_inv	Invert polarity of received data	R/W	0
4	tx_always	Enables continuous TX of packets, with no TXRX_CMD activity	R/W	0
3:2	–	<Reserved>	R	00
1	rx_cnt_en	Enable bit-count mode for receive operation	R/W	0
0	tx_cnt_en	Enable bit-count mode for transmit operation	R/W	0

***Table 10-43* • MAC_CTL3 (Address 0x3B)**

Bit	Bit Definition	Description	Type	Reset Value
7:2	–	<Reserved>	R	000000
1	sync_always	Send sync pattern continuously in TX operation	R/W	0
0	–	<Reserved>	R	0

***Table 10-44* • PCM_CTL (Address 0x3C)**

Bit	Bit Definition	Description	Type	Reset Value
7:4	–	<Reserved>	R	0000
3	pcm_wide_sync	PCM wide sync: • 0: Narrow • 1: Wide	R/W	0
2	pcm_sync_inv	PCM sync invert: • 0: Normal • 1: Invert	R/W	0
1	pcm_clk_inv	PCM clock invert: • 0: Normal • 1: Invert	R/W	0
0	pcm_mode_sel	PCM mode select: • 0: SPI • 1: PCM	R/W	0

***Table 10-45* • FRM_SIZE (Address 0x3D)**

Bit	Bit Definition	Description	Type	Reset Value
7	–	<Reserved>	R	0
6:0	frame_size	PCM frame size in bits	R/W	0100000

***Table 10-46* • PLL_DELAY1 (Address 0x3F)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	pll_delay[7:0]	PLL start-up delay, LSB. *Note: It is recommended that the default value (or reset value) be used. Do not write to this register.*	R/W	01110100

***Table 10-47* • PLL_DELAY2 (Address 0x40)**

Bit	Bit Definition	Description	Type	Reset Value
7:2	–	<Reserved>	R	000000
1:0	pll_delay[9:8]	PLL start-up delay, MSB *Note: It is recommended that the default value (or reset value) be used. Do not write to this register.*	R/W	01

***Table 10-48* • IDLE_DELAY (Address 0x41)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	idle_cnt	Transmitter start-up delay. *Note: It is recommended that the default value (or reset value) be used. Do not write to this register.*	R/W	00010011

***Table 10-49* • PA_DELAY (Address 0x42)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	pwr_amp_cnt	TX power amplifier turn-on delay. *Note: It is recommended that the default value (or reset value) be used. Do not write to this register.*	R/W	00100101

***Table 10-50* • TX_DELAY (Address 0x43)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	tx_delay_cnt	TX preamble start delay. *Note: It is recommended that the default value (or reset value) be used. Do not write to this register.*	R/W	01111100

***Table 10-51* • SLO_DELAY (Address 0x44)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	slo_delay_cnt	TX PLL slow delay. *Note: It is recommended that the default value (or reset value) be used. Do not write to this register.*	R/W	01000100

***Table 10-52* • RSSI_DELAY (Address 0x45)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	rx_rssi_cnt	Receiver RSSI start delay. *Note: It is recommended that the default value (or reset value) be used. Do not write to this register.*	R/W	00111000

***Table 10-53* • RX_DELAY (Address 0x46)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	rx_delay_cnt	When ***not*** in preamble detect mode (that is, when MAC_CTRL4[5]=0): • RX DC restore off delay. This is the time the auto_dc_res is asserted. When set to 0, auto_dc_res is asserted until frame sync. When in preamble detect mode (that is, when MAC_CTRL4[5]=1): • The preamble timeout (in bytes). The default in this case is 10956µs. When 0, preamble timeout is disabled.	R/W	11111111

***Table 10-54* • TX_CNT1 (Address 0x47)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	tx_cnt[7:0]	Transmit bit count – LSByte	R/W	11111111

***Table 10-55* • TX_CNT2 (Address 0x48)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	tx_cnt[15:8]	Transmit bit count – MSByte	R/W	11111111

***Table 10-56* • RX_CNT1 (Address 0x49)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	rx_cnt[7:0]	Receive bit count – LSByte	R/W	11111111

***Table 10-57* • RX_CNT2 (Address 0x4A)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	rx_cnt[15:8]	Receive bit count – MSByte	R/W	11111111

***Table 10-58* • PREAM_CNT (Address 0x51)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	pream_cnt	Preamble byte count. The value is the number of preamble bytes; this is the time period for which the preamble is transmitted. See "9.3 Timing Delays" on page 44 for timing diagrams, that show when *pream_cnt* begins.	R/W	00011010

***Table 10-59* • SYNC_PAT1 (Address 0x4B)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	sync_ptrn[7:0]	Sync pattern – LSByte. (Bit [0] is last bit sent.)	R/W	10011010

***Table 10-60* • SYNC_PAT2 (Address 0x4C)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	sync_ptrn[15:8]	Sync pattern – second byte	R/W	00101001

***Table 10-61* • SYNC_PAT3 (Address 0x4D)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	sync_ptrn[23:16]	Sync pattern – third byte	R/W	10001111

***Table 10-62* • SYNC_PAT4 (Address 0x4E)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	sync_ptrn[31:24]	Sync pattern – fourth byte	R/W	01001101

***Table 10-63* • SYNC_PAT5 (Address 0x4F)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	sync_ptrn[39:32]	Sync pattern – MSByte. (Bit [39] is first bit sent.)	R/W	10110001

***Table 10-64* • PREAM_LOCK_CNT (Address 0x52)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	pream_lock_cnt	Preamble lock byte count. Period for which the DC-restore/AFC is enabled after the preamble is detected. The default gives a DC-restore/AFC enable time of approximately 757µs.	R/W	00010010

***Table 10-65* • MAC_DOUT0 (Address 0x5D)**

Bit	Bit Definition	Description	Type	Reset Value
7	pdf_fir_bypass	Bypass FIR filters of data recovery	R/W	0
6	pdf_thresh_bypass	Bypass threshold in the post-detection filter (see Note)	R/W	0
5	–	<Reserved>	R	0
4:0	dout0_sel	Select output for DOUT0; see Table 10-95 on page 87	R/W	00000

***Table 10-66* • MAC_DOUT1 (Address 0x5E)**

Bit	Bit Definition	Description	Type	Reset Value
7	spi_out_dis	Disable SPI_CLK and SPI_DATA_OUT	R/W	0
6:5	–	<Reserved>	R	00
4:0	dout1_sel	Select output for DOUT1; see Table 10-95 on page 87	R/W	00000

***Table 10-67* • MAC_DOUT2 (Address 0x7F)**

Bit	Bit Definition	Description	Type	Reset Value
7:4	dout1b_sel	Selects output of DOUT1; see Table 10-96 on page 88. To select a signal to DOUT1 from Table 10-96, *dout1_sel[4:0]* must be zero.	R/W	0000
3:0	dout0b_sel	Selects output of DOUT0; see Table 10-96 on page 88. To select a signal to DOUT0 from Table 10-96, *dout0_sel[4:0]* must be zero.	R/W	0000

***Table 10-68* • MAC_CTL4 (Address 0x80)**

Bit	Bit Definition	Description	Type	Reset Value
7	–	<Reserved>	R	0
6	pream_sel[1]	MSB of *pream_sel[1:0]*. Together bits [1:0] determine expected received preamble toggle rate divider. See MAC_CTL2 register for details.	R/W	0
5	pream_det_mode	Enables preamble detection	R/W	0
4	–	<Reserved>	R	0
3	rssi_sync_abort_dis	When high, disables RSSI packet end after frame sync	R/W	0
2:0	–	<Reserved>	R	000

***Table 10-69* • STATUS_REG (Address 0x82)**

Bit	Bit Definition	Description	Type	Reset Value
7	din0	Value on DIN0	R	0
6	dout1	Value on DOUT1	R	0
5	dout0	Value on DOUT0	R	0
4	radio_off	• 0: PA output off • 1: PA output on	R	0
3	pa_tx_en	• 0: Radio/PLL enabled • 1: Radio/PLL disabled	R	0
2	arm_corr	Waiting for frame sync	R	0
1	rx_rssi_high	• 0: RSSI below threshold • 1: RSSI equal to or above threshold	R	0
0	txrx_sel	• 1: TX • 0: RX	R	0

10.9 Synthesizer Registers

Table 10-70 **• SYNTH_CH_MDIV (Address 0x5F)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	ch_m_div	M counter value — number of times the prescaler counts to 16 within one phase comparison period. The M value must be written first.	R/W	10110101

Table 10-71 **• SYNTH_CH_ADIV (Address 0x60)**

Bit	Bit Definition	Description	Type	Reset Value
7	ch_lo_ctl	Control whether the local oscillator (in RX) is set 606kHz above the wanted channel or 606kHz below the wanted channel. The choice of LO above or below channel is influenced by where the possible interferers might be and the fact that the ZL70251 does not include image rejection. • 1: LO above channel • 0: LO below channel	R/W	0
6	vco_low_range	Enable low VCO frequency operation	R/W	0
5:0	ch_a_div	A counter value — number of times the prescaler counts to 17 within one phase comparison period. The A divider should be set greater than or equal to 5. The A counter should be written second (after the M value). When the A value is written, both the A and M values are sent to the synthesizer simultaneously.	R/W	000111

Table 10-72 **• SYNTH_CTL (Address 0x61)**

Bit	Bit Definition	Description	Type	Reset Value
7:3	–	<Reserved>	R	00000
2	tx_mode_en	Enable TX mode: • 1: TX mode. • 0: RX mode (manual control via system bus). Should be low for any RX mode and during VCO frequency trimming for RX mode.	R/W	1
1:0	–	<Internal bits; always write binary 11 to these bits>	R	11

Table 10-73 **• MOD_PHASE_CNT (Address 0x63)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	mod_phase_cnt	Modulator phase count	R/W	10111

10.10 Clock Generator Registers

Table 10-74 **• SYS_CLK_DIV (Address 0x65)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	sys_clk_div	Set the divide ratio from the master clock (24.576MHz) to the system clock, which runs the control interface and other system functions	R/W	10110

Table 10-75 **• CLK_OUT_DIV (Address 0x66)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	clk_out_div	Set the divide ratio from the master clock (24.576MHz) to the CLK_OUT, which is an output from the ZL70251 IC to be used as a reference for other chips	R/W	11000

10.11 Interrupt Controller Registers

Table 10-76 **• IRQ_EN1 (Address 0x07)**

Bit	Bit Definition	Description	Type	Reset Value
7	–	<Reserved>	R	0
6	sync_detect_irq_en	Enable synchronization detect interrupt	R/W	0
5	trim_done_irq_en	Enable trim done interrupt	R/W	0
4	trim_fail_irq_en	Enable trimming and tuning process failed interrupt	R/W	0
3	adc_done_irq_en	Enable ADC done interrupt	R/W	0
2	rssi_nosig_irq_en	Enable RSSI-RX no signal interrupt	R/W	0
1	rssi_thresh_irq_en	Enable threshold interrupt for the RSSI output (rx_rssi)	R/W	0
0	–	<Reserved>	R	0

Table 10-77 **• IRQ_EN2 (Address 0x06)**

Bit	Bit Definition	Description	Type	Reset Value
7:4	–	<Reserved>	R	0000
3	rx_done_irq_en	Enable receive complete interrupt	R/W	0
2	tx_done_irq_en	Enable transmit complete interrupt	R/W	0
1	pll_lock_err_irq_en	Enable PLL error interrupt	R/W	0
0	sync_err_irq_en	Enable interrupt for no synchronization pattern found during receive period	R/W	0

***Table 10-78* • IRQ1 (Address 0x69)**

Bit	Bit Definition	Description	Type	Reset Value
7	–	<Reserved>	R	0
6	sync_detect_irq	Synchronization detect interrupt	CoR	0
5	trim_done_irq	Trim done interrupt	CoR	0
4	trim_fail_irq	Trimming and tuning process failed interrupt	CoR	0
3	adc_done_irq	ADC done interrupt	CoR	0
2	rssi_nosig_irq	RSSI-RX no signal interrupt	CoR	0
1	rssi_thresh_irq	Threshold interrupt for the RSSI output (rx_rssi)	CoR	0
0	–	<Reserved>	R	0

***Table 10-79* • IRQ2 (Address 0x6B)**

Bit	Bit Definition	Description	Type	Reset Value
7:4	–	<Reserved>	R	0000
3	rx_done_irq	Receive complete interrupt	CoR	0
2	tx_done_irq	Transmit complete interrupt	CoR	0
1	pll_lock_err_irq	PLL error (not locked) at startup of TX/RX interrupt	CoR	0
0	sync_err_irq	No synchronization pattern found during receive period interrupt	CoR	0

***Table 10-80* • RF_STAT (Address 0x6C)**

Bit	Bit Definition	Description	Type	Reset Value
7:6	–	<Reserved>	R	00
5	pll_lock	Lock status of phase lock loop – not latched • 0: Open • 1: Locked	R	0
4	iref_cmp_out	IREF comparator output status – not latched	R	0
3	vco_amp_cmp_out	VCO amplitude comparator output status – not latched	R	0
2	vco_frq_cmp_out	VCO frequency comparator output status – not latched	R	0
1	vco_hi	Above PLL range status – not latched	R	0
0	vco_lo	Below PLL range status – not latched	R	0

10.12 Tune and Trim Registers

Table 10-81 **• AUTO_TRIM_EN (Address 0x6D)**

Bit	Bit Definition	Description	Type	Reset Value
7	–	<Reserved>	R	0
6	fm_det_en_trim	Enable tuning of IF filter and FM detector and Gaussian filter (see Note)	R/W/CoD	0
5	ant_en_trim	Enable tuning of antenna (see Note)	R/W/CoD	0
4	lna_en_trim	Enable tuning of LNA load (see Note)	R/W/CoD	0
3	pd_en_trim	Enable trimming of peak detector offset (see Note)	R/W/CoD	0
2	vco_amp_en_trim	Enable tuning of VCO amplitude (see Note)	R/W/CoD	0
1	vco_frq_en_trim	Enable tuning of VCO frequency (see Note)	R/W/CoD	0
0	iref_en_trim	Enable trimming of IREF (see Note)	R/W/CoD	0

Note: All bits in the AUTO_TRIM_EN register are cleared when the trim_done_irq signal is generated at the end of the current tuning/trimming.

Table 10-82 **• CONT_TRIM_EN (Address 0x6E)**

Bit	Bit Definition	Description	Type	Reset Value
7:2	–	<Reserved>	R	000000
1	incdec_cnt_en	Manual enable of the continuous trimming of the VCO. The adjustment period is controlled by *vco_frq_cnt[7:0]*. This enable is primarily used during the procedure for VCO frequency tuning in TXPAON mode.	R/W	0
0	incdec_modetrans_en	Enables the continuous trimming of the VCO by one LSB at the end of every TX or RX packet.	R/W	0

Table 10-83 **• VFT_RX_L (Address 0x6F)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	vco_frq_rx[7:0]	VCO frequency tune LSB value for the RX mode	R/W	11111111

Table 10-84 **• VFT_RX_H (Address 0x70)**

Bit	Bit Definition	Description	Type	Reset Value
7:3	–	<Reserved>	R	00000
2:0	vco_frq_rx[10:8]	VCO frequency tune MSB value for the RX mode	R/W	100

Table 10-85 **• VFT_PAOFF_L (Address 0x71)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	vco_frq_txpaoff[7:0]	VCO frequency tune LSB value for the TX mode (with modulation off) with the power amplifier off (only bias on)	R/W	11111111

***Table 10-86* • VFT_PAOFF_H (Address 0x72)**

Bit	Bit Definition	Description	Type	Reset Value
7:3	–	<Reserved>	R	00000
2:0	vco_frq_txpaoff[10:8]	VCO frequency tune MSB value for the TX mode (with modulation off) with the power amplifier off (only bias on)	R/W	100

***Table 10-87* • VFT_PAON_L (Address 0x73)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	vco_frq_txpaon[7:0]	VCO frequency tune LSB value for the TX mode (with modulation off) with the power amplifier on	R/W	11111111

***Table 10-88* • VFT_PAON_H (Address 0x74)**

Bit	Bit Definition	Description	Type	Reset Value
7:3	–	<Reserved>	R	00000
2:0	vco_frq_txpaon[10:8]	VCO frequency tune MSB value for the TX mode (with modulation off) with the power amplifier on	R/W	100

***Table 10-89* • VFT_L (Address 0x75)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	vco_frq[7:0]	VCO frequency tune LSB value at output of multiplexer. This register combined with VFT_H holds the VCO frequency trim value for the mode (one of the three in the previous six registers) that the chip is currently in.	R/W	11111111

***Table 10-90* • VFT_H (Address 0x76)**

Bit	Bit Definition	Description	Type	Reset Value
7:3	–	<Reserved>	R	00000
2:0	vco_frq[10:8]	VCO frequency tune MSB value at output of multiplexer	R/W	100

***Table 10-91* • VCO_FRQ_CNT (Address 0x77)**

Bit	Bit Definition	Description	Type	Reset Value
7:0	vco_frq_cnt	Counter value used for the increment/decrement tuning of the VCO frequency. Multiplying this count value by four sys_clk periods gives the time used between VCO frequency trim updates (if selected).	R/W	00101010

***Table 10-92* • LNA_BEST_ADC (Address 0x7A)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	lna_best_adc	Best (highest) value from the ADC during the latest LNA tuning. For test or debug only.	R	00000

***Table 10-93* • ANT_BEST_ADC (Address 0x7B)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4:0	ant_best_adc	Best (highest) value from the ADC during the latest antenna tuning. For test or debug only.	R	00000

***Table 10-94* • VCO_CTL (Address 0x7C)**

Bit	Bit Definition	Description	Type	Reset Value
7:5	–	<Reserved>	R	000
4	vref_nom	VREF to VCO frequency trim comparator (see Note 1)	R/W	0
3	vref_low	VREF to VCO frequency trim comparator (see Note 1)	R/W	0
2:0	vco_frq[13:11]	VCO frequency control	R/W	110

Notes:

1. *If vref_low is 0 and vref_nom is 0, then Vvco is 611mV (high threshold and default).*
   If vref_low is 0 and vref_nom is 1, then Vvco is 509mV (nominal).
   If vref_low is 1 (and vref_nom is any value), then Vvco is 400mV (low).
   Initial VCO frequency should be trimmed with 509-mV reference.

10.13 Data Port Test Modes

Use the values in Table 10-95 to select which signal is output to the DOUT0 and DOUT1 pins. Values are valid for MAC_DOUT0 and MAC_DOUT1 registers; see Table 10-65 on page 80 and Table 10-66 on page 80.

***Table 10-95* • Data Port Test Modes**

Value	Signal	Value	Signal
0x00	–	0x10	auto_dc_res
0x01	txrx_sel	0x11	arm_bit_sync
0x02	rx_en	0x12	arm_correlator
0x03	tx_en	0x13	sync_detect
0x04	pll_lock_err	0x14	sync_err
0x05	white_enbl	0x15	rx_done
0x06	clk_en	0x16	rssi_en
0x07	xmtr_en	0x17	rssi_running
0x08	pll_slow	0x18	rssi_monitoring
0x09	tx_done	0x19	rx_rssi_high
0x0A	pdf_msbn_out	0x1A	adc_done
0x0B	pdf_rx_data	0x1B	rssi_nosig
0x0C	rx_input_data	0x1C	rx_pd_thresh
0x0D	rx_spi_data	0x1D	rx_rssi_thresh
0x0E	bit_lock	0x1E	trim_ctrl
0x0F	rcvr_en	0x1F	tt_adj_frq_vco_trim

The register MAC_DOUT2 (see Table 10-67 on page 80) is used to determine what signal is sent out on DOUT1 and DOUT0. The same signals available for DOUT0, shown in Table 10-96, are available for DOUT1. This allows any two signals to be output for test on the test output bits, DOUT1 and DOUT0.

Table 10-96* • Selections for *dout0b_sel* and *dout1b_sel

Value	Signal	Source
0x00	1'b0	N/A
0x01	radio_off	Timing control
0x2	osc_en	SSI
0x3	pream_detected	RX control
0x4	pream_timeout	RX control
0x5	pream_det_en	RX control
0x6	dcres_ctrl_en	RX control
0x7	txrx_cmd_2q	Timing control
0x8	mac_rx_rst	RX control
0x9	1'b0	N/A
0xA	1'b0	N/A
0xB	1'b0	N/A
0xC	1'b0	N/A
0xD	1'b0	N/A
0xE	1'b0	N/A
0xF	1'b0	N/A

A – References

Document No.	Document Title
	FCC Part 15 and the European pr ETS 300-220 regulatory documentation
	Mil-Std-883 Method 3015
EN301 357 – 1	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Cordless audio devices in the range 25 to 2000 MHz; Consumer radio microphones and in-ear monitoring systems operating in the CEPT harmonized band 863 to 865 MHz; Part 1: Technical characteristics and Test methods
EN301 357 – 2	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Cordless audio devices in the range 25 to 2000 MHz; Consumer radio microphones and in-ear monitoring systems operating in the CEPT harmonized band 863 to 865 MHz; Part 2: Harmonized EN under article 3.2 of the R&TTE Directive
EN301 489 – 1	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Electromagnetic Compatibility (EMC) (EMC) standards for radio equipment and services; Part 1: Common technical requirements
EN301 489 – 9	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Electromagnetic Compatibility (EMC) (EMC) standards for radio equipment and services; Part 9: Specific conditions for wireless microphones, similar Radio Frequency (RF) audio link equipment, cordless audio and in-ear monitoring devices

B – Glossary of Acronyms

ADC	Analog to Digital Converter
AFC	Automatic Frequency Control
ARQ	Automatic Repeat Request
BER	Bit Error Ratio
CCA	Clear Channel Assessment
CSMA	Carrier Sense Multiple Access
CW	Continuous Wave
DAC	Digital to Analog Converter
DC	Direct Current
EIRP	Effective Isotropic Radiated Power
EMC	Electro-Magnetic Compatibility
FIFO	First In First Out (memory)
FSK	Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
IF	Intermediate Frequency
LBT	Listen Before Talk
LO	Local Oscillator
MAC	Media Access Controller (most of the ZL70251 digital section)
PLL	Phase Locked Loop
PN	Pseudo-random Number
PPM	Parts per million
RSSI	Received Signal Strength Indicator
RX	Receive
TX	Transmit
VCO	Voltage Controlled Oscillator

Note: REGISTER NAMES and *bit words* that are referenced in this document are defined in section "10 – System Memory Map" on page 60 and its subsections. **STATES** are defined in "7.1.4 RSSI-RX Mode 1 State Machine" on page 38. Many PIN NAMES and signal names referenced in this document are defined in the ZL70251 Data Sheet.

C – List of Changes

The following table lists substantive changes that were made in the ZL70251 Programmer User's Guide (146499).

Revision	Changes	Page
Revision 2, Production (February 2014)	In chapter "1 – Introduction", corrected text to refer to ZL70251 ADK.	8
	In step 3 of the example in "4.1 A and M Value Calculation", the binary representation for the A value is six bits.	12
	Made changes to Table 6-1, including: • Removed F (Factory) for current reference and peak detector offset trims. • Added table note 1 regarding calibrations to be done when a frequency change occurs. Removed three table notes and/or reworded remaining two notes. References in "Notes" column were added, deleted, and changed. • Merged the three rows for SAR VCO frequency TXPAOFF mode and VCO amplitude into a single row, renumbering subsequent trims. • Added row for FSK frequency separation trim, renumbering subsequent trims. • Rename trim to *transmitter output power* trim.	15
	In "6.2 Tune and Trim Sequence", added paragraph about calibration sequence and IRQ1 register.	16
	In "6.3 Tune and Trim Setup", removed sentences about IRQ1 register.	16
	In "6.3 Tune and Trim Setup" through "6.14 Enable Automatic Trimming of the VCO", all procedures were reorganized into tabular format for ease of use. Newly added tables include Table 6-2 through Table 6-16. Some of the procedures underwent significant rewrites to accommodate the tabular format.	16 to 34
	In "6.4 Current Reference Trim", minor edit to second paragraph (added "trace").	16
	In "6.6 VCO Frequency and Amplitude Tuning", merged the SAR VCO frequency tune TXPAOFF mode and the VCO amplitude trim into a single step with four substeps. Also deleted four sentences and added in their place a recommendation to do calibrations upon change of frequency.	19
	Rewrote "6.6.1 Frequency Band Selection", including replacing Table 6-5 with a new table.	20
	Merged the SAR VCO frequency tune TXPAOFF mode and the VCO amplitude trim into a single procedure (renumbering subsequent sections): • Deleted former "6.6.2 SAR VCO Frequency Tune TXPAOFF Mode" and "6.6.3 VCO Amplitude Trimming" sections. • Replaced them with a single section "6.6.2 SAR VCO Frequency Tune TXPAOFF Mode and VCO Amplitude Trim". Note minor text edits to use new name for renamed *transmitter output power* trim.	22
	In "6.6.3 VCO Frequency Tune TXPAON Mode", replaced notes above procedure.	23
	In "6.6.4 SAR VCO Frequency Tune RX Mode", removed note above procedure.	25
	In "6.8 Antenna Tune" and "6.9 LNA Load Tune", made minor text edit to use new name for renamed *transmitter output power* trim.	26 to 28

Revision	Changes	Page
Revision 2, continued	Added section "6.11 FSK Frequency SeparationModulation Index Trim".	32
	Moved "6.13 Transmitter Output Power Trim" to be after "6.12 Restore Register Values", renumbering both sections. Both paragraphs were also modified as follows: • "6.13 Transmitter Output Power Trim" was modified to change the trim name to *transmitter power output trim* (and a detailed procedure table was added as previously noted). The footnote was moved to the bottom of the tabular procedure and also modified to clarify. • "6.12 Restore Register Values" was completely rewritten including the addition of Table 6-14.	33 to 34
	Minor text edits in "6.15 LNA Gain" to clarify.	35
	Chapter "7 – Packet Reception" was renamed and reorganized as follows: added an introductory paragraph, added section "7.2 Preamble Detection", and reorganized existing sections (demoting headings and moving a section to new chapter "8 – Channel Monitoring").	36 to 39
	Replaced first sentence of "7.1 RSSI Threshold" with new paragraph.	36
	Added "equal to or" and made minor text changes to paragraphs "7.1.1 Dynamic Calibration of the RSSI Threshold" through "7.1.3 Terminating Packet (below threshold)".	36 to 37
	Added new chapter "8 – Channel Monitoring" to accommodate new section "8.1 Listen Before Talk (LBT)" and section "8.2 RSSI Measurement" (modified and moved from chapter "7 – Packet Reception"). Subsequent chapters were renumbered.	40
	Rewrote bullets in "9.4.1 Transmit Startup in Bit-Count Mode" to eliminate redundancy or conflicts with "9.5 Packet Transfer Operations".	45
	Modified three timing diagrams, Figure 9-3, Figure 9-4, and Figure 9-5, to show pll_slow signal and SLO_DELAY value.	45 to 46
	Changed *SPI* to *SPI bus* in "9.4.3 Bidirectional Streaming in Bit-Count Mode" and "9.4.4 Bidirectional Streaming in Non-Bit-Count Mode".	47 to 47
	Added paragraph under "9.5 Packet Transfer Operations".	52
	In "9.5.1 Transmit Operations" through "9.5.4 Transmit or Receive Operation Abort", all procedures were reorganized into tabular format for ease of use. Newly added tables include Table 9-2 through Table 9-12. Some of the procedures underwent significant rewrites to accommodate the tabular format.	52 to 59
	Corrected text to refer to ZL70251 memory map in "10 – System Memory Map" introduction paragraphs.	60
	Clarified instructions for bitwise registers in "10 – System Memory Map" introduction paragraphs.	60
	In Table 10-1: • Changed reset value at address 0x02 (CHIP_IDL) to reflect current hardware release. • Added recommended initialization values at addresses 0x12 (RF_CTL2) and 0x22 (INTERNAL34). • Removed recommended initialization value at address 0x7C (VCO_CTL). • Added new rows for addresses 0x22, 0x3B, 0x4B, 0x4C, 0x4D, 0x4E, 0x4F. • Renamed registers at address 0x31, 0x32, and 0x33 to mark them as internal.	62

Revision	Changes	Page
Revision 2, continued	In "10.2 Control Interface Registers", added Table 10-4 and Table 10-5 for CHIP_IDL and CHIP_IDH, respectively.	66
	In Table 10-11, corrected reset value for RF_TRIM_EN[7:1].	67
	Added wording to Table 10-12 regarding recommended value for RF_CTL2[7:1] and changed *Type* to *R/W*.	67
	In Table 10-13: • Minor text edits to use new name for renamed *transmitter output power* trim. • Modified note.	68
	In Table 10-14: • Added a definition and description for the *half_band* bit at RF_CTL7[5]. • Added wording regarding using reset value for RF_CTL7[4] and changed *Type* for that bit to *R/W*.	68
	In "10.6 Trim Registers", added Table 10-19 for INTERNAL34.	69
	In Table 10-29, removed erroneous note regarding recommended initialization values.	72
	In "10.7 ADC Registers", added Table 10-31, Table 10-32, and Table 10-33 for INTERNAL49, INTERNAL50, and INTERNAL51, respectively.	73
	In Table 10-42, added a definition and description for the *tx_always* bit at MAC_CTL2[4].	76
	In "10.8 MAC Registers", added Table 10-43 for MAC_CTL3 and added Table 10-59 through Table 10-63 for SYNC_PAT1 through SYNC_PAT5, respectively.	76, 79, 79
	In Table 10-53, rewrote description.	78
	In Table 10-58, modified description to refer to "9.3 Timing Delays".	79
	In Table 10-67, corrected cross-references to refer to appropriate table.	80
	In Table 10-68, removed erroneous note regarding recommended initialization values.	80
	In Table 10-69, added a definition and description for the *din0* bit at STATUS_REG[7].	81
	Added wording to Table 10-72 regarding using reset value for SYNTH_CTL[1:0].	82
	Removed *_stat* suffix from all bit names in the RF_STAT register (Table 10-80) for consistency with the ADK.	84
	In Table 10-82, rewrote descriptions to clarify.	85
	In Table 10-94, corrected reset value for VCO_CTL[7:5] and removed note regarding recommended initial register setting.	87
	Updated appendix "B – Glossary of Acronyms".	90
	Updated appendix "D – Product Support".	94
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