Designing an 8-port PoE System with PD39100 & PD69108 (802.3af/802.3at Compliant)

APPLICATION NOTE

Introduction

This application note provides detailed information and circuitry design guidelines for implementing an 8-port Power over Ethernet (PoE) system, based on Microsemi's™ PD69108 8-channel PoE manager and PD39100 PoE Controller.

For communicating with the hosting system either an UART or an I^2C interface is optional (UART is included in this application note).

This document enables designers to integrate PoE capabilities into an Ethernet switch, as specified in IEEE802.3af and IEEE802.3at standards.

PD69108 8-port PoE manager implements real time functions as specified in IEEE 802.3af and IEEE802.3at standards, including detection, classification, port-status monitoring, and system level activities such as power management and MIB (Management Information Base) support for system management. PoE manager is designed to detect and disable disconnected PDs (Powered Devices), using DC disconnection methods as specified in the standard.

Applicable Documents

- IEEE 802.3af-2003 standard, DTE Power via MDI
- IEEE802.3at-2009 standard, DTE Power via MDI
- PD69108 datasheet, catalog number 06-0057-058
- PD39100 datasheet

Features

- IEEE802.3af-2003 compliant
- IEEE802.3at-2009 compliant, including two-event classification
- Controls up to 8 PoE ports (one PD69108/PD69104)
- Pre-Standard / Capacitor Detection
- Detection of Cisco devices
- Supports both UART and I2C interfaces to Host CPU
- 16 emergency power banks support using four discrete lines connected directly to PD69108
- Power management for up to 8 ports
- Programmable over-voltage and under-voltage
- 16 predefined power budget control
- Direct LED driving for up to 8 ports (LED 0 to7)
- PoE Max System LED direct driving (LED8)
- Software download via I^2C or UART
- System and port measurements
- Detailed port status
- Thermal protection and monitoring
- Programmable temperature alarm limit
- Forced power for system testing
- System reset
- Port power limit setting
- Port and Leds matrix
- Port priority
- Automatic detection of PoE device type
- RoHS compliant

PoE System

The system described here is designed to support a low cost 8-port PoE switch.

The following figure demonstrates a PoE system board which can be easily integrated on top of a switch, providing the capability to add any PoE application while using a daughter board applications (refer to Figure 1).

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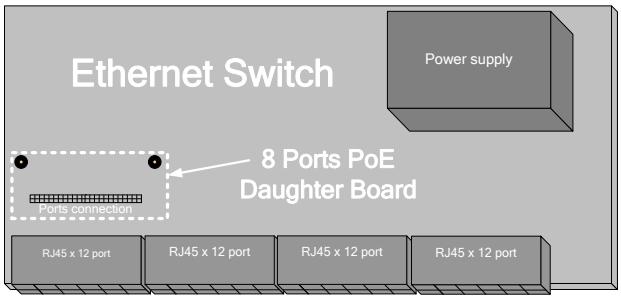

Figure 1: PoE Daughter Board Example

General Description

The circuit includes the following blocks (Figure 2):

- PoE circuit for 8 ports based on one PD69108
- PD39100 Controller circuit, used to initialize, control and monitor PD69108 via an internal ESPI (isolated) bus.

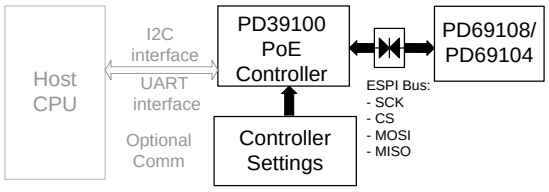

Figure 2: 8-Port Configuration

General Circuit Description

The 8-port configuration for the PoE system shown in Figure 2, comprises one PoE managers circuits (PD69108) functioning as a slave with a PoE controller (PD39100).

PoE controller utilizes ESPI bus to control PD69108. PoE operations are automatically performed by PoE manager circuits, while PoE controller performs power management and other tasks.

Communication Interfaces

Communication between Host CPU and local PoE controller is optional and may be based on UART or I^2C interface. For more information, refer to *Serial Communication Protocol User Guide, catalog number 06-0032-056*.

ESPI Bus

The Enhanced Serial Peripheral Interface (ESPI) bus used for internal communication includes the following lines:

- MOSI (Master Out/Slave In) allows PoE Controller to communicate with PD69108s.
- MISO (Master In/Slave Out) allows PD69108s to communicate with PoE controller.
- SCK is a serial clock generated by the controller.
- CS (Chip Select) is utilized by PoE controller to transmit data to PD69108.

Control Signals

- **xReset_IN** – A control signal driven by Host CPU to reset the PoE system – Active low
- **xDisable_ports** – control signal driven by Host CPU to disables all PoE ports at once – Active low
- **Power Management Control** – PD69108s PG 0 to 3 Input Signals – used for configuring Total PoE Power Budget

Indications

- **LED 0 to 7** – Direct LED drive is included per port, to indicate port PoE status (see PD39100 datasheet).
- **LED_SYS_OK** – Direct LED drive for System Power status indication is included, to indicate PoE power status (see PD39100 datasheet).

Communication Flow

- Host CPU use a Serial Communication protocol to PoE controller (PD39100).
- PoE Controller converts Serial Communication Protocol to ESPI Communication and sends it via isolated ESPI lines to PD69108.

Main Supply

The PoE system operates within a range of 44 to 57 VDC (802.3at port's range is 50 to 57 VDC). To comply with UL SELV regulations, maximum output voltage should not exceed 60VDC.

Grounds

Several grounds are used in the system.

- PoE Domain Analog
- PoE Domain Digital
- Chassis
- Host Domain Floating

Digital and analog grounds are electrically same ground. However, to reduce noise coupling, grounds are physically separated and connected only at a single point.

Chassis ground is connected to switch's chassis ground. This ground plane should be 1500 V_{rms} isolated from the PoE circuitry.

PoE controller relates to Host domain floating ground which is isolated for PoE domain grounds.

Grounding is further detailed in *Application Note 186, catalog number 06-0081-080 for Layout Design Guidelines*.

5 V_{DC} and 3.3 V_{DC} Regulators

PD69108 has a $5V_{DC}$ regulator and a $3.3V_{DC}$ regulator providing up to 6mA each. This current is used for powering other external components in the PoE domain; those components must also be isolated by $1500V_{rms}$ from switch circuitry.

Additional Circuit Description

PoE Controller Circuitry

1.2 Mb/s ESPI communication interface is used between PD39100 and PD69108, and as the communication interface with Host CPU via UART or I^2C protocol.

For its operation, PoE controller requires stable, filtered power that comes from the host (3_3V_cpu); hence, a number of components are included in the design:

- **C12-C16, R29, and C20-C21:** Used for filtering these power sources.

LED Drive Support

Direct LED drive is included to support PoE port status indication (see LED0 to LED7 signals).

An Additional Direct LED drive is included for System Power status indication (see LED_SYS_OK signal in PD39100 datasheet).

Important note:

1. Maximum current each LEDx pin can sink is **9mA**. Do not exceed this value in your design.
2. Maximum current LED_SYS_OK pin can push is **9mA**. Do not exceed this value in your design.

PoE Manager Circuitry

PD69108 performs a variety of internal operations and PoE functions, requiring a minimum of external components.

PD69108 Front End Circuitry includes several external components, for handling up to 8 PoE ports.

Reference Current Source

Reference for internal voltages within PD69108 is set by a precision resistor (R54).

Sense Resistors

A 360 mΩ, ±1% sense resistor is connected to each PORT_SENSE pin (R59-R67). This resistor is used to measure port current.

Recommended trace resistance of each sense resistor should be close to 12mΩ. For more information, refer to *Application Note 186, catalog number 06-0081-080 for Layout Design Guidelines*.

Front End and Protection

Each output port includes internal protection circuitry against external discharges that may damage the PD69108.

When any IC experiences input voltage above its absolute maximum rating, it is exposed to damage. Since PoE manager is connected to a high current source, best design practice is to use a protection fuse (See F1-F2, F4-F9) to avoid high current path during PSU over voltage faults. These fuses are also utilized as a current limiting device, operating as specified in IEC 60950-1:2001.

Note: According to IEC 60950-1:2001 these fuses may be avoided in PoE systems with power supply of less than 100W.

Serial Communication Host-Controller

PoE controller can communicate with hosting system using UART or I^2C communication. UART or I^2C communication between Host CPU and PoE controller is managed by setting PoE controller's address. This is done by setting Pin #16, as specified in PD39100 datasheet.

UART Interface

Circuit supports:

- 3.3V (or 5V) TTL level signals
- 19,200 bps
- 8 bit
- No parity
- 1 stop bit
- No flow control

I^2C Interface

PoE Controller can communicate with hosting system using UART or I^2C communication.

I^2C communication between Host CPU and PoE Controller is managed by setting PoE Controller's address. This is done by selecting a value for R51. This resistor sets analog level into pin #16 as specified in the following table:

I^2C Address	Address (hex)	R51 (ohms)	I^2C Address	Address (hex)	R51 (ohms)
#0	UART	NA	#8	0x20	8870
#1	0x4	97600	#9	0x24	6810
#2	0x8	53600	#10	0x28	5230
#3	0xC	35700	#11	0x2C	3920
#4	0x10	25500	#12	0x30	2800
#5	0x14	19100	#13	0x34	1870
#6	0x18	14700	#14	0x38	1020
#7	0x1C	11300	#15	0x3C	324

Note: Host CPU should support clock stretch.

Power Management

Total power consumption of all 8 ports is being controlled and monitored through PD69108 and PD39100.

Default Power limits is determined according to PD69108's Power Good pins (Digital Input pins "PG0 to 3").

Users can configure the total maximum power available for PoE Ports by connecting each of PG Input pins to DGND or DVDD

"0" – Connected to DGND

"1" – Connected to DVDD

This Application Note illustrates a scenario in which all PG pins are grounded. In this specific case, system power would be set to 270W. The 16 predefined power levels are described In the table below:

Total Power level	PG[3:0]
250W	0000
60W	0001
64W	0010
70W	0011
75W	0100
80W	0101
85W	0110
90W	0111
100W	1000
115W	1001
130W	1010
145W	1011
160W	1100
175W	1101
200W	1110
235W	1111

Ground Interface Connection (AGND)

Power supplies ground connector enables the current a path back to the power supply. Ground connection should be capable of carrying all strings currents back to power supplies.

Thermal Design

Design for 802.3at PoE standard should take into account power dissipation of PoE manager and of associated circuitry, and switch's maximal ambient operating temperature. Adequate ventilation and airflow should be part of the design to avoid thermal over-stress on the following issues

Ambient Temperature

Application's thermal design should take into account the temperature derived from switch's power dissipation and from PoE daughter board powered at maximum load.

PD69108

PoE design should ensure PD69108's maximal operating junction temperature (150°C) **is not** exceeded under worst case conditions. Worst case conditions typically involve operation under maximum ambient temperature, output ports fully loaded at 802.3at power and all other unit functions fully operational. *PD69108 datasheet, catalog number 06-0057-058* contains additional thermal characteristics details.

PD39100

Layout considerations should ensure that:

- PD39100 is placed away from potential high temperature spots.
- Maximal case temperature **does not** exceed 85°C under worst case conditions.

Sense Resistors

Each port's front-end circuit has a single sense resistor. Resistor's value should be 360mΩ and should dissipate about 0.19W at 720mA (802.3at maximum load) and 44 mW at 350mA (802.3af maximum load). Resistors traces' resistance needs to be controlled to achieve maximum current accuracy. Heat generated from these resistors contributes to a higher ambient temperature near PD69108. For 802.3at ports, use the following sense resistors types:

Description	SIZE	Mnf.	MAN. PART #
0.360R 1% 0.5 W 200 PPM	1210	Rohm	MCR25JZHFLR360

Note Sense resistor's temperature coefficient of resistance (ppm) should be less than or equal to $\pm 200\ [10^{-6}/^{\circ}C]$.

Schematics

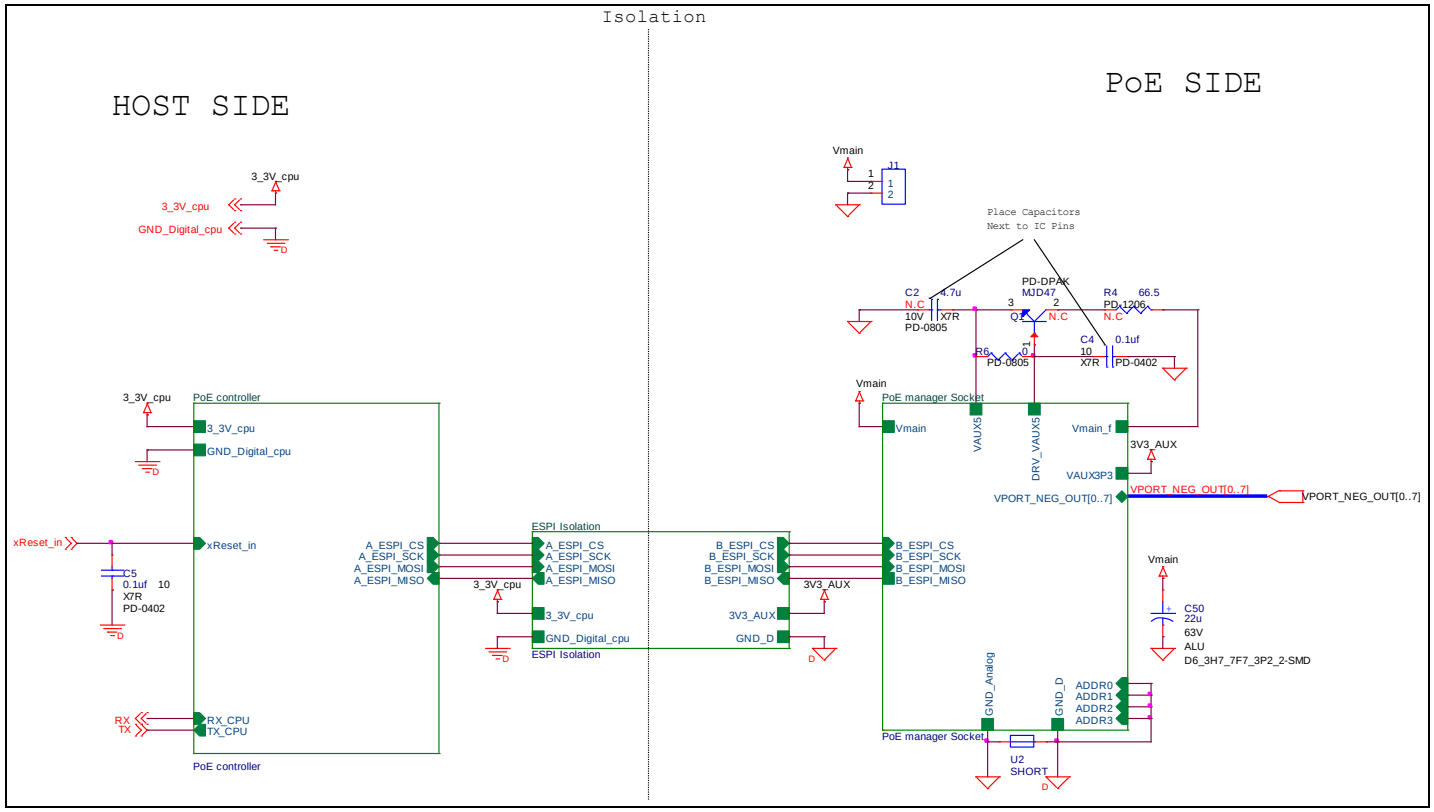

Figure 3: Top Level Blocks

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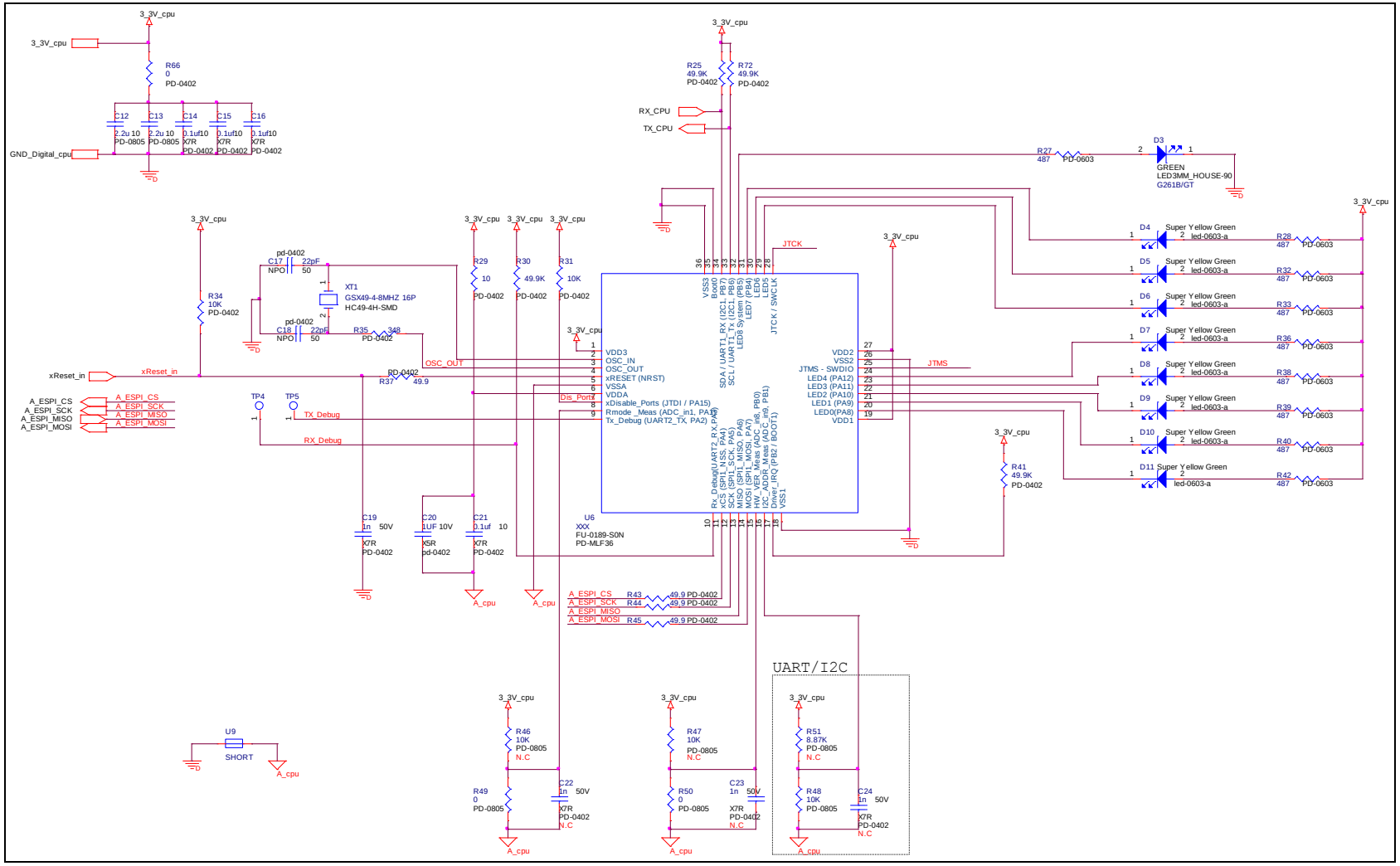

Figure 4: PD39100 PoE Controller Circuitry

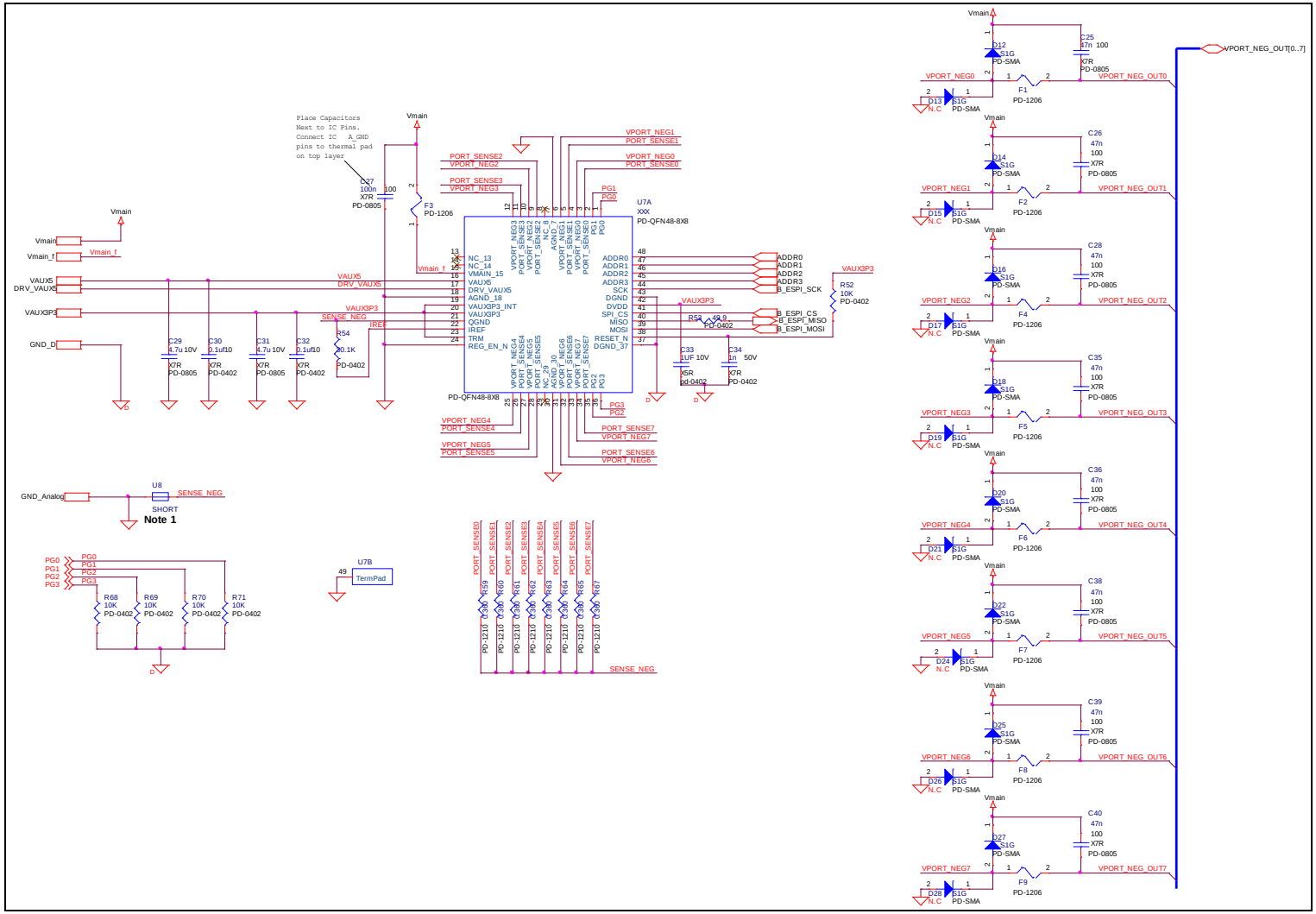

Figure 5: PD69108 Circuitry for PoE Manager

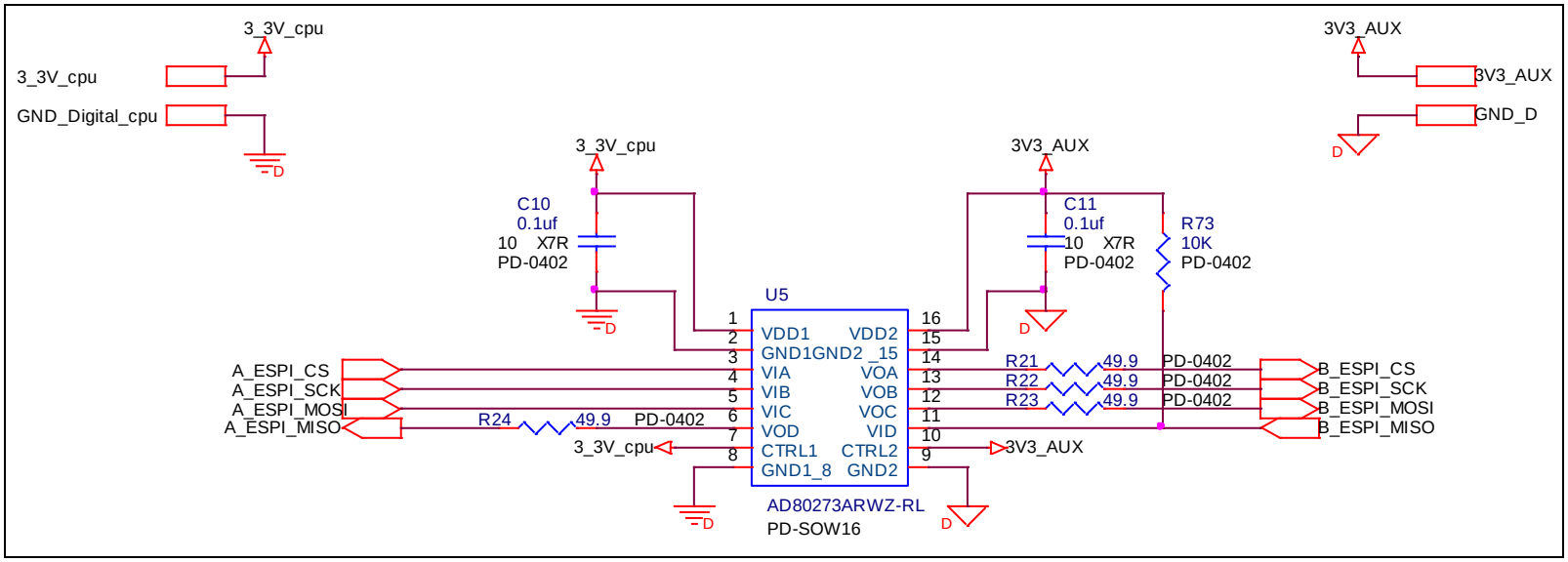

Figure 6: ESPI Isolation Circuitry

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Bill of Materials

Reference	Quantity	Part / Value	PCB Footprint	Notes / Remarks
C2,C29,C31	3	4.7µF	0805	
C4,C5,C10,C11,C14,C15, C16,C21,C30,C32	10	0.1µF	0402	
C12,C13	2	2.2µF	0805	
C17,C18	2	22pF	0402	
C19,C22,C23,C24,C34	5	1nF	0402	
C20,C33	2	1µF	0402	
C25,C26,C28,C35,C36,C38, C39,C40	8	47nF	0805	
C27	1	100nF	0805	
C50	1	22µF	D6_3H7_7F7_3P2_2-SMD	
D4,D5,D6,D7,D8,D9,D10, D11	8	19-21-SYGCS530E3TR8	LED-0603	
D3	1	LED3mm	HOUSE-90	
D12,D13,D14,D15,D16,D17, D18,D19,D20,D21,D22,D24, D25,D26,D27,D28	16	S1G	PD-SMA	
F1,F2, F3, F4,F5,F6,F7,F8,F9	9	F1206B1R50FW-TR	1206	See Note 1
Q1	1	MJD47	DPAK	Supports up to 20mA current draw from the 3.3V_AUX
R4	1	66.5Ω	1206	
R6,R49,R50	3	0	1206	
R7,R31,R34,R52,R68,R69,R70,R71,R73	8	10KΩ	0402	
R21,R22,R23,R24,R37,R43,R44,R45,R53	9	49.9Ω	0402	
R25,R30,R41,R72	4	49.9KΩ	0402	
R27,R28,R32,R33,R36,R38,R39,R40,R42	9	487Ω	0603	
R29	1	10Ω	0402	
R35	1	348Ω	0402	
R46,R47,R48	3	10KΩ	0805	
R51	1	8.87KΩ	0805	
R54	1	30.1KΩ	0402	
R66	1	0	0402	
R59,R60,R61,R62,R63,R64,R65,R67	8	0.360Ω	1210	
TP4,TP5	2	TP60	TP60	
U2,U8,U9	3	SHORT		Short in PCB.
U5	1	AD80273ARWZ-RL	SOW16	
U6	1	PD39100	QFN36-6X6	CPU - PoE Controller
U7	1	PD69108	QFN48-8X8	MSCC – 8 Ports PoE Manager
XT1	1	GSX49-4-8MHZ 16P	HC49-4H-SMD	CPU 8MHz Clock Osc.

Note: In PoE systems with power supply of Less than 100W, these fuses located on the ports may be avoided, as per the IEC 60950-1: 2001 standard

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Revision History

Revision Level / Date	Para. Affected	Description
0.1 / Dec 1st, 2010	-	Initial Release – Preliminary version
0.2 / Mars 11th, 2012		Editing and Proofing
0.3 / April 24th, 2012		
0.4 / July 29th, 2013		Adding maximum current led pins can sink at page #3

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