Microsemi IP Cores Accelerate the Development Cycle and Lower Development Costs

October 2014

Introduction

Today's FPGAs and System-on-Chip (SoC) FPGAs offer vast amounts of user configurable resources that make it possible to create complete systems in a single device. In such scenarios, the use of pre-designed and verified Intellectual Property (IP) blocks helps to reduce the development cost and time. As the pre-defined IP Cores are already completed, the riskiest and most unpredictable phase of verification and debugging is eliminated and the risk associated with the development is reduced.

The use of an IP Core design methodology needs to be supported by advanced design tools that simplify the integration, configuration, and testing of IP-centric designs. For example, when configuring IP Cores it is important to make sure that conflicting definitions are not allowed through the tools without raising a flag to the designer. Additionally, the large number of IP Core connections can be difficult to manage manually, so some short-cut approaches to interconnectivity that eliminate common connection mistakes can eliminate many of the sources of errors in a design.

The Microsemi Approach to Simplifying IP Core-Centric Designs

Microsemi has approached the efficient implementation of IP Core-centric designs with two primary strategies.

The first strategy is to support industry standards that improve the efficiency of creating, managing, protecting, and interfacing various IP Cores. IP-centric design will typically use multiple IP Cores, often from different suppliers, so it is important that these design blocks easily connect to each other and are interoperable among various design flows. Microsemi supports the following industry standards for IP Cores:

- IEEE P1735 Standard Encryption and Rights Management Standard
- ARM® Standard Interfaces such as: AHB, AXI, and APB3
- IP XACT XML Schema for specifying IP connections and metadata

The second strategy is to create an easy to use and automatic design flow for integrating and configuring IP Cores within your design. Without an efficient development flow, time and effort will be lost 'fighting' with the tools instead of using them to easily incorporate pre-defined IP blocks. The Microsemi Libero® SoC tool suite provides key features to simplify IP integration and configuration, as shown below:

- Dropdown menus and other guided approaches to specifying configurations that avoid costly and error-prone 'by hand' configurations.
- IP Cores with standard busses, like the various ARM interface busses, can be connected using a smart connect tool that 'knows' which connections to make for error-free integration.

These two approaches accelerate your design cycle by insuring interoperability between IP Cores and their tools and increasing efficiency within the design tool suite. More details on each of the elements of these two approaches are given in the following sections of this brochure.

IEEE P1735 IP Encryption and Rights Management for Microsemi IP Cores

As the use of IP Cores in modern FPGA and SoC FPGA designs has increased, it is likely that a new design will use multiple IP Cores from different vendors. As the IP Core developers use different methods to protect and manage their designs, it would significantly increase the cost of supporting different design flows.

Fortunately, the IEEE P1735 IP encryption standard is available and IP Core providers can use IEEE P1735 to encrypt, and thus protect, their valuable IP Cores from reverse engineering. FPGA manufacturers and third party FPGA tool providers support IEEE P1735 in their tool flows, hence customers may easily use IP Cores protected by IEEE P1735.

Microsemi has adopted the IEEE P1735 encryption standard for IGLOO®2 FPGAs and SmartFusion®2 SoC FPGAs within the Libero SoC suite of design tools. This insures interoperability between designs using Microsemi DirectCores and third party CompanionCores (IP Cores that support IEEE P1735), and Synopsys Synplify Pro®, Mentor Graphics Modelsim®, and Microsemi Libero SoC design tools.

How IEEE P1735 Works

IP Core providers protect their products using an encryption algorithm, as shown in Figure 1 below. The IP vendor creates a Symmetric Data Key and encrypts the IP Core code. The IP vendor then obtains the EDA vendors Public Key and encrypts their Symmetric Data Key with it. These two data blocks are then bundled, according to the IEEE P1735 standard, and delivered to the IP Core end user or the downstream CAE vendor. In this way, the end user can design with the IP Core but the design itself is protected from reverse engineering.

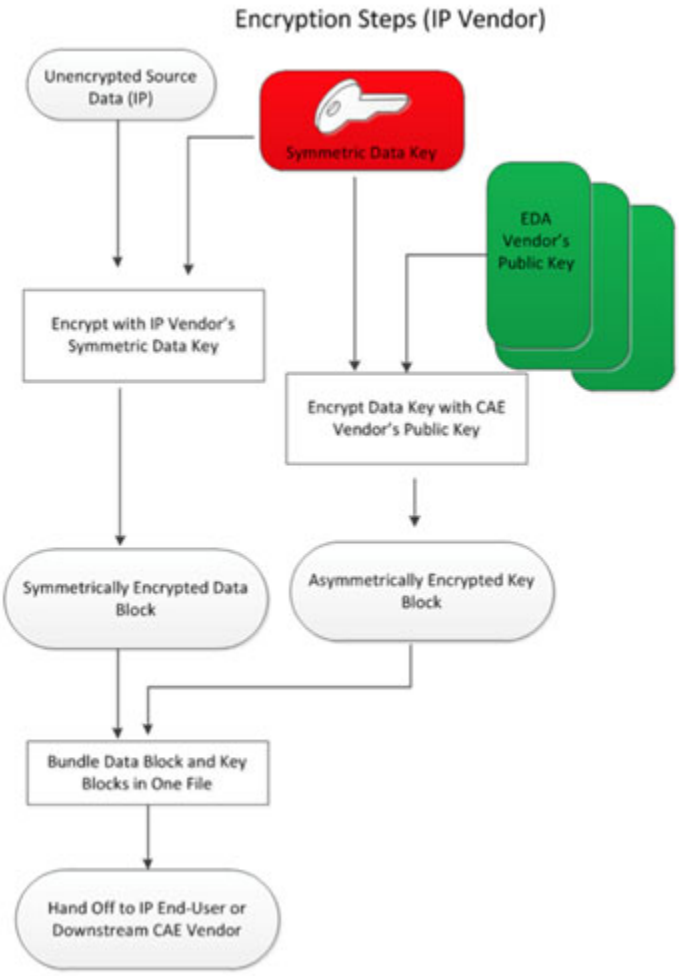

Figure 1: **Encryption Flow used by IP Providers to Protect their IP**

In order to use an encrypted IP Core, the end user can include the IP Core directly in the design, as shown in Figure 2 below. The FPGA tools, either from the FPGA vendor or the CAE vendor, will run as normal but the internals of the encrypted IP Core are not exposed, hence they are not available for on-chip debugging or for schematic viewing. As the IP Cores are pre-proven, there is no need for debugging the internals or viewing schematics—they are simply used as block boxes, where the interface signals are exposed but nothing else is.

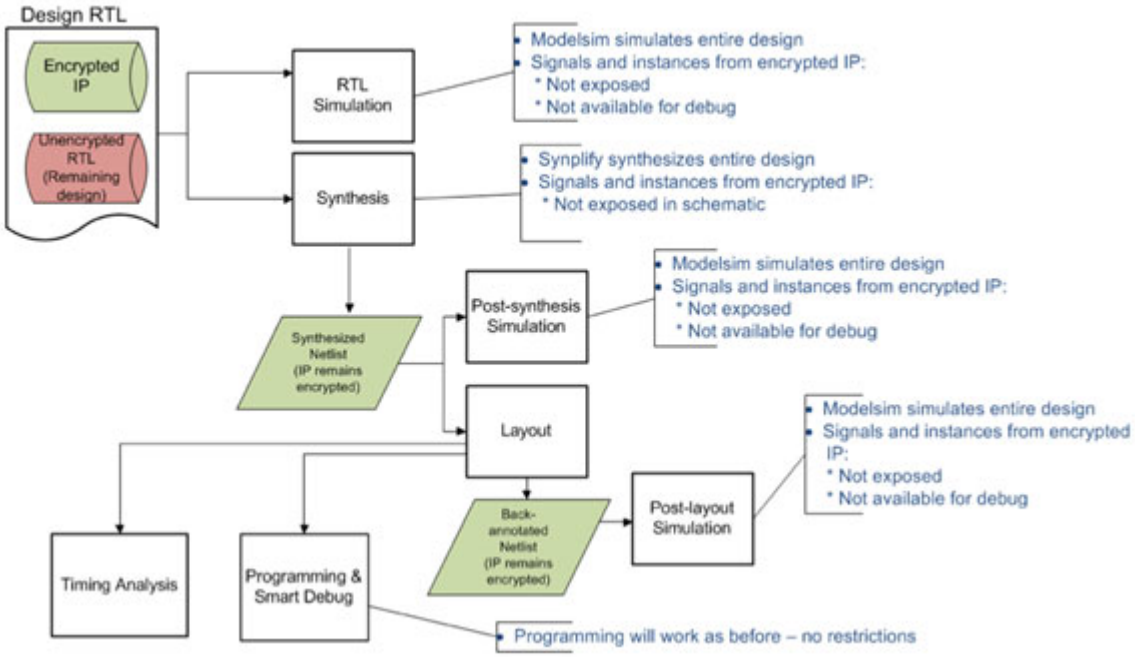

Figure 2: **Encrypted IP Core Design Flow in the Libero SoC Tool Suite**

More information on the use of IEEE 1735 with Microsemi IP Cores is given in the "Libero SoC Secure IP User's Guide", shown in the Reference Section at the end of this brochure.

ARM Centric Bus Interconnect

Microsemi was an early adaptor of an ARM-centric approach to implementing SoC FPGAs and continues to support ARM bus interfaces for common IP Core functions. Using a common bus interface provides a variety of benefits such as:

- Leveraging established interfacing standards—this allows IP developers to focus on functional differentiation, not implementing a variety of different interfaces to deliver the best overall solution to their customers.
- Enabling a wider variety of IP Core developments.
- Supporting Interoperability between different IP Core providers, and simplifying system integration.
- Leveraging simulation and test bench environments over multiple designs when common interfaces are used, thus reducing development time and cost.
- Avoiding the developer need to learn multiple competing standards.

IGLOO2 FPGAs and SmartFusion2 SoC FPGAs support a variety of ARM bus interfaces including hardened implementations, like those within the SmartFuson2 Microcontroller Subsystem (MSS) and the IGLOO2 High-Performance Memory Subsystem (HPMSS), as well as within the FPGA fabric on both SmartFusion2 and IGLOO2 devices. Some examples of where standard interfaces are used include:

- The SmartFusion2 MSS uses the AHB bus matrix to connect to hardened peripherals as well as the FPGA fabric.
- The SmartFusion2 MSS DDR controller uses the AXI bus for high-speed data transfers and the AHB for configuration.
- The SmartFusion2 fabric DDR controller uses the AXI bus for high-speed data transfers and the AHB bus for configuration.
- The IGLOO2 HPMSS uses an AXI interface to the FPGA fabric for high-speed data transfers and the AHB for configuration for the hardened DMA controllers.
- The 5G SERDES, on both the IGLOO2 FPGA and SmartFusion2 SoC FPGA, uses the AXI bus for high-speed data transfers and the AHB for configuration of PCIe® and other SERDES-based standards.
- Fabric-based peripherals use the AHB bus for connecting to the SmartFusion2 AHB bus matrix.
- Fabric-based AHB master and slave controllers are available to simplify connecting various peripheral functions and custom hardware accelerators within the FPGA fabric.

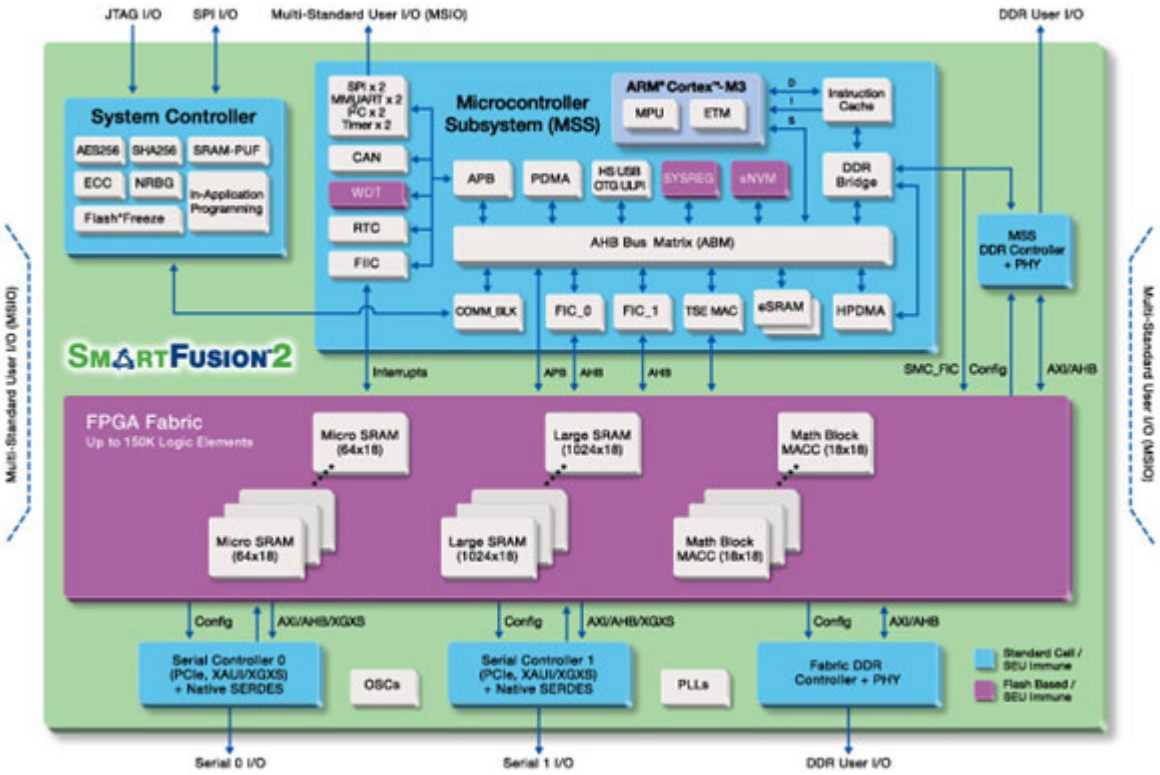

Figure 3: **SmartFusion2 Block Diagram Showing the use of IP-Centric Bus Interfaces**

Microsemi's use of a widely popular interface standard dramatically simplifies an IP centric-based design while lowering the cost of acquiring and supporting the variety of IP Cores that are required in today's FPGA and SoC FPGA designs.

IP-XACT XML Standard for IP Definition and Storage

The IEEE 1685 IP-XACT XML standard was created in 2009 to define and describe electronic components and their designs in a consistent and automatic manner. It enables the creation of compatible component descriptions from a wide variety of members in a standard format. This results in compatible libraries that can be easily created and shared between users, vendors, and design teams. Most importantly, for IP-centric design the standard describes configurable components by using XML metadata that various vendors' development tools can use. Common tools and scripts are developed easier, thanks to the IP-XACT standard; for being vendor and tool neutral and not customized for a particular development environment.

Microsemi uses IP-XACT for creating and accessing IP cores within the Libero SoC IP Core vault. The vault is the repository for all IP cores accessible to the user's design and is automatically kept up-to-date using IP-XACT standard processes and definitions. All IP Cores, whether provided as DirectCores by Microsemi, or as CompanionCores by third parties, or as a development by an in-house design team, use IP-XACT for storage within the vault, or during configuration within the Microsemi Libero SoC tool flow. Some of the benefits to the designer of Microsemi and its development partners are:

- Leveraging established definition standards—this allows IP developers to focus on functional differentiation, instead of needing to implement a variety of different standard IP Core definition standards.
- Ensuring interoperability between different IP Core providers and CAE vendors— this simplifies the system integration.
- Simplifying the development of standard scripts and tools that store, access, and create IP Core definitions from any IP Core vendor or within any FPGA development tool flow.
- Enabling simple and guided configuration of IP Cores to eliminate the risks associated with conflicting and error-prone 'by hand' configuration settings.

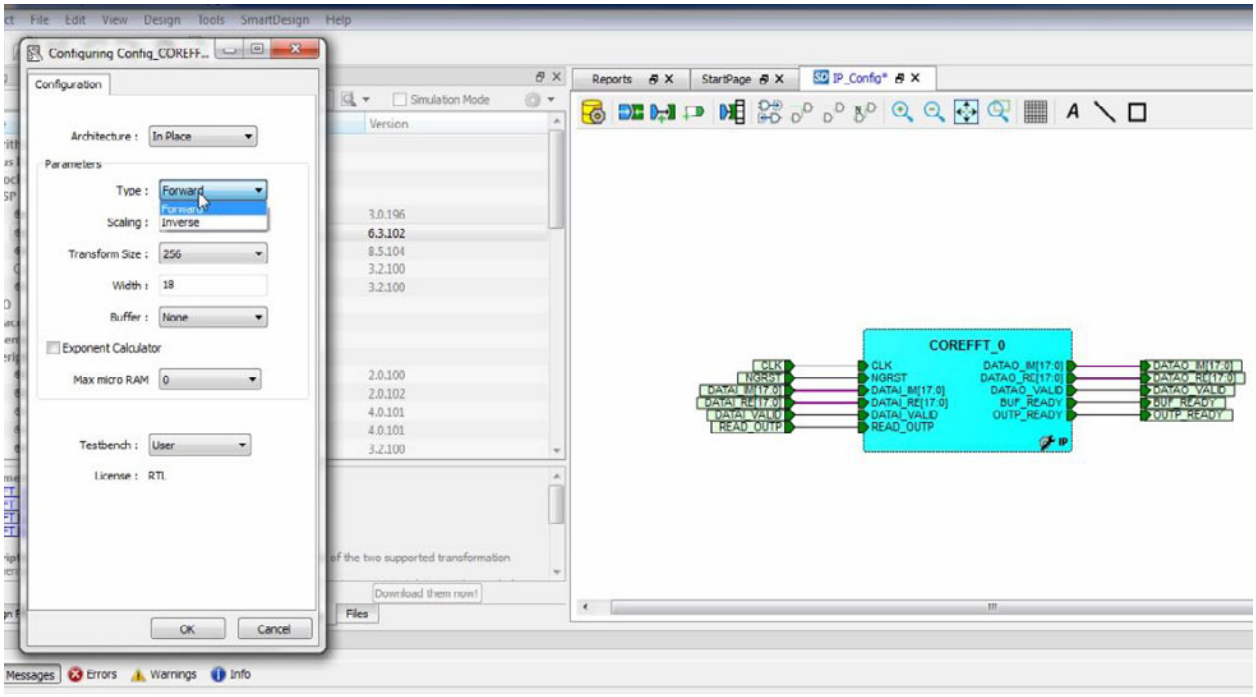

Figure 4: **Automatic Configuration of an IP Core within Libero SoC uses IP-XACT Definition Data**

The use of IP-XACT simplifies the storage and accessing of IP Cores by the Libero SoC tool flow to dramatically improve the ease of integration of IP Cores, no matter where the IP Core is sourced. Development time is reduced and integration risks are mitigated by using IP-XACT with all Microsemi supported IP Cores.

Conclusion

Using IP Cores that target Microsemi FPGAs and SoC FPGAs, can reduce development time and reduce development cost. Microsemi delivers these benefits by supporting key industry standards that enable interoperability and by providing advanced design tools that simplify the process of integrating IP Cores into your design. Learn more about the IP Cores available for Microsemi devices and the advantages of using them on the Microsemi IP Core website at: *http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores*.

References

Libero SoC Secure IP User's Guide

http://www.microsemi.com/document-portal/doc_download/133573-libero-soc-secure-ip-flow-user-guide

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense and security, aerospace, and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs, and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 3,400 employees globally. Learn more at **www.microsemi.com**.

55900185-1/10.14