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Synplify Pro[®] for Microsemi Edition Release Notes

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Release Note Topics

About the I-2013.09M-SP1-1 Release	2
I-2013.09M-SP1 Feature and Enhancement Summary	2
Platforms	3
Required Operating System Patches	3
Documentation	5
Known Problems and Solutions	7

About the I-2013.09M-SP1-1 Release

This I-2013.09M-SP1-1 release includes software features and enhancements for the Synplify Pro® Microsemi Edition product.

For the complete summary of features and enhancements contained in the base release, see [I-2013.09M-SP1 Feature and Enhancement Summary, on page 2](#).

I-2013.09M-SP1 Feature and Enhancement Summary

The following table highlights the I-2013.09M-SP1 features:

Feature	Description
VM Flow Support	The tool now generates Verilog output netlist (.vm) for SmartFusion2 and IGLOO2 for P&R flow. See the online help or reference.pdf->Designing with Microsemi->Output Files and Forward-annotation for Microsemi.
Ignoring SystemVerilog Assertions (SVA)	For SVA support, see the online help or reference.pdf ->SystemVerilog Language Support->Assertions.
Context Help Update	The Context Help editor adds support for the following: <ul style="list-style-type: none">• Verilog constructs• Tcl constraint commands for collections Use the template to copy example constructs or commands into your HDL or Tcl file. See the online help or user_guide.pdf->Preparing the Input->Setting up HDL Source Files->Using the Context Help Editor.
HDL Analyst Incremental Quick Load (Beta)	The behavior of the HDL Analyst quick load feature has been modified as follows: <ul style="list-style-type: none">• Initially, enable the HDL Analyst Database Generation (Beta) option so the compiler pre-partitions the design and generates a database consisting of multiple netlist files (srs) that can be used by the HDL Analyst tool. This option is disabled by default.• Then, set the Incremental Quick Load (Beta) option from the HDL Analyst tool to enable or disable incremental quick load. When enabled, the HDL Analyst tool dynamically loads only the affected design hierarchy as needed. Otherwise, the entire design is loaded by default. See the online help or user_guide.pdf->Setting up a Logic Synthesis Project->Setting Logic Synthesis Implementation Options->Setting Optimization Options.
Tcl export_project Command	Creates a new module- or instance-based subproject that can be exported and inserted into the current project. Use the various options of this Tcl command to help you create the subproject easily in batch mode. See the online help or command_reference.pdf->Tcl Commands->Alphabetical List of Commands->export_project.

Feature	Description
Log File and Reporting Enhancements	<p>Includes various log navigation enhancements:</p> <ul style="list-style-type: none"> • Use the Project Status Page Location option to save the current project status to a location of your choice. You can then view the project status offline with any browser on a remote device. • Detailed reports link directly to the log file from the project status summary page. <p>You can now open the Timing Report view from the project status summary page, as well.</p> <p>See the online help or user_guide.pdf->Synthesizing and Analyzing the Results->Checking Log File Results->Accessing Results Remotely.</p> <p>See the online help or user_guide.pdf->Synthesizing and Analyzing the Results->Checking Log File Results->Accessing Specific Reports Quickly.</p>
Project Status Query	<p>Writes out the results of the reports displayed in the Project Status view (status_report command).</p> <p>See the online help or command_reference.pdf->Tcl Commands ->Alphabetical List of Commands->status_report.</p>
P1735 Encryption	<p>P1735 is a proposed IEEE standard.</p> <p>Additional undocumented options are available for IP encryption with P1735 standard.</p> <p>Enter <code>encryptP1735.pl -help</code> for details.</p>

Platforms

This section includes platform support for the Synopsys FPGA synthesis products. The software is supported on the platforms and operating systems listed below:

Windows (x86/x64)	<ul style="list-style-type: none"> • Windows 7 Professional or Enterprise (32/64-bit) • XP Professional SP2 or later (32/64-bit) • Vista Enterprise or Business (32/64-bit). This is the last release to support this platform.
Linux (x86/x64)	<p>All Linux platforms require 32-bit compatible libraries.</p> <ul style="list-style-type: none"> • Red Hat Enterprise Linux 4/5/6 (32/64-bit). This is the last release to support RHEL 4 and 32-bit RHEL 6. • SUSE Linux Enterprise 10/11 (32/64 bit)

Required Operating System Patches

Running this software requires that the Linux operating system include specific patches. To determine whether your operating system requires patches, refer to the following procedure.

Checking the Installed Patches

All Linux-based FPGA synthesis applications include a script (syn_system_check) that is designed to check patches that have been installed and the patches that need to be installed or updated.

To use this script:

1. Install the product software.
2. Run the script by entering the following command in a shell:
`/install_dir/product_version/bin/syn_system_check`
3. The script runs and generates a system check summary report that lists the patches and patch status (OK, Install, or Upgrade).
4. Consult the display and install or update any of the patches indicated.

Example

The following is a sample report.

```
+++++
Synplicity system check summary report for host 'synsun2'

1. /home/syn/user available size == 13728736 KB      [ OK ]
2. /tmp available size == 243192 KB                  [ OK ]
3. /var/tmp available size == 22069 KB               [ OK ]
4. Current DISPLAY is set to 'user:0'               [ Check user ]
5. Required Patch '106950-13'                        [ Install Patch ]
6. Upgrade from '106146-14' to '106146-31' Required [ Upgrade Patch ]
7. Upgrade from '106327-08' to '106327-13' Required [ Upgrade Patch ]
8. Upgrade from '106541-07' to '106541-19' Required [ Upgrade Patch ]
9. Upgrade from '108376-12' to '108376-34' Required [ Upgrade Patch ]
10. sparc architecture                              [ OK ]
11. synsun2 solaris 5.7                             [ OK ]

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Explanation of Operating system patches, following patches are
available at vendor's ftp site

[ 106146-31 ] SunOS 5.7: M64 Graphics Patch
[ 106327-13 ] 32-Bit Shared library patch for C++
[ 106541-19 ] SunOS 5.7: Kernel update patch
[ 106950-13 ] SunOS 5.7: Linker Patch ( required by 106327-13 )
[ 108376-34 ] OpenWindows 3.6.1: Xsun Patch

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```

Documentation

The following documents are included with the Synopsys FPGA synthesis products. All documents can be accessed through the online help (HTML), and as PDF documents. See [Accessing Online Help on page 6](#), and [Accessing PDF Documents on page 5](#) for information on how to access the documents.

Document	Access
User Guide	Online help, context-sensitive help, PDF
Reference Manual	Online help, context-sensitive help, PDF
Attribute Reference Manual	Online help, context-sensitive help, PDF
Command Reference Manual	Online help, context-sensitive help, PDF
System Designer User Guide	Online help, context-sensitive help, PDF

Accessing PDF Documents

PDF documents display in Adobe Acrobat Reader. You can download the latest Acrobat Reader at no cost from Adobe's website (www.adobe.com). The PDF files provided are optimized for output to a laser printer, not for viewing online.

You can access the PDF documents in multiple ways, while running the tool or separately:

- From within the tool, with the Help-Online Documents command.
- From outside the tool, through the Documentation tab in SolvNet.
- From outside the tool, as described below:

Linux	From outside the software, select Open Acrobat Reader: <code>acroread</code> Open <code>installDirectory/documents/docFile</code>
Windows	Start->Programs->Synopsys->FPGA Synthesis I-2013.09M-SP1-1->Documents Then, select the desired document.

If the PDF for the online documentation does not open in the synthesis tool, make sure you are using a recent version of the Acrobat Reader that can be downloaded from Adobe's website. Do not use the View->Full Screen option when viewing documents in Acrobat Reader unless you are sure you want this full magnification. On some applications, this selection takes over the monitor and there is no apparent way to access other running tasks or windows. If you do happen to use the Full Screen option, you can use Ctrl-I to undo it.

Accessing Online Help

This section describes how to access online help and context-sensitive help in the Synplify Pro tool.

If your online help graphics do not display correctly, this is usually because your Display setting is 256-Color. Reset it to 16-bit Color, then reopen the online help.

Accessing Help from inside the tool

All platforms	Select Help->Help for the online help system. For context-sensitive help, click F1 in a dialog box or window. For context-sensitive help for an error message, click the link in the log file or the Message viewer. If your online help search does not locate error messages, open online help and set the Filtered by field to either Unfiltered or Messages Only.
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Accessing Help from outside the tool

Windows	Select Start->Programs->Synopsys->FPGA Synthesis I-2013.09M-SP1-1->Help
Linux	Run fpga_help.

Known Problems and Solutions

The following problems apply to supported features in the Synplify Pro tool.

Crossprobing Source Code Files Created with Third-Party Editors

When using source code files created with third-party editors, you sometimes cannot crossprobe to the correct line number in the source file.

Solution: Open the file in the FPGA synthesis tool text editor.

Editing Externally Created Project (prj) Files

If Tcl commands or script files were used to build your project, you might not be able to save this Project file from the synthesis UI in downstream tools, because they contain hard-coded file paths.

Solution: Generally, use the same method to save a project as you did to create the project. In this case, save the project file to an external text editor and not in the project UI.

Tool Invocation Slow on Linux With Network Problems

Invoking the synthesis tools might be slow when you are experiencing network problems on Linux platforms, such as when a mounted drive is not accessible. If you previously had network problems, the synthesis tool may remain slow even though the network problems have cleared.

Solution: Delete the \$HOME/.config/Trolltech.conf file to avoid caching. This might help to invoke the tool faster.



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