Optical Transport Network Clock Translator Selector Guide

Optical Transport Network (OTN) has emerged as the physical layer interface protocol of choice for carriers to transport a variety of services over a single optical fiber. Microsemi offers the widest portfolio of single-chip devices delivering “any frequency, any port” performance for OTN.

Part	DPLLs or Paths	DPLL BW (Hz)	Inputs	Diff. Outputs	CMOS Outputs	Low-Jitter APLLs	GP Clock Gen	Typ. Jitter (ps_{RMS})	Input Frequency	Output Frequency	NV Memory	Host Bus	2K/8K Align	1 Hz Align	NCO (ppb)	Pkg size (mm)
ZL30152	1	14–896	2 D/SE	4	2	1	0	0.7	1 kHz–750 MHz	1 kHz–750 MHz	OTP	SPI/I2C				9 x 9
ZL30155	2	14–896	4 D/SE	8	4	2	0	0.7	1 kHz–750 MHz	1 kHz–750 MHz	OTP	SPI/I2C				11 x 11
ZL30157	2	14–896	4 D/SE	8–12	4–12	1	1	0.7	1 kHz–750 MHz	1 kHz–750 MHz	OTP	SPI/I2C				11 x 11
ZL30160	4	14–896	4 D/SE	8	4–12	2	2	0.7	1 kHz–750 MHz	1 kHz–750 MHz	OTP	SPI/I2C				11 x 11
ZL30165	4	5–806	8 D/SE	8	8	4	0	0.65	1 kHz–750 MHz	1 Hz–750 MHz	OTP	SPI/I2C			0.001	13 x 13
MAX24705	1	4–400	2 D/SE	0–5	0–10	1–2	0	0.35	2 kHz–750 MHz	1 Hz–750 MHz	Int EE	SPI	•		0.01	10 x 10
MAX24710	1	4–400	2 D/SE	0–10	0–20	1–2	0	0.35	2 kHz–750 MHz	1 Hz–750 MHz	Int EE	SPI	•		0.01	10 x 10
ZL30166	3	5–896	9 D/SE + 2 SE	8	8	4	0	0.65	1 kHz–750 MHz	1 Hz–750 MHz	OTP	SPI/I2C		•	0.001	13 x 13
ZL30167	2	5–896	9 D/SE + 2 SE	8	8	4	0	0.65	1 kHz–750 MHz	1 Hz–750 MHz	OTP	SPI/I2C		•	0.001	13 x 13
ZL30168	4	5–896	8D/SE	8	8	4	0	0.65	1 kHz–750 MHz	1 Hz–750 MHz	OTP	SPI/I2C			0.001	13 x 13
ZL30169	1	14–500	2 D/SE + 2 SE	3	6	1	0	0.25	1 kHz–1250 MHz	1 Hz–1035 MHz	Int EE	SPI/I2C	•		0.01	5 x 5
ZL30182	2	5–500	4 D/SE + 2 SE	6	12	2	0	0.25	1 kHz–1250 MHz	1 Hz–1035 MHz	Int EE	SPI/I2C	•		0.01	5 x 10
ZL30174	3	14–470	5 D/10 SE	6	14	3	1	0.18	1 kHz–900 MHz	1 Hz–900 MHz	Int EE	SPI/I2C	•	•		10 x 10

Abbreviations:
APLL= analog phase-locked loop. D/Diff= differential. DPLL= digital phase-locked loop. Freq= frequency. Gen= generator. GP= general purpose. Int. EE= internal EEPROM. Int-N= integer-N (can only multiply by an integer). NCO= numerically controlled oscillator. NV= nonvolatile. OTP= one-time programmable. Ppb= parts per billion. Pkg= package. SE= single-ended (CMOS).

Inputs:
APLLs are fractional-N unless specified as Int-N. GP clock gen are general-purpose clock generators that make output clock signals with more than 1 ps RMS jitter. 2k/8k align means the part can phase-align all outputs to a 2 kHz or 8 kHz alignment input. 1 Hz align means the part can phase-align all outputs to a 1 Hz alignment input.

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