Microsemi Corporation

April 9, 2014

Customer Notification No: PCN1309A

Customer Advisory Notice (CAN)

Subject: Addendum to PCN1309 – Synopsys Synplify Pro Software Bug Regarding Safe State Machine Recovery

Dear Customer,

This addendum provides detailed information on the method of identifying the affected design by synthesis software bug which affects the state machine recovery when the safe state machine synthesis attribute was enabled (syn_encoding=safe). Searching the EDIF netlist only may be inadequate by itself.

Following are the methods to identify if the design is getting affected by this bug. Method 1 is the best and easiest way to examine. For other methods, you will need the Synplify project file and design files (RTL, *.fdc, *.sdc, *.srr, and *.prj) available for review to identify if the bug has affected the design.

Method 1

1. Install one of these recent releases:

   From Synopsys: Synplify Pro 2013.09 or 2013.09 SP1

   From Microsemi: Synplify Pro ME I-2013.09M SP1
2. Open .prj and re-synthesize
3. If the following error is present in the .srr (log file):

@E: : counter_self.vhd(85) | Cannot find asynchronous or synchronous reset signal and reset state for state machine current_state[0:16] (view:work.counter_self(rtl)). So, attribute syn_encoding = "safe" cannot be implemented for this state machine.

your design is indeed affected by the bug and the safe logic is not built.

If the above error is not present then your design does not have the FSM bug.

Method 2

1. If you use an encoding style of sequential or gray **AND**
2. If the state machine has a power of 2 number of states

   There are no illegal states and FSM bug will not occur.

Method 3

If you did not use syn_encoding = “safe”,

The design will not have the FSM bug.

Check

- Search for the following line(s) in .srr file to check if the syn_encoding= “safe” attribute is not used

Adding property syn_encoding, value "safe", to instance dut.current_state[0:16].

If this is statement is not present in your .srr file, then your design does not have the bug.

- Use ‘grep’ for *syn_encoding* through the files – RTL, *.fdc, *.sdc, *.srr, and *.prj. , to confirm if the syn_encoding attribute is not set to “safe”.

Method 4

If you have FSM Compiler OFF,

The design will not have the FSM bug. Default is OFF.

Check

Check the .prj file if set_option -symbolic_fsm_compiler is not present or set_option -symbolic_fsm_compiler is 0, then your design is good.

Method 5

If your test methodology includes thorough simulation of state machines and recovery, then it is likely you will have encountered the FSM problem and corrected it during validation prior to programming devices.

This will have been done by “stress” testing during simulation by injecting failures to the state machines to test FSM recovery.

Analyzing if your design meets all the criteria and the FSM bug is present

First, you must have at least one state machine that has

syn_encoding = “safe”

AND

FSM Compiler ON

Additional details about the syntax, where the syn_encoding attribute can be set in the HDL and tools, and how FSM Compiler is enabled, can be found in the Reference Manual which is installed with the tool in the doc folder or can be downloaded from our website:
Synopsys FPGA Synthesis Synplify Pro ME H-2013.03M-SP1-1 Reference or
http://www.microsemi.com/products/fpga-soc/design-resources/design-software/synplify-pro-me#documents.

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Regards,

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