

Microsemi Corporation

April 4, 2014

Customer Notification No: CN1413

Customer Advisory Notice (CAN) – Action Required

Subject: uSRAM and LSRAM timing updates in SmartFusion2 SoC and IGLOO2 FPGAs

Description of Issue(s):

This notification describes timing updates made to the LSRAM and uSRAM blocks in SmartFusion2 SoC FPGA and IGLOO2 FPGAs. These changes are effective in the Libero SoC v11.3 software release. Detailed changes and expected impact on design performance are provided here to help designers identify whether their designs are likely to be impacted by these timing changes. The IGLOO2 Datasheet (revision 2) on the web contains the new timing data. The SmartFusion2 Datasheet will be updated to revision 6 with the same data. In the interim, users can use the IGLOO2 Datasheet timing information as a reference.

Change Description

1. LSRAM Fmax Read and Write clock (and Pipeline clock) decreased to 400MHz (IND -1), 300MHz (MIL, -1), 340MHz (IND, STD), 255MHz (MIL, STD). These changes impact the following parameters in the datasheet:

LSRAM under WC Conditions							
Parameter	Description	Condition	-1		Std		Units
			Min	Max	Min	Max	
tCY	Clock Period	COM	2.5	-	2.941	-	ns
		IND	2.5	-	2.941	-	ns
		MIL	3.333	-	3.921	-	ns
tCLKMPWH	Clock Minimum Pulse Width High	COM	1.125	-	1.323	-	ns
		IND	1.125	-	1.323	-	ns
		MIL	1.5	-	1.765	-	ns
tCLKMPWL	Clock Minimum Pulse Width Low	COM	1.125	-	1.323	-	ns
		IND	1.125	-	1.323	-	ns
		MIL	1.5	-	1.765	-	ns

LSRAM under WC Conditions							
Parameter	Description	Condition	-1		Std		Units
			Min	Max	Min	Max	
tPLCY	Pipelined Clock Period	COM	2.5	-	2.941	-	ns
		IND	2.5	-	2.941	-	ns
		MIL	3.333	-	3.921	-	ns
tPLCLKMPWH	Pipelined Clock Minimum Pulse Width High	COM	1.125	-	1.323	-	ns
		IND	1.125	-	1.323	-	ns
		MIL	1.5	-	1.765	-	ns
tPLCLKMPWL	Pipelined Clock Minimum Pulse Width Low	COM	1.125	-	1.323	-	ns
		IND	1.125	-	1.323	-	ns
		MIL	1.5	-	1.765	-	ns

2. uSRAM Fmax Read and Write clock (and Pipeline clock) decreased to 250MHz (-1 and STD)

uSRAM under WC Conditions							
Parameter	Description	Condition	-1		Std		Units
			Min	Max	Min	Max	
tCY	Read Clock Period	COM	4	-	4	-	ns
		IND	4	-	4	-	ns
		MIL	4	-	4	-	ns
tCLKMPWH	Read Clock Minimum Pulse Width High	COM	1.8	-	1.8	-	ns
		IND	1.8	-	1.8	-	ns
		MIL	1.8	-	1.8	-	ns
tCLKMPWL	Read Clock Minimum Pulse Width Low	COM	1.8	-	1.8	-	ns
		IND	1.8	-	1.8	-	ns
		MIL	1.8	-	1.8	-	ns
tPLCY	Read Pipelined Clock Period	COM	4	-	4	-	ns
		IND	4	-	4	-	ns
		MIL	4	-	4	-	ns
tPLCLKMPWH	Read Pipelined Clock Minimum Pulse Width High	COM	1.8	-	1.8	-	ns
		IND	1.8	-	1.8	-	ns
		MIL	1.8	-	1.8	-	ns
tPLCLKMPWL	Read Pipelined Clock Minimum Pulse Width Low	COM	1.8	-	1.8	-	ns
		IND	1.8	-	1.8	-	ns
		MIL	1.8	-	1.8	-	ns
tCCY	Write Clock Period	COM	4	-	4	-	ns
		IND	4	-	4	-	ns
		MIL	4	-	4	-	ns
tCCLKMPWH	Write Clock Minimum Pulse Width High	COM	1.8	-	1.8	-	ns
		IND	1.8	-	1.8	-	ns
		MIL	1.8	-	1.8	-	ns
tCCLKMPWL	Write Clock Minimum Pulse Width Low	COM	1.8	-	1.8	-	ns
		IND	1.8	-	1.8	-	ns
		MIL	1.8	-	1.8	-	ns

3. Other uSRAM timing updates are depicted below:

uSRAM under WC Conditions							
Parameter	Description	Condition	-1		Std		Units
			Before	New	Before	New	
tCLK2Q	Read Access Time with Pipeline Register	COM	0.34	0.23	0.4	0.27	ns
	Read Access Time without Pipeline Register	COM	1.75	1.18	2.06	1.39	ns
tADDRSU	Read Address Setup Time in Synchronous Mode	COM	0.17	0.13	0.2	0.15	ns
	Read Address Setup Time in Asynchronous Mode	COM	0.93	1.65	1.09	1.94	ns
tADDRHD	Read Address Hold Time in Synchronous Mode	COM	0.11	0.08	0.13	0.1	ns
	Read Address Hold Time in Asynchronous Mode	COM	0.07	-0.62	0.09	-0.73	ns

Performance Impact

Designs accessing the uSRAM or LSRAM at clock rates above the new frequency limits will see these rates dropping to the new limit.

Suggested Action

If SRAM blocks are being used in the design, users should perform a new static timing analysis using SmartTime in the Libero SoC v11.3 release.

Products Affected by this Change

Refer to Addendum A for the complete product list (click on the paper clip icon in the upper left margin of this document to view).

Contact Information:

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Regards,

Microsemi Corporation

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