

Synchronous Ethernet (SyncE) Products

Synchronous Ethernet (SyncE) is a physical layer (PHY)-based synchronization implementation for packet networks requiring frequency synchronization. Microsemi provides standalone SyncE with an easy migration path to IEEE 1588, or combined SyncE and IEEE 1588 for both frequency and time alignment.

The market leader in SyncE timing devices, Microsemi was the first to introduce SyncE PLLs in 2006. Microsemi now offers the industry's most comprehensive portfolio of SyncE timing devices, providing G.8262 compliance and ultra-low jitter for 10G PHYs.

Highly-integrated, feature-rich SyncE products from Microsemi allow manufacturers to create cost-effective network equipment designs that support accurate end-to-end transmission of voice, video, and data over wired and wireless networks.

Applications

- Core routers, edge routers, Carrier Ethernet switches—timing cards and line cards, which support up to 100 Gbps interfaces, line rate converters, and carrier-grade timing cards, SONET/SDH, Fibre Channel, XAUI, SyncE, and OTN
- Broadband equipment including PON, DSLAM, and RT-DSLAM
- Wireless backhaul—integrated basestation reference clock for air interface for GSM, WCDMA, LTE and WiMAX macro, micro or femtocells, edge router, or access aggregation nodes

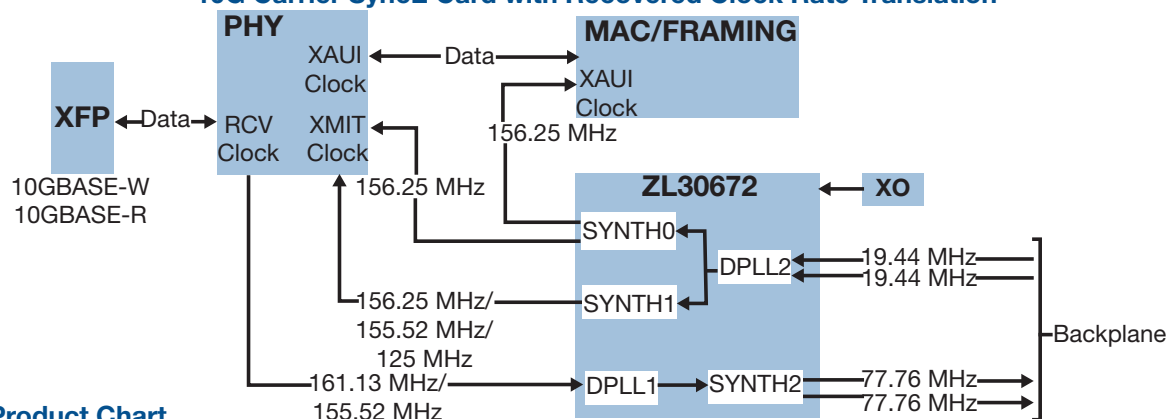
Timing Card Product Features

- Compliance with ITU-T G.8262, G.8262.1, G.813, G.781, G.8261, G.823, and G.824
- Telcordia GR-1244 and GR-253 Stratum 3
- Low bandwidth loop filter from 0.1 mHz to 1 kHz
- Hitless reference switching, up to 11 input references
- Holdover accuracy better than <0.1 ppb
- Accept and generate any frequency from 1 Hz to 1250 MHz

Line Card Product Line Features

- Ultra low jitter (as low as <250 fs RMS for line cards up to 100G)
- Loop filter from 14 Hz to 896 Hz
- Hitless reference switching between up to 8 input references
- Frequency translation and jitter attenuation of any frequency between <0.5 Hz and 1045 MHz
- Numerically controlled oscillator (NCO) capability

10G Carrier SyncE Card with Recovered Clock Rate Translation



SyncE Product Chart

	ZL30151	ZL30611 ZL30612 ZL30614	ZL30161 ZL30162 ZL30163 ZL30164	ZL30621 ZL30622 ZL30623	ZL30601 ZL30602 ZL30603 ZL30604	ZL30681 ZL30682 ZL30683	ZL30671 ZL30672 ZL30673
Application	Line card	Line card	Central timing	Pizza box	Central timing	Line card	Central timing
PLL channels	1	1, 2, and 4	1, 2, 3, and 4	1 and 2	1, 2, 3, and 4	1, 2, and 3	1, 2, and 3
Inputs	3	10	11	3 and 6	10	10	10
Ref inputs	No	Yes	Yes	No	Yes	Yes	Yes
Outputs	3	14	12 and 16	3 and 6	14	16	16
Output jitter	350 fs	250 fs	700 fs	350 fs	250 fs	<300 fs	<300 fs

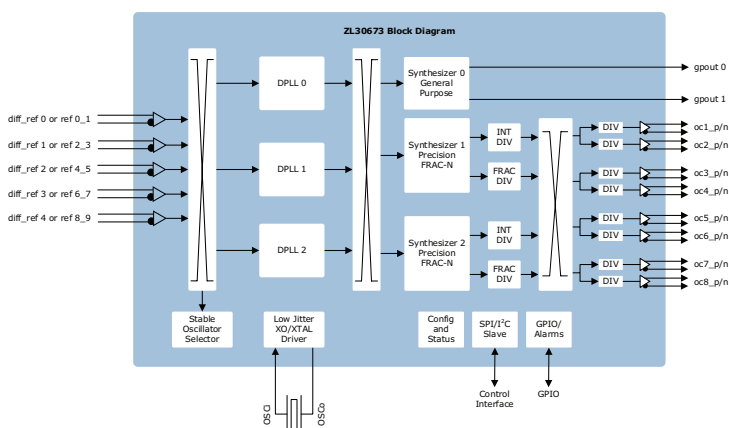
Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

Synchronous Ethernet (SyncE) Products

ZL30673 Synchronous Ethernet System Synchronizer

- Precise phase/frequency measurement and tuning lowers system latency to meet 4G LTE, 5G, and wireless infrastructure requirements
- Two programmable ultra-low jitter synthesizers generate any frequency from 0.5 Hz to 1045 MHz
- Maximum jitter less than 300 fs in 12 KHz to 20 MHz band meets jitter of 10G/40G and 100G PHYs
- One programmable general purpose synthesizer generates any clock from 0.5 Hz to 180 MHz.
- 8 differential or 16 single ended (CMOS) ultra-low jitter outputs plus two general purpose outputs
- Accepts up to 10 LVPECL/LVDS/HCSL/LVCMOS inputs
- Any input reference can be fed with clock, sync (frame pulse), clock /sync pair, or clock modulated with sync pulse (embedded pps—ePPS and embedded pp2s—ePP2S)
- Automatic hitless reference switching and digital holdover on reference fail with initial holdover accuracy better than 10 ppb
- Up to three programmable digital PLLs/NCOs with loop bandwidth from 0.1 mHz to 470 Hz synchronize to any clock rate from 0.5 Hz to 900 MHz and to clock plus sync pulse (0.5 Hz and up)

ZL30673 Block Diagram



ZL30622 Synchronous Ethernet System Synchronizer

- Fully compliant to ITU-T G.813/G.8262 compliance (options 1 and 2)
- Programmable bandwidth, 0.1 Hz to 500 Hz
- Hitless reference switching
- High-resolution holdover averaging
- Digitally controlled phase adjustment
- Three inputs (two differential/CMOS, one CMOS) with frequencies from 8 kHz to 1250 MHz (8 kHz to 300 MHz for CMOS)
- Any output frequency from <1 Hz to 1035 MHz
- Output jitter as low as 0.25 ps RMS (12 kHz–20 MHz integration band)
- Automatic self-configuration at power-up from internal EEPROM; up to four configurations pin-selectable
- Telecom timing cards for SONET/SDH, SyncE, wireless base stations, and other systems

ZL30622 Block Diagram

