Rad-Tolerant Current Mode PWM Controller

Description

The SGR1844/SGR1845 is fit, form and function compatible to the SG1844/SG1845 with the addition of guaranteed performance after radiation exposure to Total Ionizing Dose (TID), Enhanced Low Dose Rate Sensitivity (ELDRS), and Single Event Latch-up (SEL) conditions. The SGR1844/45 family of control ICs provides all the required features to implement off-line Fixed Frequency, Current-mode switching power supplies with a minimum number of external components. Current-mode architecture demonstrates improved line regulation, improved load regulation, pulse-by pulse current limiting and inherent protection of the power supply output switch.

The bandgap reference is trimmed to ±1% over temperature. Oscillator discharge current is trimmed to less than ±10%. The SGR1844/45 has undervoltage lockout, current-limiting circuitry and start-up current of less than 1mA. The totem-pole output is optimized to drive the gate of a power MOSFET. The output is low in the off state to provide direct interface to an N-channel device. Both operate up to a maximum duty cycle range of zero to <50% due to an internal toggle flip-flop which blanks the output off every other clock cycle. The SGR1844/45 is specified for operation over the full military ambient temperature range of -55°C to 125°C.

Features

- Optimized for Off-Line Control
- Low Start-Up Current (<1mA)
- Automatic Feed Forward Compensation
- Trimmed Oscillator
- Discharge Current
- Pulse-By-Pulse Current Limiting
- Enhanced Load Response
- Characteristics
- Undervoltage Lockout with 6V Hysteresis (SGR1844 only)
- Double Pulse Suppression
- High-Current Totem-Pole Output
- Internally Trimmed Bandgap Reference
- 500kHz Operation
- Undervoltage Lockout SGR1844 - 16 Volts SGR1845 - 8.4 Volts
- Low Shoot-through Current <75mA Over Temperature

High Reliability Features - SGR1844/SGR1845

- Rad-tolerance: (Test data available)
- TID to a Minimum of 100krad(Si) w/ 150krads overtest and 168 hours anneal
- ELDRS to a Minimum of 50krad(Si)
- SEL Immunity to a Minimum of 87MeV-cm^2/mg

Product Highlight

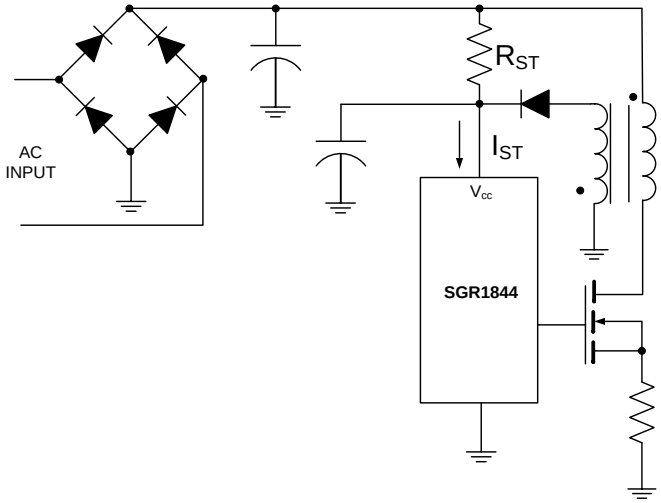
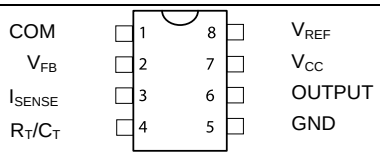
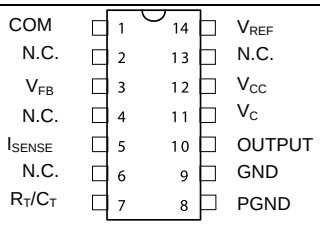
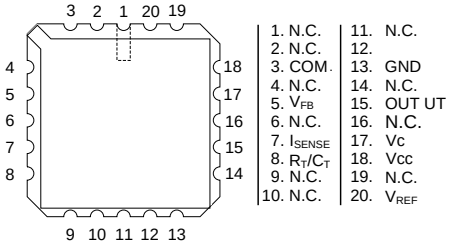
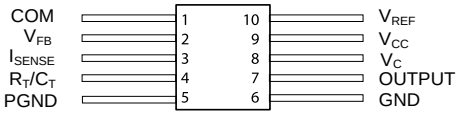


Figure 1 · Product Highlight

Connection Diagrams and Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type	Connection Diagram
-55°C to 125°C	Y	8-PIN CERAMIC DUAL INLINE PACKAGE	SGR1844Y SGR1844Y-EV* SGR1845Y SGR1845Y-EV*	CERDIP	 **Y PACKAGE** (Top View) PbSn Tin Lead Finish
	J	14-PIN CERAMIC DUAL INLINE PACKAGE	SGR1844J SGR1844J-EV* SGR1845J SGR1845J-EV*	CERDIP	 **J PACKAGE** (Top View) **PbSn** Lead Finish
	L	20-Pin CERAMIC LCC	SGR1844L SGR1844L-EV* SGR1845L SGR1845L-EV*	Ceramic (LCC) Leadless Chip Carrier	 **L PACKAGE** (Top View) PbSn Lead Finish
	F	10-PIN CERAMIC FLAT PACK PACKAGE	SGR1844F SGR1844F-EV* SGR1845F SGR1845F-EV*	FLAT PACK	 **F PACKAGE** (Top View) PbSn Lead Finish

* EV is Microsemi's "Equivalent V" flow that follows MIL-PRF-38535 requirements for Class V processing.

Absolute Maximum Ratings[1 - 2]

Parameter	Value	Units
Supply Voltage (Low Impedance Source)	30	V
Output Current (Peak)	±1	A
Output Current (Continuous)	350	mA
Output Energy (Capacitive Load)	5	µJ
Analog Inputs (V_{FB}, I_{SENSE})	-0.3 to +6.3	V
Error Amplifier Output Sink Current	10	mA
Operating Junction Temperature		
Hermetic (Y, J, L, F Packages)	150	°C
Storage Temperature Range	-65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	300	°C
RoHS / Pb-free Peak Package Solder Reflow Temp. (40 second max. exposure)	260 (+0, -5)	°C

Notes:
1. *Exceeding these ratings could cause damage to the device.*
2. *All voltages are with respect to Pin 5. All currents are positive into the specified terminal.*

Thermal Data

Parameter	Value	Units
Y Package:		
Thermal Resistance-Junction to Ambient, θ_{JA}	130	°C/W
J Package		
Thermal Resistance-Junction to Ambient, θ_{JA}	80	°C/W
F Package		
Thermal Resistance-Junction to Case, θ_{JC}	80	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	145	°C/W
L Package		
Thermal Resistance-Junction to Case, θ_{JC}	35	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	120	°C/W

Notes:
Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

Recommended Operating Conditions[3]

Symbol	Parameter	Recommended Operating Conditions			Units
		Min.	Typ.	Max.	
V_S	Supply Voltage Range		30		V
I_{PK}	Output Current (Peak)		±1		A
I_{OUT}	Output Current (Continuous)		200		mA
	Analog Inputs (Pin 2, Pin 3)	0		2.6	V
EA_{ISNK}	Error Amp Output Sink Current		5		mA
OSC_{FR}	Oscillator Frequency Range	0.1		500	kHz
R_T	Oscillator Timing Resistor	0.52		150	kΩ
C_T	Oscillator Timing Capacitor	0.001		1.0	µF
Operating Ambient Temperature Range:					
	SGR1844/45	-55		125	°C

Note:
3. Range over which the device is functional.

Electrical Characteristics

Unless otherwise specified, these specifications apply over the operating ambient temperatures for SGR1844/SGR1845 with -55°C ≤ T_A ≤ 125°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

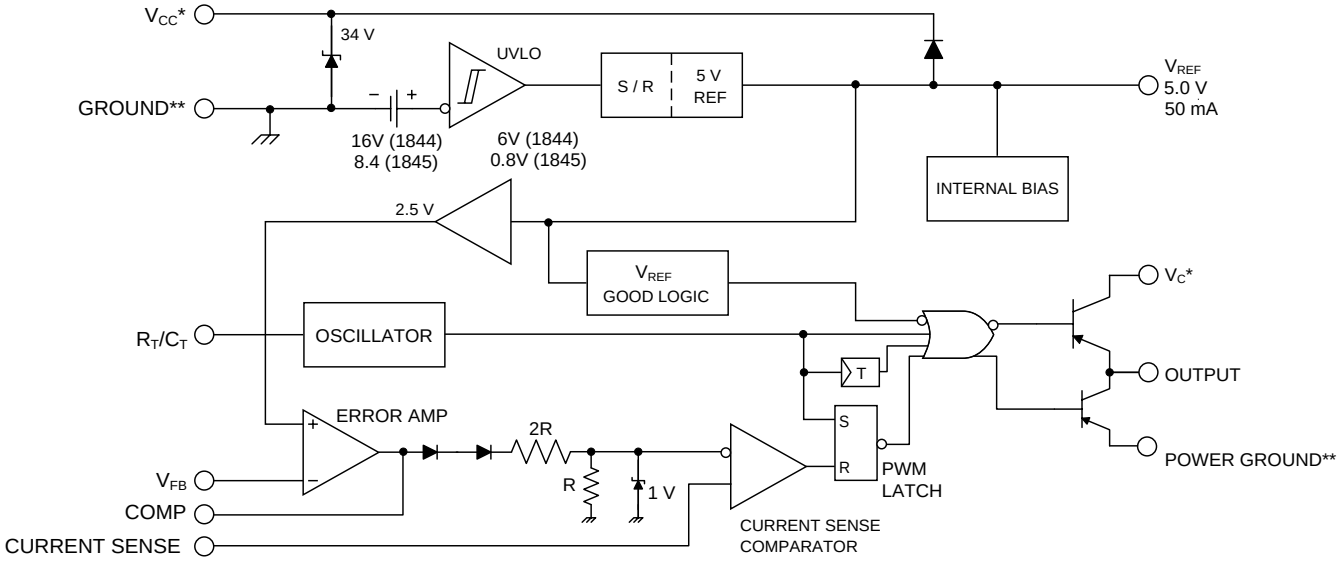
Symbol	Parameter	Test Condition	SGR1844/45			Units
			Min	Typ	Max	
Reference Section						
V_{REF}	Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	V
V_{REG}	Line Regulation	12V ≤ V_{IN} ≤ 25V		6	20	mV
I_{REG}	Load Regulation	1mA ≤ I_O ≤ 20mA		6	25	
	Temperature Stability[4]			0.2	0.4	mV/°C
	Total Output Variation[4]	Line, Load, Temperature.	4.90		5.10	V
V_N	Output Noise Voltage[4]	10Hz ≤ f ≤ 10kHz, T_J = 25°C		50		µV
	Long Term Stability[4]	T_A = 125°C,1000hrs		5	25	mV
V_{ISC}	Output Short Circuit		-180	-100	-30	mA
Oscillator Section[6]						
f	Initial Accuracy	T_J = 25°C	47	52	57	kHz
f_{REG}	Voltage Stability	12V ≤ V_{CC} ≤ 25V		.02	1	%
	Temperature Stability[4]	T_{MIN} ≤ T_A ≤ T_{MAX}		5		
OSC_{PP}	Amplitude	$V_{RT/CT}$ (Peak to Peak)		1.7		V
I_{DSG}	Discharge Current	T_J = 25°C	7.8	8.3	9.1	mA
		T_{MIN} ≤ T_A ≤ T_{MAX}	6.8		9.3	

Symbol	Parameter	Test Condition	SGR1844/45			Units
			Min	Typ	Max	
Error Amp Section						
EA_{IH}	Input Voltage	V_{COMP} = 2.5V	2.45	2.50	2.55	V
EA_{IIB}	Input Bias Current		-1	-0.3		µA
A_{VOL}	Open Loop Gain	2V ≤ V_O ≤ 4V	65	90		dB
EA_{BW}	Unity Gain Bandwidth[4]	T_J = 25°C	0.7	1		MHz
PSRR	Power Supply Rejection Ratio	12V ≤ V_{CC} ≤ 25V	60	70		dB
EA_{SNK}	Output Sink Current	V_{VFB} = 2.7V, V_{COMP} = 1.1V	2	6		mA
EA_{SRC}	Output Source Current	V_{VFB} = 2.3V, V_{COMP} = 5V		-0.8	-0.5	
EA_{VOH}	V_{OUT} High	V_{VFB} = 2.3V, R_L = 15k to GND	5	6		V
EA_{VOL}	V_{OUT} Low	V_{VFB} = 2.7V, R_L = 15k to VREF		0.7	1.1	
Current Sense Section						
CS_{AVOL}	Gain[5 - 6]		2.85	3	3.15	V/V
	Maximum Input Signal[5]	V_{COMP} = 5V	0.9	1	1.1	V
PSRR	Power Supply Rejection Ratio[5]	12V ≤ V_{CC} ≤ 25V		70		dB
CS_{IIB}	Input Bias Current		-10	-2		µA
CS_{DELAY}	Delay to Output[4]			150	300	ns
Output Section						
VOL	Output Low Level	I_{SINK} = 20mA		0.1	0.4	V
		I_{SINK} = 200mA		1.5	2.2	
VOH	Output High Level	I_{SOURCE} = 200mA	13	13.5		
		I_{SOURCE} = 200mA	12	13.5		
RS	Rise Time[4]	T_J = 25°C, C_L = 1nF		50	150	ns
FT	Fall Time[4]	T_J = 25°C, C_L = 1nF		50	150	ns
Under-Voltage Lockout Section						
UVLO	Start Threshold	1844	15	16	17	V
		1845	7.8	8.4	9.0	
V_{SMIN}	Min. Operation Voltage After Turn-On	1844	9	10	11	
		1845	7.0	7.6	8.3	
PWM Section						
DC_{MAX}	Maximum Duty Cycle		46	48	50	%
DC_{MIN}	Minimum Duty Cycle				0	
Power Consumption Section						

Symbol	Parameter	Test Condition	SGR1844/45			Units
			Min	Typ	Max	
I_S	Start-Up Current			0.5	1	mA
I	Operating Supply Current	V_{FB} = V_{ISENSE} = 0V		11	17	
Z	V_{CC} Zener Voltage	I_{CC} = 25mA		34		V

Note:
4. *These parameters, although guaranteed, are not 100% tested in production.*
5. *Parameter measured at trip point of latch with V_{VFB} = 0.*
6. *Gain defined as: $A = \Delta V_{COMP} / \Delta V_{ISENSE}$; $0 \le V_{ISENSE} \le 0.8V$*
7. *Adjust V_{CC} above the start threshold before setting at 15V.*
8. *Output frequency equals one half of oscillator frequency.*

Block Diagram



* - V_{CC} and V_C are internally connected for 8-pin packages.
** - POWER GROUND and GROUND are internally connected for 8-pin packages.

Figure 1 · Block Diagram

Characteristic Curves

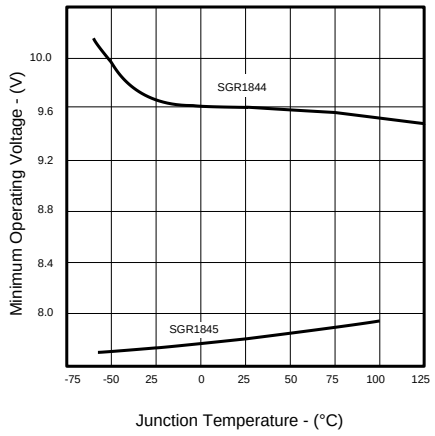


Figure 2 · Dropout Voltage vs. Temperature

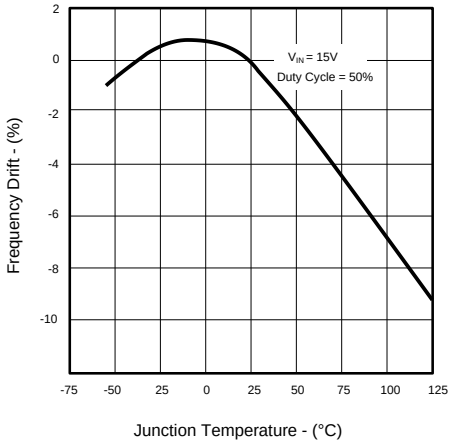


Figure 3 · Oscillator Temperature Stability

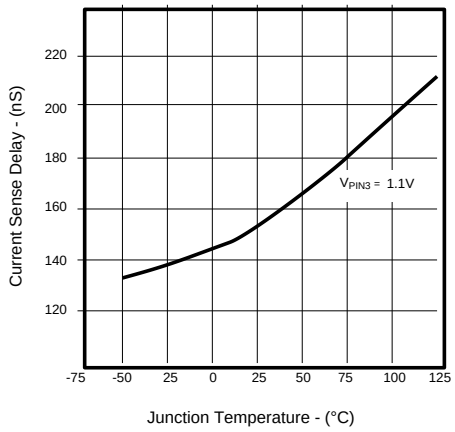


Figure 4 · Current Sense to Output Delay vs. Temperature

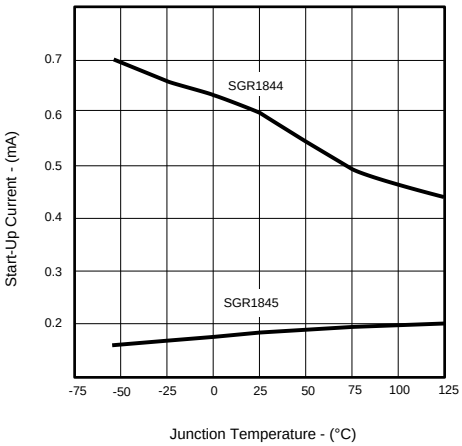


Figure 5 · Start-Up Current vs. Temperature

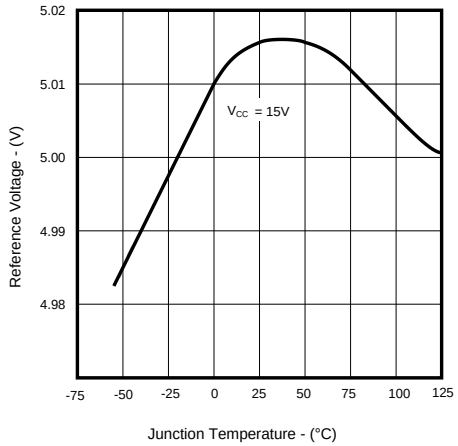


Figure 6 · Reference Voltage vs. Temperature

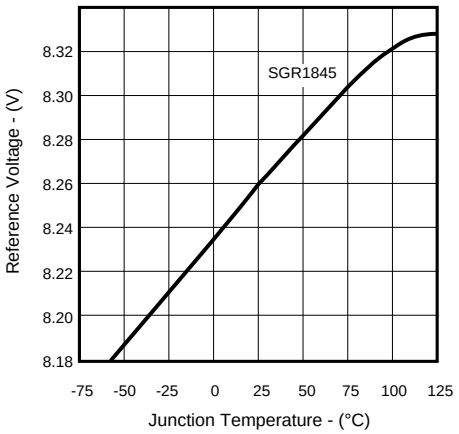


Figure 7 · Start-Up Voltage Threshold vs. Temperature

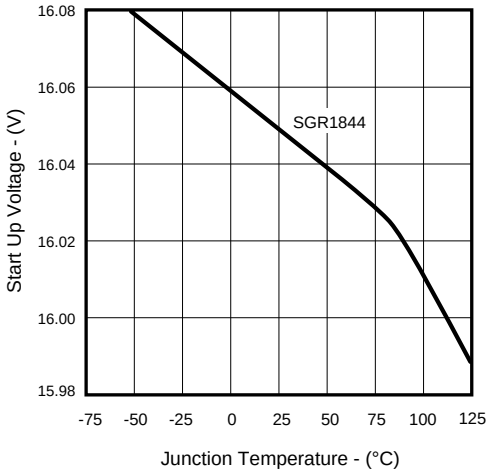


Figure 8 · Start-Up Voltage Threshold vs. Temperature

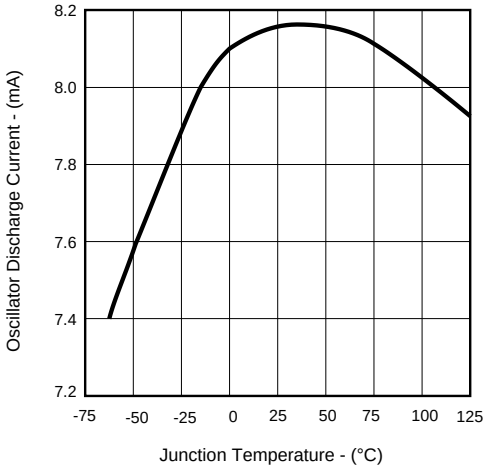


Figure 9 · Oscillator Discharge Current vs. Temperature

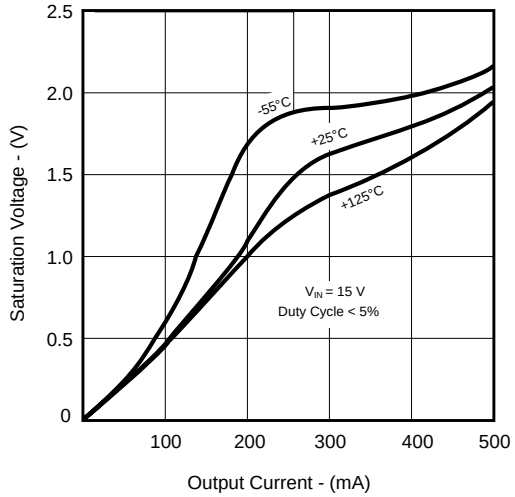


Figure 10 · Output Saturation Voltage vs. Output Current and Temperature (Sink Transistor)

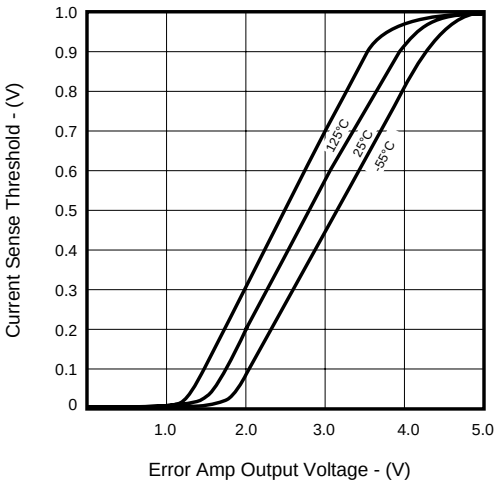


Figure 11 · Current Sense Threshold vs. Error Amplifier Output

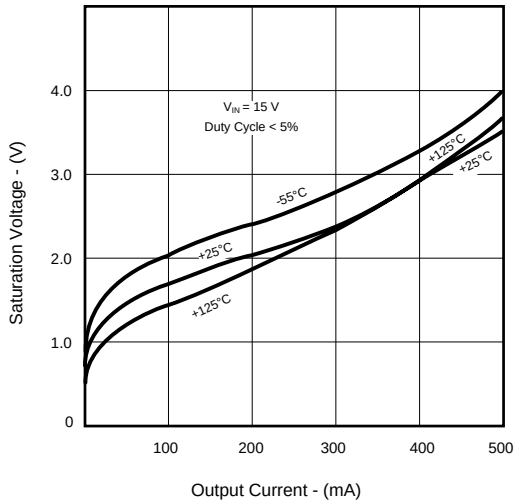


Figure 12 · Output Saturation Voltage vs. Output Current and Temperature (Source Transistor)

Application Information

The oscillator of the 1844/45 family of PWM's is programmed by the external timing components (R_T, C_T) as shown in Figure 14.

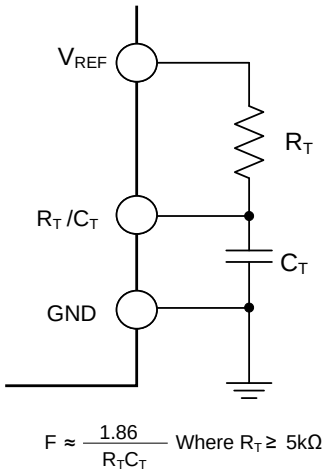


Figure 13 · Oscillator Timing Circuit

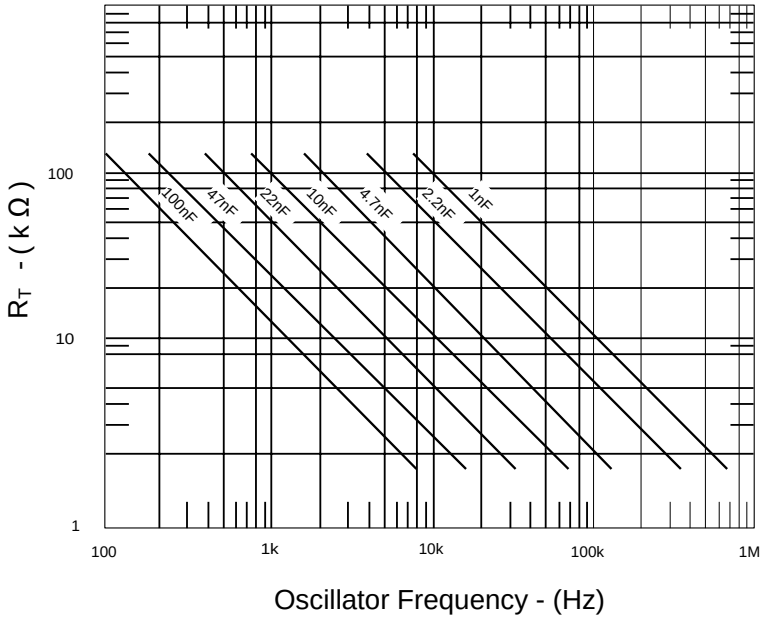


Figure 14 · Oscillator Frequency vs. R_T for various C_T

Typical Application Circuits

Pin numbers referenced are for 8-pin package and pin numbers in parenthesis are for 14-pin package.

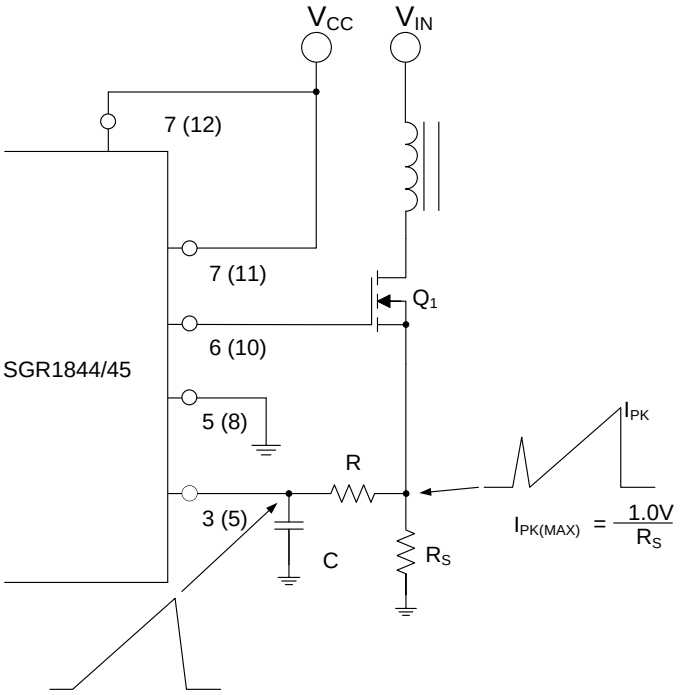


Figure 15 · Current Sense Spike Suppression

The RC low-pass filter will eliminate the leading edge current spike caused by parasitic of Power MOSFET.

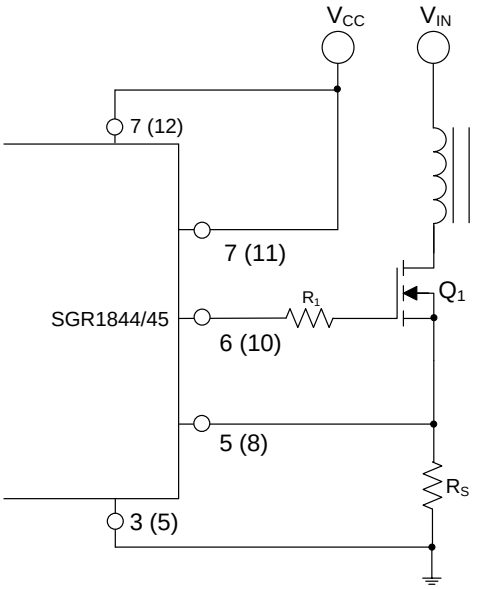


Figure 16 · MOSFET Parasitic Oscillations

A resistor (R1) in series with the MOSFET gate reduce overshoot and ringing caused by the MOSFET input capacitance and any inductance in series with the gate drive. (Note: It is very important to have a low inductance ground path to insure correct operation of the I.C. This can be done by making the ground paths as short and as wide as possible.)

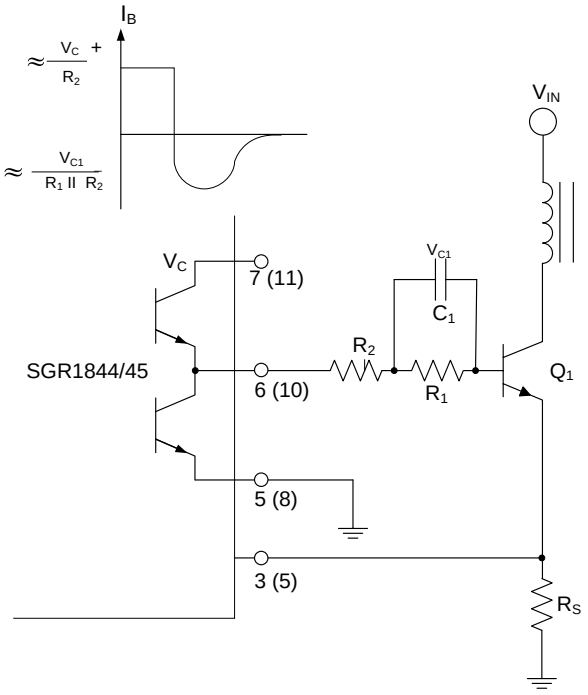


Figure 17 · Bipolar Transistor Drive

The 1844/45 output stage can provide negative base current to remove base charge of power transistor (Q_1) for faster turn off. This is accomplished by adding a capacitor (C_1) in parallel with a resistor (R_1). The resistor (R_1) is to limit the base current during turn on.

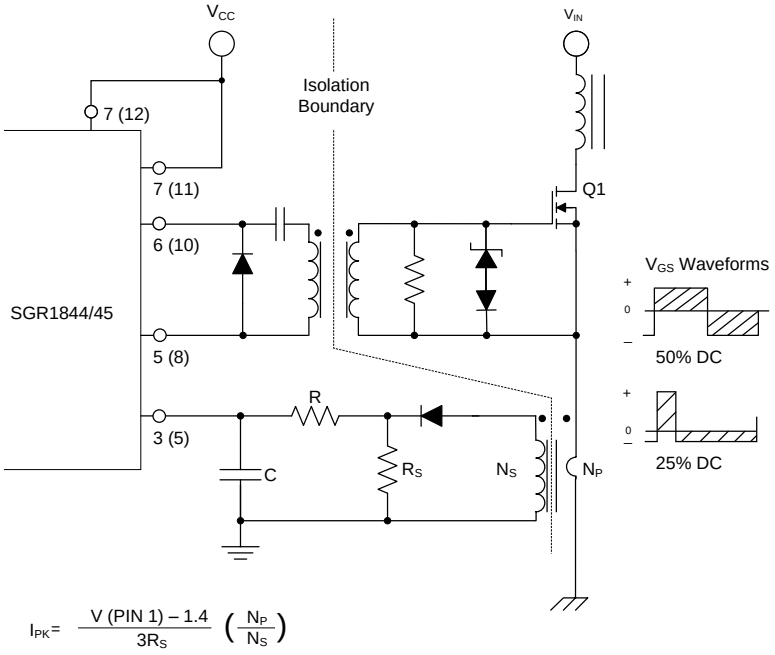


Figure 18 · Isolated MOSFET Drive

Current transformers can be used where isolation is required between PWM and Primary ground. A drive transformer is then necessary to interface the PWM output with the MOSFET.

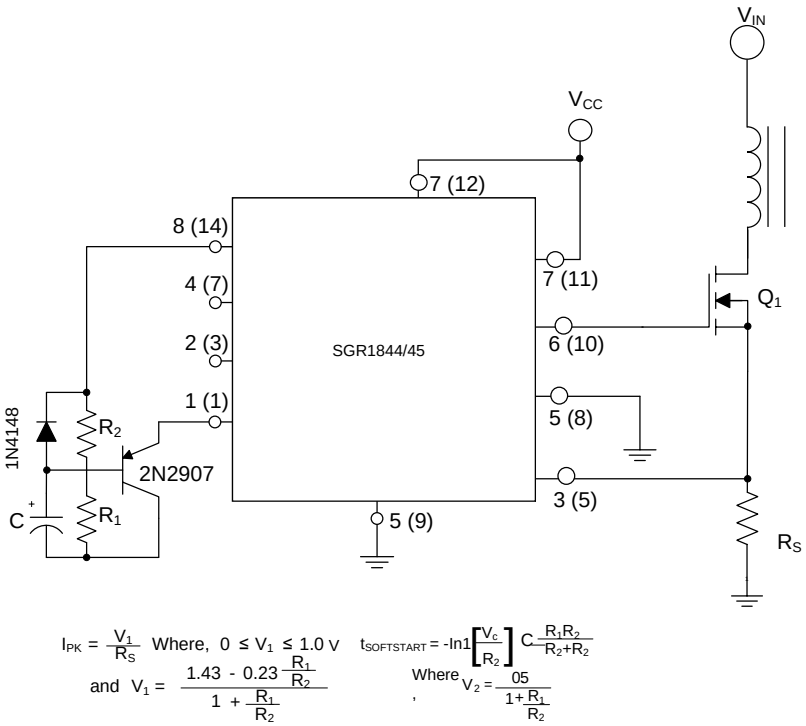


Figure 19 · Adjustable Buffered Reduction of Clamp Level with Softstart

Softstart and adjustable peak current can be done with the external circuitry shown above.

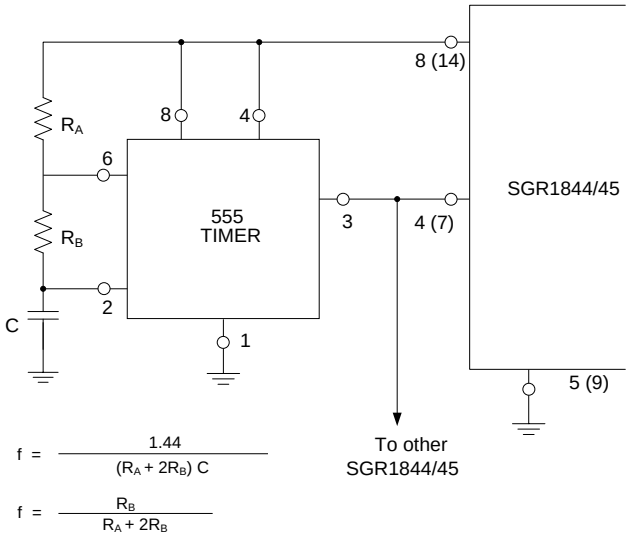


Figure 20 · External Duty Cycle Clamp and Multi-Unit Synchronization

Precision duty cycle limiting for a duty cycle of <50%, as well as synchronizing several 1844/45's is possible with the above circuitry.

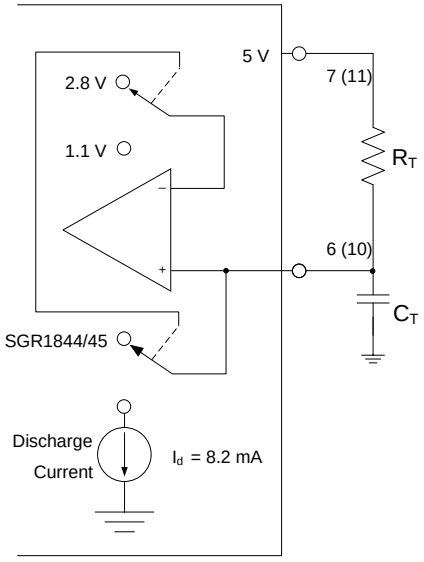


Figure 21 · Oscillator Connection

The oscillator is programmed by the values selected for the timing components R_T and C_T. Refer to application information for calculation of the component values.

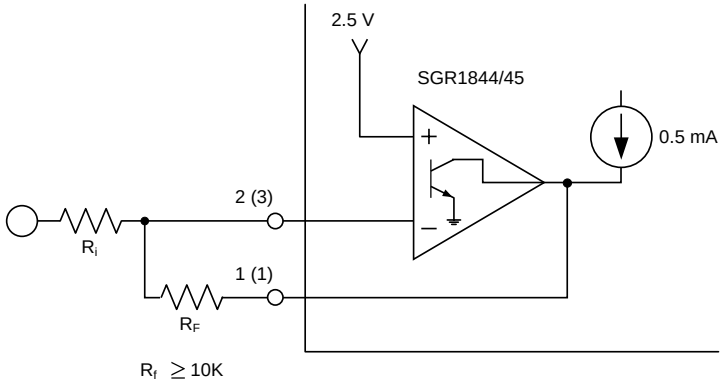
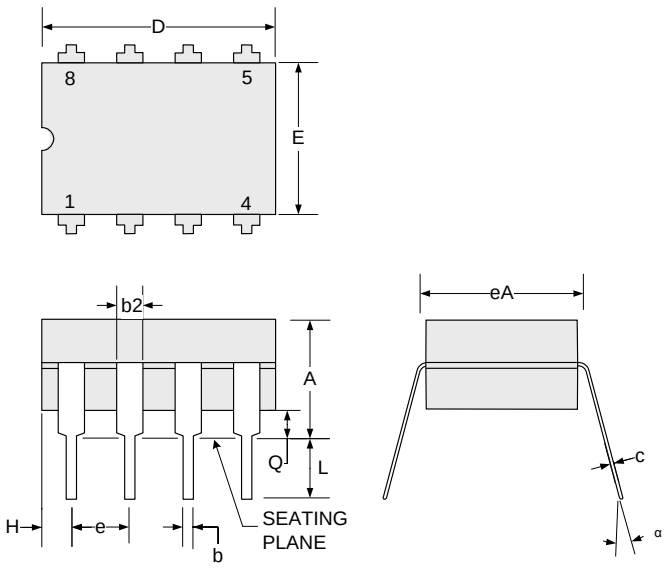


Figure 22 · Error Amplifier Connection

Error amplifier is capable of sourcing and sinking current up to 0.5mA.

PACKAGE OUTLINE DIMENSIONS

Controlling dimensions are in inches, metric equivalents are shown for general information.

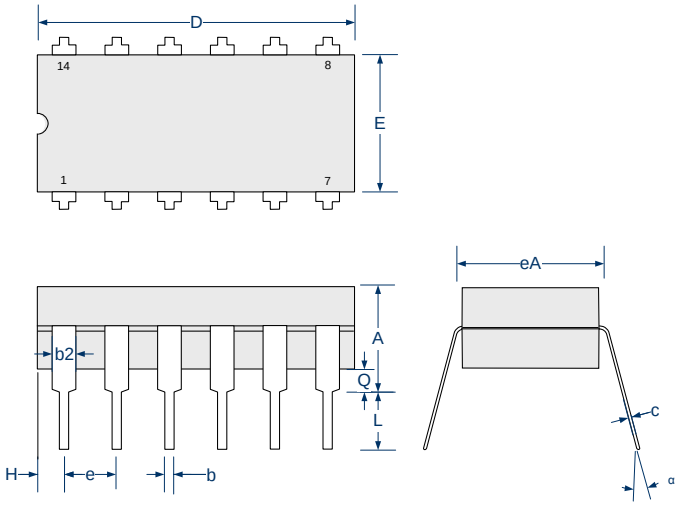


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.08	0.170	0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	9.52	10.29	0.375	0.405
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	4.06	0.125	0.160
α	-	15°	-	15°
Q	0.51	1.02	0.020	0.040

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.

Figure 23 · Y 8-Pin CERDIP Package Dimensions



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.08	0.170	0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	19.30	19.94	0.760	0.785
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	4.06	0.125	0.160
α	-	15°	-	15°
Q	0.51	1.02	0.020	0.040

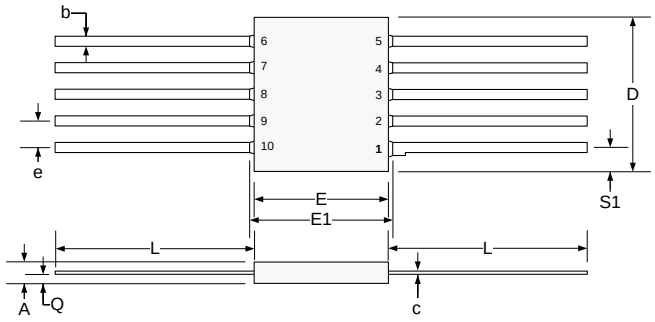
Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.

Figure 24 · J 14-Pin CERDIP Package Dimensions

PACKAGE OUTLINE DIMENSIONS

Controlling dimensions are in inches, metric equivalents are shown for general information.

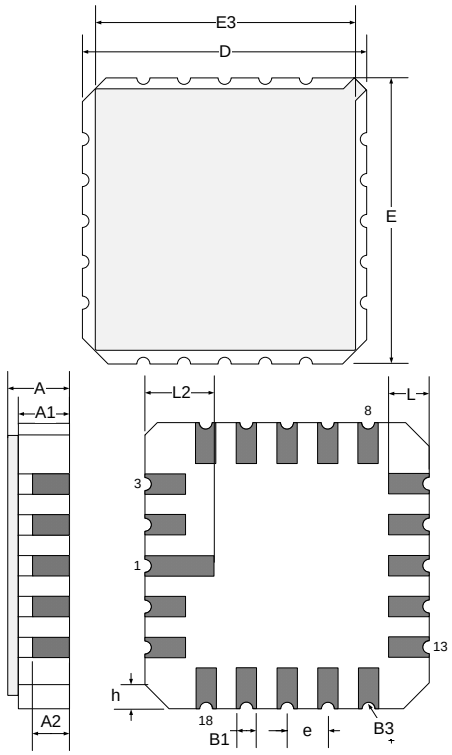


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.45	1.70	0.057	0.067
b	0.25	0.483	0.010	0.019
c	0.102	0.152	0.004	0.006
D	-	7.37	-	0.290
E	6.04	6.40	0.238	0.252
E1	-	6.91	-	0.272
e	1.27 BSC		0.050 BSC	
L	6.35	9.40	0.250	0.370
Q	0.51	1.02	0.020	0.040
S1	0.20	0.38	0.008	0.015

Note:

1. Lead No. 1 is identified by tab on lead or dot on cover.
2. Leads are within 0.13mm (.0005”) radius of the true position (TP) at maximum material condition.
3. Dimension “e” determines a zone within which all body and lead irregularities lie.

Figure 25 · F 10-Pin Ceramic Flatpack Package Dimensions



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
D/E	8.64	9.14	0.340	0.360
E3	-	8.128	-	0.320
e	1.270 BSC		0.050 BSC	
B1	0.635 TYP		0.025 TYP	
L	1.02	1.52	0.040	0.060
A	1.626	2.286	0.064	0.090
h	1.016 TYP		0.040 TYP	
A1	1.372	1.68	0.054	0.066
A2	-	1.168	-	0.046
L2	1.91	2.41	0.075	0.95
B3	0.203R		0.008R	

Note:

All exposed metalized area shall be gold plated 60 micro-inch minimum thickness over nickel plated unless otherwise specified in purchase order.

Figure 26 · L 20-Pin Ceramic Leadless Chip Carrier Package Dimensions

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