Fault Tolerant LEON3 Processor & SpaceWire Router Standard Products

Microsemi Space Forum Russia – November 2013

Sandi Habinc
Managing Director, Aeroflex Gaisler AB
Product Portfolio

- LEON3/LEON4 processors
  - Standard version
  - Fault Tolerant version
- LEON compatible IP cores
  - Floating Point Unit
  - Memory Management Unit
  - Memory controllers
  - Serial and parallel interfaces
- TSIM and GRSIM: LEON simulators
- GRMON: LEON debug monitor
- RTOS: VxWorks, ThreadX, Nucleus, LynxOS etc.
- LEON development boards
- Test equipment
- Software development environment based on open source tools
- Technical support and adaptations
LEON3 SPARC V8 Processor

Features

- IEEE-1754 SPARC V8 compliant, 32-bit processor
- 7-stage pipeline, multi-processor support
- Separate multi-set caches with LRU/LRR/RND
- On-chip debug support unit with trace buffer
- Highly configurable
  - Cache size 1-256 kByte, 1-4 sets, LRU/LRR/RND
  - Hardware Multiply/Divide/MAC options
  - MMU, FPU high-performance or small-size
  - Pipeline optimization for specific target technologies
  - Fault tolerance optimization for specific target technologies
  - 400 MHz on ASIC (130 nm, 400 MIPS, 400 MFLOPS, 25 kgates)
  - 20-30 MHz on Microsemi RTAX-S/SL FPGA
  - 25-35 MHz on Microsemi RT ProASIC®3 FPGA
- Certified SPARC V8 by SPARC International
- Suitable for space and military applications
- Baseline processor for space projects in US, Europe and Asia
SpaceWire Protocol and Interface

- The SpaceWire standard is a self-clocking serial protocol that provides a high speed, low power serial interface while offering a flexible simple user interface
- Protocol is derived from IEEE 1355-1995
- Current standard document is ECSS-E-ST-50-12C
- Physical layer is LVDS ANSI/TIA/EIA-644
  - On-chip or external LVDS drivers
  - Aeroflex SpaceWire Physical Layer Transceiver (UT200SpWPHY01)
- Industry standard protocol
  - Accepted by all major space organizations: NASA, ESA, JAXA, ISRO, KARI, IAI, ROSCOSMOS, etc.
  - 5th International SpaceWire Conference held in Sweden in June 2013
- Simple user interface
  - 9 or 10 bit transmit & receive on-chip FIFO memories are typical
  - Supports variable packet size and data rates
  - DMA interface, with support for RMAP or RMAP CRC acceleration
LEON3FT RTAX-S/SL & RT3PE

- **Processor Features**
  - 32-bit SPARC V8 processor implemented on RTAX2000S/SL and RT ProASIC3
  - LEON3FT processor core
    - Harvard architecture with separate caches:
      - 8 kByte Instruction Cache
      - 4 kByte Data Cache
    - Hardware multiply and divide
    - Power-down mode
    - On-chip debug support unit with 4 kByte trace buffer
    - IEEE-754 single/double precision Floating Point Unit (FPU)
    - SPARC Reference Memory Management Unit (MMU)
  - Fault tolerant design detects & corrects errors (SEU) in on-chip memory without any performance penalty or software interruption
  - SEU testing performed successfully (reported in 2005)
  - 20 MIPS and 4 MFLOPS @ 25 MHz
  - 25 MHz, 500 mW at 100% load, 380 mW in power-down
LEON3FT Peripherals

Peripheral Features

- Triple SpaceWire links with RMAP CRC and DMA
- Redundant MIL-STD-1553 BRM with DMA (based on Microsemi IP core)
- PCI Initiator / Target / Arbiter with DMA (based on Microsemi IP core)
- Dual 10/100 Mbit/s Ethernet MAC with DMA
- Redundant CAN-2.0 interface with SJA1000 software interface
- 8/32-bit memory controller for PROM, EEPROM, SRAM and SDRAM with ECC (BCH and Reed-Solomon)
- 32-bit Timer unit, UARTs with FIFO, 16/32-bit I/O port
- All IP cores SEU proof
The LEON3FT RTAX-S/SL and RT3PE architectures is based on a common design for all the different configurations, featuring a 32-bit AMBA AHB bus for high-speed communication and a 32-bit AMBA APB bus for peripherals and registers. Several cores are standard, such as the LEON3FT processor, but some are optional, such as the number of SpaceWire links.
### LEON3FT Configurations

- **Standard configurations**: Instrument Controller, Spacecraft Controller and Payload Controller

<table>
<thead>
<tr>
<th>Configuration / Feature</th>
<th>IC-1 CID-1</th>
<th>IC-2 CID-2</th>
<th>SC-1 CID-3</th>
<th>SC-2 CID-4</th>
<th>SC-3 CID-5</th>
<th>SC-4 CID-6</th>
<th>PC-1 CID-7</th>
<th>PC-2 CID-8</th>
</tr>
</thead>
<tbody>
<tr>
<td>LEON3FT</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>FPU</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>MMU</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Yes</td>
<td>Yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hardware Mul/Div</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Yes</td>
<td>Yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Debug Support Unit</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>UART Debug Link</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>JTAG Debug Link</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>On-chip Memory</td>
<td>4 kB</td>
<td>4 kB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SpaceWire Links</td>
<td>2</td>
<td>3</td>
<td>2</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mil-1553 RT</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mil-1553 BC/RT/MT</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CAN</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCI Initiator / Target</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Ethernet MAC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>Memory Controller</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>SDRAM support</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Standard peripherals</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Package</td>
<td>CQ352</td>
<td>CQ352</td>
<td>CQ352</td>
<td>CG624</td>
<td>CG624</td>
<td>CG624</td>
<td>CQ352</td>
<td>CQ352</td>
</tr>
<tr>
<td>Speed</td>
<td>24 MHz</td>
<td>25 MHz</td>
<td>24 MHz</td>
<td>25 MHz</td>
<td>25 MHz</td>
<td>25 MHz</td>
<td>25 MHz</td>
<td>25 MHz</td>
</tr>
</tbody>
</table>

Radiation Tolerant SpaceWire Router

- Compliant with ECSS-E-ST-50-12C
- Configuration port using RMAP ECSS-E-ST-50-52C
- Wormhole Routing
  - Non-blocking switch-matrix connecting any input to any output
  - Path, Logical and Regional Logical addressing
  - Group Adaptive Routing
  - Packet Distribution
  - Priority levels for output port arbitration
- SpaceWire ports, up to 8 external
  - Up to 200 Mbit/s in both directions per link
  - Support for on-chip or off-chip LVDS
- FIFO ports, 2 external, 9-bit wide, cascadable
- AMBA ports, 2 internal with DMA and RMAP
- PCI initiator and target with DMA, 32-bit, 33 MHz
- System-time distribution via all ports
- Timers on all ports to prevent deadlock
# SpaceWire Router Configurations

<table>
<thead>
<tr>
<th></th>
<th>RT-SPW-ROUTER-10X</th>
<th>RT-SPW-ROUTER-6X</th>
</tr>
</thead>
<tbody>
<tr>
<td>SpaceWire ports</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>FIFO ports</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>AMBA ports with RMAP</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>Configuration port with RMAP</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Configuration port with AMBA</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>PCI Initiator/Target</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>AMBA status</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>UART/JTAG Debug Link</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>FPGA</td>
<td>Microsemi RTAX2000S(L) CQFP352,CCGA624</td>
<td>Microsemi RTAX2000S(L) CQFP352,CCGA624</td>
</tr>
<tr>
<td></td>
<td>Microsemi RT3PE3000L CCGA484</td>
<td></td>
</tr>
<tr>
<td>SpaceWire physical interface</td>
<td>LVTTL</td>
<td>LVTTL</td>
</tr>
<tr>
<td></td>
<td>LVDS</td>
<td>LVDS</td>
</tr>
</tbody>
</table>
GR701A PCI to SpW, 1553B and CAN

- GR701A companion chip for processors and PCI systems implemented on RTAX2000S/SL FPGA
- PCI bus Initiator and Target, 32-bit, 33 MHz
- 3 SpaceWire links with RMAP, 80 Mbit/s
- Redundant MIL-STD-1553 BRM
- 16 kByte EDAC protected on-chip SRAM
- 8-bit EDAC protected bus to external memory
- 2 UART/RS232
- 16-bit I/O port
- Timers and watchdog
- CQFP352 package
GR703 Telemetry & Telecommand

- GR703 companion chip provides PCI based processors with SpaceWire interfaces and CCSDS telemetry encoding and telecommand decoding capabilities, such as protocol sub-layer handling, Reed-Solomon and convolutional encoding, BCH decoding, pseudo-randomization.

- CCSDS TM/TC ground station / EGSE available for development and testing.
Example System with FPGAs

- The FPGAs presented herein can be combined in many different constellations to compose a desired on-board data handling or payload processing system.

- An example is shown hereunder where the 32-bit PCI bus is used to interconnected a main processor chip with various companion chips to form a data handling system.
Supported RTAX-S/SL Devices

- LEON3FT-RTAX-S/SL, RT-SPW-ROUTER, GR701A and GR703 delivered in all quality levels as pre-programmed off-the-shelf components
- All LEON3FT-RTAX-S/SL standard configurations available now
- RT-SPW-ROUTER 10x and 6x configurations available now
- Hi-rel parts available in CQFP352 and CCGA624 packages
- Low-cost prototypes on AX2000/FBGA896 are available using an adapter

- Prototyping board for RTAX2000S/CCGA624 or AX2000/FBGA896 is available from Aeroflex Gaisler
Supported RT ProASIC3 Devices

- LEON3FT-RT3PE and RT-SPW-ROUTER delivered in all quality levels as pre-programmed off-the-shelf components

- All LEON3FT-RT3PE standard configurations available now

- RT-SPW-ROUTER 10x configuration available now

- Hi-rel parts available in CCGA484 packages

- Low-cost prototypes on ProASIC3L/FBGA484

- Prototyping board is available from Aeroflex Gaisler

- Support for FlashPro4 cable for programming and software debugging with GRMON
Custom Configurations

- All our LEON3FT and SpaceWire products are based on GRLIB VHDL IP core library, which is a complete System-on-a-chip design environment available for end-user development:
  - Processors
  - Peripherals
  - Memory controllers
  - Serial and parallel high speed interfaces
  - AMBA on-chip bus with Plug & Play support
  - Fault tolerant and standard version
  - Support for many tools & prototyping boards
  - Support for portability between technologies

- Custom LEON3FT configurations based on the current architecture are possible (additional NRE)

- Aeroflex Gaisler can also integrate customer-furnished IP cores

- Flexible licensing (per FPGA or project)
LEON3 Operating Systems

- LEON3 is supported by several open-source kernels:
  - eCos, RTEMS, Pthreads, uCLinux, Linux 2.6
  - GNU GCC-3.4.4 compiler and associated tools
  - Eclipse IDE available for RTEMS and Pthreads

- LEON3 port and BSP available for VxWorks 5.4 & 6.X
- LEON3 port and BSP available for ThreadX-5.0
- LEON3 port and BSP available for Nucleus
- LEON3 port and BSP available for LynxOS

- Software drivers available for SpaceWire, MIL-STD-1553, CAN, Ethernet, PCI, etc.
- Support for Windows and LINUX hosts
Development Tools

- **GRMON hardware debug monitor:**
  - Supporting all kernels/compilers
  - Command line or Eclipse RCP
  - GDB remote debug support

- **TSIM behavioral simulator:**
  - Single-core LEON2/LEON3
  - Code coverage, profiling, back trace
  - I/O emulation
  - High-performance (> 20 MIPS)
  - Command line or Eclipse IDE
  - GDB remote debug support

- **GRSIM behavioral simulator**

- **Support for Windows and Linux**
Conclusions

- LEON3FT-RTAX-S/SL and LEON3FT-RT3PE:
  - flexible solution for platform, payload and instruments

- RT-SPW-ROUTER 10x and 6x SpaceWire router:
  - a new solution for networking
  - 200 Mbit/s in both directions
  - 16x router through bridging without any extra glue logic

- TID and SEU performances compatible with all missions

- Quick turn-around time for custom configurations

- Lower-cost prototype solutions available

- Higher performance, lower power and price

- Global acceptance by customers