# Introduction

This application note provides detailed information and circuitry design guidelines for the implementation of a 48-port Power over Ethernet (PoE) system, based on Microsemi's™ 12-channel PoE manager-PD69012, using a $I^2C$ interface for communication with hosting system. This document enables the designer to integrate PoE capabilities, as specified in the IEEE standard 802.3af and IEEE802.3at-2009, into an Ethernet switch.

The PD69012 PoE manager implements real time functions as specified in the IEEE 802.3af and IEEE802.3at-2009 standard including detection, classification and port-status monitoring, as well as system level activities such as power management and MIB (Management Information Base) support for system management. The PoE manager is designed to detect and disable disconnected PDs (Powered Devices), using both DC and AC disconnection methods, as specified in the standard.

This application note should be used in conjunction with *Application Note 175, Catalogue Number 06-0055-080 for Layout Design Guidelines*. For easier design and development an Evaluation Board (P/N PD-DB-7424A, 24 ports EVB (evaluation board)) can be ordered.

# Applicable Documents

- IEEE 802.3af-2003 standard, DTE Power via MDI
- IEEE802.3at-2009 standard, DTE Power via MDI
- PD69012 Data Sheet, Catalogue Number 06-0069-058
- Application Note 175 - Layout Design Guidelines for PoE Systems, Catalogue Number 06-0055-080
- PD-IM-7400 Evaluation Board User Guide Catalogue Number 06-0025-056
- Auto Mode User Guide Catalogue Number 06-1200-056
- Tech Note 144 – Emergency Power Management Catalogue Number 06-0028-081

# Background

The PD69012 enables two operation modes:

- **Auto mode (Automatic operation)** provides a basic set of features in a stand-alone application (no need for a local PoE Controller).
- **Enhanced mode** provides enhanced features using a local dedicated PoE Controller (PD69000).

This application note defines Auto mode operation. In this configuration, the PoE managers communicate directly with a Host CPU.

# Auto Mode Features

- IEEE 802.3af compliant
- IEEE802.3at-2009 compliant
- IETF Power Ethernet MIB (RFC 3621) compliant
- Can be cascaded for up to eight PoE managers, 96 ports
- Pre-standard PD detection
- Detection of Cisco devices
- $I^2C$ bus for External interface communication
- Supports EPROM interface for parameters configuration (optional)
- Advanced power management; up to 96 ports
- User friendly PoE communication protocol
- Continuous voltage and current monitoring per port and per system
- Thermal monitoring and protection
- Parameter setting per port and per system
- Disables ports
- Built in 3.3v regulator
- Internal power on reset
- Interrupt out
- Port LEDs support
- Emergency power management
- RoHS compliant

# Integration

The system described is destined for a 48-port switch.

The same design can be applied to 1 to 8 PoE managers controlling 12 ports each (12 ports to 96 ports, in multiples of 12).

The PoE system daughter board can be easily integrated on top of a switch and provide the capability to add any PoE application while using a different daughter applications (Enhanced or Auto mode). Refer to Figure 1.

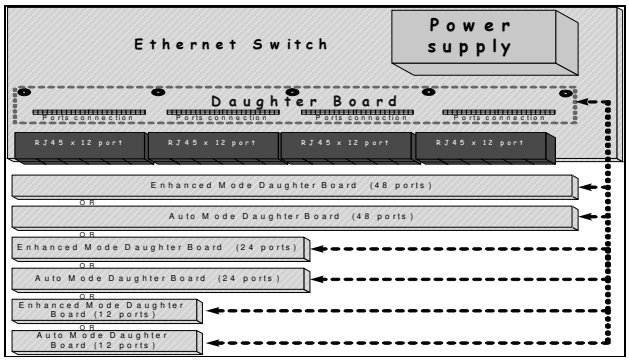


**Figure 1: PoE Daughter Board Integration**

# Overall Description

The circuit includes the following blocks (Figure 2):

- PoE circuit for 48 ports based on four PD69012s
- Communication interface and isolation circuits

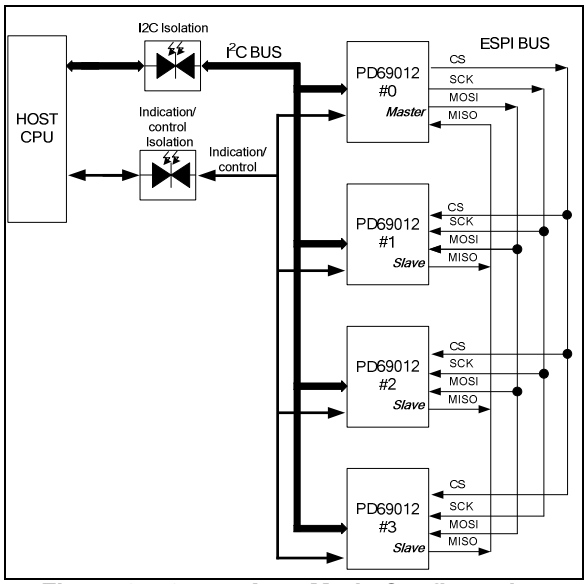


**Figure 2: 48-port Auto Mode Configuration**

# General Circuit Description

The 48-port configuration for a PoE system shown in Figure 2 comprises four PoE managers circuits (PD69012s), communicating with a Host CPU via an isolated I²C bus. The ESPI bus is dedicated for internal communication amongst the PD69012s (for power management).

Any PD69012device can be configured as a Master, while the other devices are configured as Slaves, using the ASICINI input.

This Master/Slave configuration only affects the Enhanced Serial Parallel Interface (ESPI) bus. To avoid ESPI clock and data I/Os contentions it is critical that only one of them be configured as the Master, and all other devices should be configured as Slaves.

## Communication Interfaces

Communication between the Host CPU and the local PoE managers is performed via an isolated I²C interface. Each PD69012 can be individually addressed by setting the address of the device. This is done by selecting the R83 value (Figure 7).

For more information, refer to the *Auto Mode User Guide Catalogue Number 06-1200-056*.

## ESPI Bus

The ESPI, bus used for internal communication, includes the following lines:

- **MOSI (Master Out/Slave In)**: Provides communication from the Master PD69012 to the Slave PD69012s.
- **MISO (Master In/Slave Out)**: Provides communication from the PD69012s to the PoE Controller.
- **SCK**: Serial clock generated by the Master PD69012.
- **CS (Chip Select)**: Utilized by the Master PD69012 to send data to all the Slaves PD69012s simultaneously. However only the selected PD69012 responds.

## Control

Refer to Figure 3.

- An **xReset_IN_isolated** control signal driven by the Host CPU is utilized to reset the PoE system.
- An **xDisable_ports_isolated** control signal driven by the Host CPU is utilized to disable all PoE ports at once.

### Indications

Refer to Figure 3.

To indicate PoE events, the PoE manager produces an **xInt_out_isolated** interrupt signal.

### Communication Flow

Communication between the Host CPU and the PoE Managers is performed via I2C communication.

Commands are mapped in registers and include all the MIB functionality. Communication between the Host CPU and a specific PD69012 is managed by setting the PoE Manager I2C address.

The Host CPU issues commands via an isolated I/O lines to the PoE Managers. This isolation is a basic IEEE PoE standards requirement. For more information, refer to the *Auto Mode User Guide Catalogue Number 06-1200-056*.

### Main Supply

The PoE system operates within a range of 44 to 57 V (802.3at port's range 50 to 57 V). To comply with UL SELV regulations, maximum output voltage should not exceed 60 V.

When utilizing the DC Disconnect function, the PoE system can operate over up to 57 V. However, the AC Disconnect function requires a 5 V level to be added to the supply voltage (55 + 5 = 60 V).

Therefore, the maximum input voltage should not exceed 55 V. The supplied voltage must be isolated from the Switch supply and chassis by 1500 Vrms.

### Grounds

The system utilizes several grounds:

- Chassis
- Digital
- Analog

The chassis ground is connected to the switch's chassis ground. This ground plane should be 1500 Vrms isolated from the PoE circuitry.

The digital and analog grounds are electrically the same ground. However, to reduce noise coupling, the grounds are physically separated and connected only at a single point.

This is further detailed in the *AN-175 Application Note Catalogue Number 06-0055-080*.

### 3.3 V Regulator

Each of the PD69012s has a 3.3 V regulator (EXT_REG & VPERI), providing up to 6 mA.

This current is utilized for powering components external to the PoE domain; those components must also be isolated by 1500 Vrms from the switch circuitry.

An external transistor can be added to the output to increase the current. Q1 (Figure 6) can provide up to 30 mA to the opto-couplers in the interface circuitry.

## Detailed Circuit Description

The following sections describe the Overall Block Diagram (Refer to Figure 6).

### Communication Interface

There is a single communication interface in this circuitry, between the Ethernet switch and the PoE managers. This interface is a 1500 Vrms isolation I²C interface. Note that each side of the circuitry is fed by a separate power supply. The isolation circuit is detailed in Figure 6.

### Control and Indication Signals

Refer to Figure 3.

The Control/Indication signals are "single H/W lines" type, running between the Host CPU and the PoE System. These signals are optically coupled to achieve 1500 Vrms isolation.

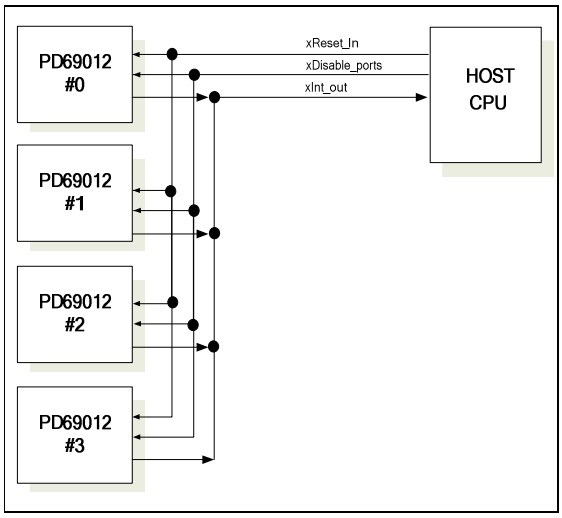


**Figure 3: Control and indication Signals**

## Control Signals

There are two control lines driven by the Host CPU to the PoE managers:

- **xDisable_ports_isolated**: Disables all PoE ports immediately.
- **xReset_IN_isolated**: Driven by the hosting system to reset the PoE system

## Indication Signal

The **xint_out** interrupt signal, which originates from the PoE managers, indicates events including Port On, Port Off, Port Fault, PoE manager Fault, and Voltage Out of Range. For full list of interrupt events, refer to *Auto Mode User Guide Catalogue Number 06-1200-056*.

## PoE Manager Circuitry

Refer to Figure 7.

The PD69012 performs a variety of internal operations and PoE functions, requiring a minimum of external components.

Each PD69012 handles up to 12 ports. Figure 7 shows the PoE manager #0 with its related components for a 12-port configuration.

**Note** For the solution described in this Application Note (48-port), multiply the circuitry in Figure 7 four times.

## Auto Mode Configuration

This configuration is set by R3/R92 divider tied in to the ASICINI line (R3/Figure 6).

In Auto Mode operation, the divider's voltage value configures the PoE manager to Master and Slave1 - Slave7 as specified in the following table:

| ASIC_INI | Minimum Voltage | Maximum Voltage | Resistors Value | |
|---|---|---|---|---|
| | | | R92 (low) | R3 (high) |
| Master | 0 | 0.14 | 10000 | 309000 |
| Slave1 | 0.35 | 0.44 | 10000 | 52300 |
| Slave2 | 0.51 | 0.6 | 10000 | 34800 |
| Slave3 | 0.67 | 0.75 | 10000 | 24900 |
| Slave4 | 0.83 | 0.9 | 10000 | 18700 |
| Slave5 | 0.99 | 1.06 | 10000 | 14300 |
| Slave6 | 1.15 | 1.21 | 10000 | 11300 |
| Slave7 | 1.3 | 1.36 | 10000 | 8870 |

## Line Detection Calibration

When performing line detection procedure, the PoE manager utilizes certain voltage levels over the output port.

To accurately set these levels, reference voltages are developed across the parallel combination of R90 and R91.

This combination simulates the equipment tied in to the port.

## Reference Current Source

The reference for internal voltages within the PD69012 is set by a precision resistor (R87).

## Charge Pump

An increase of 5 V over the power supply main input (44 to 55V, + 5V) is required.

The 5 V increase is implemented by a Charge-Pump circuitry that utilizes three elements as follows:

- A self-sustaining clock mechanism, utilized to start and keep the process going. This is performed internally in the PD69012.
- Energy transfer element (C63 and C66).
- Switching diode to constrain the energy flow in one direction (D53).

## Sense Resistors

A 500 mΩ (or 487 mΩ), (1%) sense resistor is connected to the port output line. This resistor measures the port current.

The resistor with its traces resistance should be close to 500 mΩ. For more information, refer to the *Layout Design Guidelines Catalogue Number 06-0055-080*.

## Protection Fuse for Abnormal Operating Voltage

Any IC that experiences input voltage above its absolute maximum rating will incur unexpected damage. Since the PoE manager is connected to a high current source, it is best design practice to use a protection fuse (F49) to avoid high current paths during PSU over voltage faults.

## Low Pass Filter

Each of the output ports includes provisions against external discharges that may damage the PD69012.

C59 and R85 create a path to the ground to limit damaging potentials (for the PoE manager #0 circuitry).





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## LED Support

Refer to Figure 4.

LED support for port status indication is accomplished by utilizing the dedicated LEDs support bus as follow:

- 'LED_SCK_Auto_Mode_Master/Slave_0/1/2'
- 'LED_DATA_Auto_Mode_Master/Slave_0/1/2'
- 'xLED_Latch_Auto_Mode_Master/Slave_0/1/2'

These signals control the LEDs and indicate the port status (each PD69012 indicates its corresponding PoE ports only).

**Note** **xLED latch_Auto_Mode_Master/Slave** 0/1/2 output signals are open drain logic.

Bus behavior is synchronous serial communication in one direction (write only), 15,625 b/s (default value), transmitting the status of each PoE manager accordingly.

The packet is transmitted with Start and End header bytes. For more details, refer to *Technical Note 118 Catalogue Number 06-0008-081*.

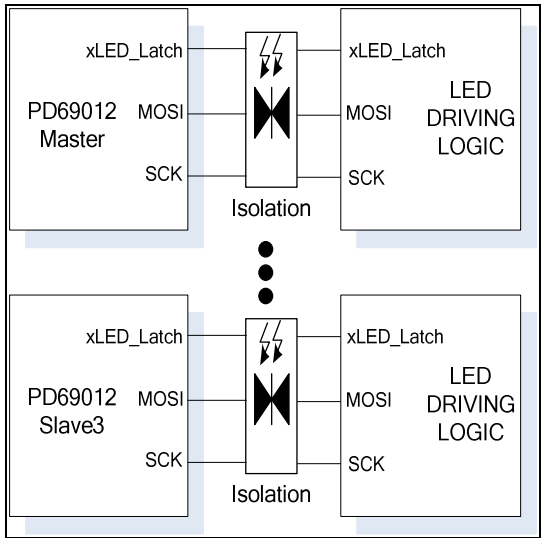


**Figure 4: SPI Bus and LED Support**

## Emergency Power Management

PoE circuits can be powered by up to three separate power supplies (see Figure 5). It is recommended that each power supply be able to generate a logic signal, indicating its operate/fail status. Two logical outputs can be derived from the PSU:

- **xPower good signal (default)**:
  PG = '0' logical, indicating operational power supply
  PG = '1' logical, indicating failed power supply
  (In this mode, R7 should not be connected and R6 should be connected).
- **Power good signal**:
  PG = '1' logical, indicating operational power supply
  PG = '0' logical, indicating failed power supply
  (In this mode, R6 should not be connected and R7 should be connected).

The PoE circuit allocates power to the system in accordance with the overall available power, derived from logic signals coming from the power supplies. With three power supplies having up to three different output power levels, up to eight power banks can be derived from their combinations. The utilized pins are as specified below:

| Pin Number | Signal | Remarks |
|---|---|---|
| #18 | PG0_PoE_manager | Power Good 0 |
| #19 | PG1_PoE_manager | Power Good 1 |
| #20 | PG2_PoE_manager | Power Good 2 |

If the PG pin is not used, the pin must be connected to the GND or Vperi (according to the appropriate PG logic) with no resistor. Figure 5 describes the connections between the power supplies' logic signals and the PoE managers.

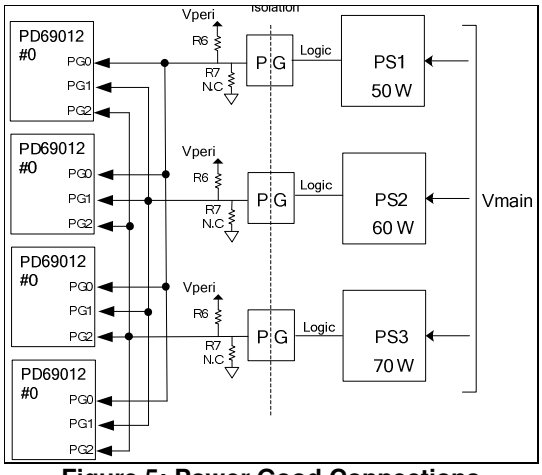


**Figure 5: Power Good Connections**

For isolation requirement destined for Emergency Power Management, refer to *Technical Note-144 Catalogue Number 06-0028-081*, section "Isolation Requirements".

## Front-end Circuitry

Refer to Figure 8.

This circuit is an analog front-end circuit, destined for a single port. For this Application Note, the circuit is to be multiplied up to 48 times in accordance with the number of PoE ports in the system.

## Output Ports

Refer to Port 0.

The output port circuitry is shown in Figure 8. Note that R19 (46.4k) is of the same value as the resistor used as the line detection calibration resistor R90 (see Figure 8). In turn, each port is supplied with a constant current across this resistor.

The load resistance of the PD attached to the port is calculated in parallel with R19. The resulting voltage developed across both resistances is compared to the calibration source (R90 || R91) voltage, so as to establish the validity of the terminal.

Other components are used for the following purposes:

- D1 is a polarity reversal diode, used to prevent application of reversed voltage from an external source.
- C4 forms a noise suppression component.
- F1 is a current limiting device, operating as specified in the IEC 60950-1:2001 requirements. The fuse is not required if the power supply is below 100 W.

**Note** If the output port circuitry is not fully populated, for example 10 ports instead of 12, the unused spare two ports are to be wired as follows: **PORT_SENSE** and **FET_G** should be tied to the **AGND** and **VPORT_NEG** should be tied to the **Vmain nets**. The above is applicable when no Rsense resistor is assembled on the board. There is no need to assemble the following items for unused channels: Q2, C4, F1, D1 and R19.

**I²C Interface Circuitry (see Figure 11)**: The I²C isolation circuitry comprises isolators provide the 1500 Vrms isolation required by the IEEE 802.3af-2003Standard.

This circuit supports:

- Data rate up to 400 kb/s
- SDA I/O signal
- SCL clock

In designing the system, it is critical that separate power supply sources for each side of the circuitry are used.

The PoE side of the isolating circuit is fed by the VPERI potential, derived from PoE manager #0 and driver (Q1).

The Ethernet switch side of the circuitry is derived from a 3.3 or 5 V potential generated by the switch.

I²C communication between the Host CPU and the PoE managers is managed by setting the address of the PoE manager. This is done by selecting the value of R83. This resistor sets the analog level into pin #53 (I2CINI), as specified in the following table.

| I2CINI | Address (hex) | R306 (ohms) | I2C Address | Address (hex) | R306 (ohms) |
|---|---|---|---|---|---|
| #0 | 0 * | 309000 | #8 | 40 | 8870 |
| #1 | 8 * | 93100 | #9 | 48 | 6810 |
| #2 | 10 | 52300 | #10 | 50 | 5230 |
| #3 | 18 | 34800 | #11 | 58 | 3920 |
| #4 | 20 | 24900 | #12 | 60 | 2800 |
| #5 | 28 | 18700 | #13 | 68 | 1870 |
| #6 | 30 | 14300 | #14 | 70 | 1020 |
| #7 | 38 | 11300 | #15 | 78 | 324 |

* These addresses are General Call address and should not be used.

For more information, refer to the *PD69012 Data Sheet, Catalogue Number 06-0069-058*.

## Ground Interface Connection (AGND)

The power supplies' ground connector J1 (see Figure 6) enables the current path back to the power supply. The ground connection should be capable of carrying all the strings current back to the power supplies.

# Thermal Design

The design for 802.3at PoE standard should take into account power dissipation of the PoE manager, power dissipation of the associated circuitry and the maximum ambient operating temperature of the switch.

Adequate ventilation and airflow should be part of the design to avoid possible thermal over-stress on the following areas:

## PD69012 Maximum Operating Temperature

PoE design should ensure that the PD69012's maximum operating junction temperature PD69012 (150° C) is not exceeded under worst case conditions.

Worst case conditions typically involve operation under maximum ambient temperature, output ports fully loaded at 802.3at power and all other unit functions are fully operational. The *PD69012 Data Sheet, Catalogue Number 06-0069-058* contains additional thermal characteristics details.

## Sense Resistors

Refer to Figure 7.

Each port's front-end circuit has a single sense resistor. The resistor's value should be 500 mΩ (or 487 mΩ). The resistor dissipates about 0.26 W at 720 mA (802.3at maximum load) and 62 mW at 350 mA (802.3af maximum load).

To achieve maximum current accuracy, the resistors should be placed near the PD69012.

Heat generated from these resistors contributes to a higher ambient temperature near the PD69012.

For 802.3af ports use the sense resistors types listed in the following table:

| QTY for 12 Ports | Description | PCB Foot print | Manufac. | Manufact. Part Number |
|---|---|---|---|---|
| 12 | RES TCK FLM 0.500R 1% 125 mW 0805 SMT | PD-0805 | Venkel | LCR0805R 500FSNT |
| 12 | RES TCK FLM 0.487R 1% 125 mW 0805 SMT | PD-0805 | Koa | SR732ETT DR487F |

For 802.3at ports, use the following sense resistors types:

| QTY for 12 Ports | Description | PCB Footprint | Manufac. | Manufacturer's Part Number |
|---|---|---|---|---|
| 12 | RES TCK FLM 0.500R 1% 500 mW 1210 SMT | PD-1210 | Venkel * | LCR1210R500FSNT-MS |
| 12 | RES TCK FLM 0.487R 1% 500 mW 1210 SMT | PD-1210 | Venkel * | LCR1210R487FSNT-MS |

*Dedicated part number for Microsemi PoE application; preferential pricing for Microsemi customers.

**Note** The sense resistor's temperature coefficient of resistance (ppm) must be less than or equal to $\pm 200\ [10^{-6}/^{\circ}C]$.

## Power MOSFETs

Refer to Figure 7

Each port circuit has a single external Power MOSFET.

The design should ensure the maximum operating junction temperature of the MOSFETs (150°C or 175°C as specified in MOSFET's data sheet) is not exceeded under worst case conditions.

For more details related on how to examine and choose a MOSFET for a PoE application, refer to the *How to Choose MOSFET for 802.3at and 802.3af PoE applications TN, Catalogue Number 06-0022-081*.

Examples for approved MOSFETs are shown in the following tables.

**Table 1: 802.3af MOSFET Examples**

| # | PCB Footprint | Manufacturer | Manufacturer's Part Number |
|---|---|---|---|
| 1 | SOT-223 | Fairchild | IRLM110A |
| 2 | DPAK | Fairchild | FQD5N15 |
| 3 | SOT-223 | Infineon | BSP372 |

**Table 2: 802.3at MOSFET Examples**

| # | PCB Footprint | Manufacturer | Manufacturer's Part Number |
|---|---|---|---|
| 1 | DPAK | Fairchild | FQD19N10L |
| 2 | SOT-223 | Fairchild | FDT3612_SB82273 * |
| 3 | DPAK | ST | STD10NF10T4 |
| 4 | DPAK | IR | IRFR3910 |
| 5 | SOT-223 | Infineon | BSP373 |

*Dedicated part number for Microsemi PoE application; preferential pricing for Microsemi customers

## Ambient Temperature

The application's thermal design should take into account the temperature derived from the Switch's power dissipation and from the PoE daughter board powered at maximum load.

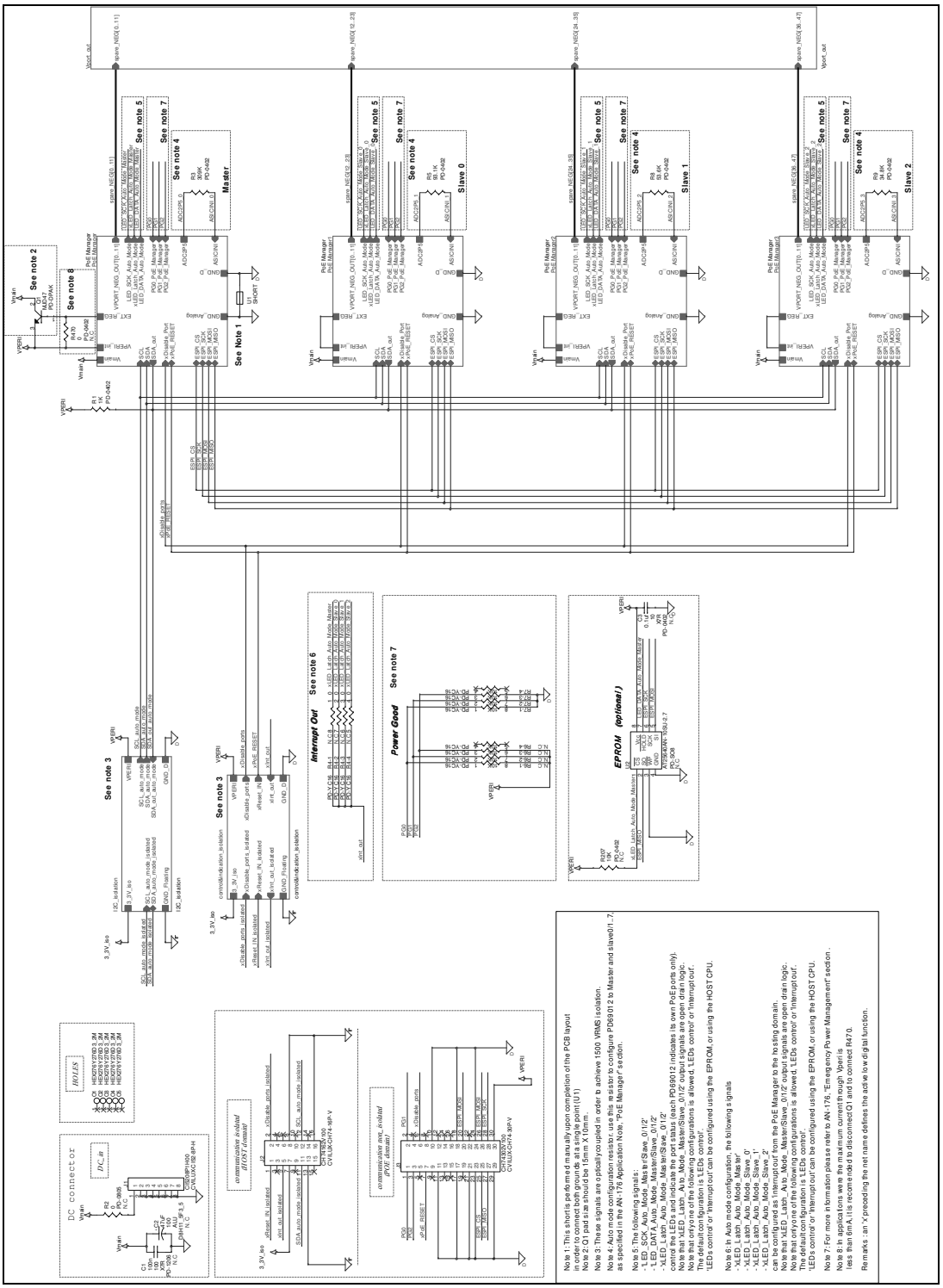


**Figure 6: Overall Block Diagram for 48-port Auto Mode System (I²C Interface)**

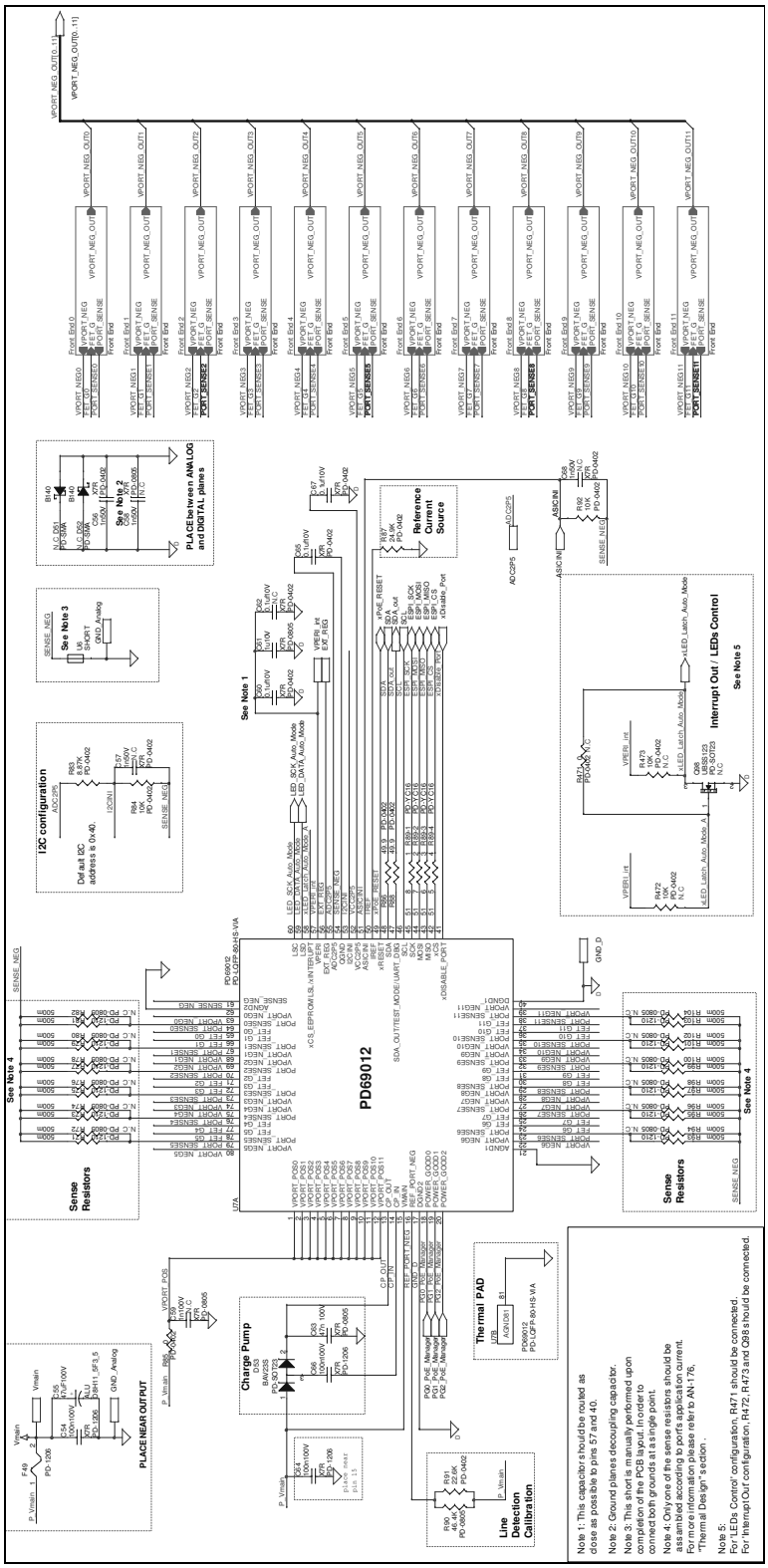


**Figure 7: PD69012 Circuitry for PoE Manager #0**

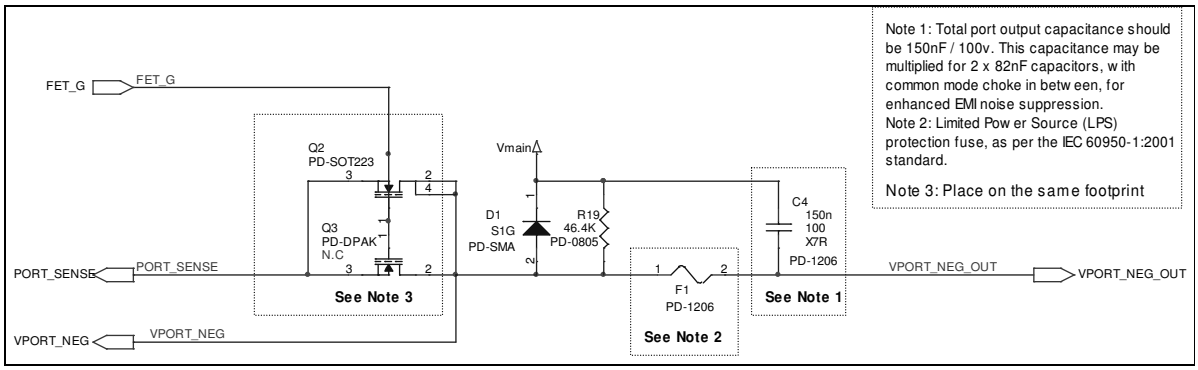


**Figure 8: Front-End Circuitry**

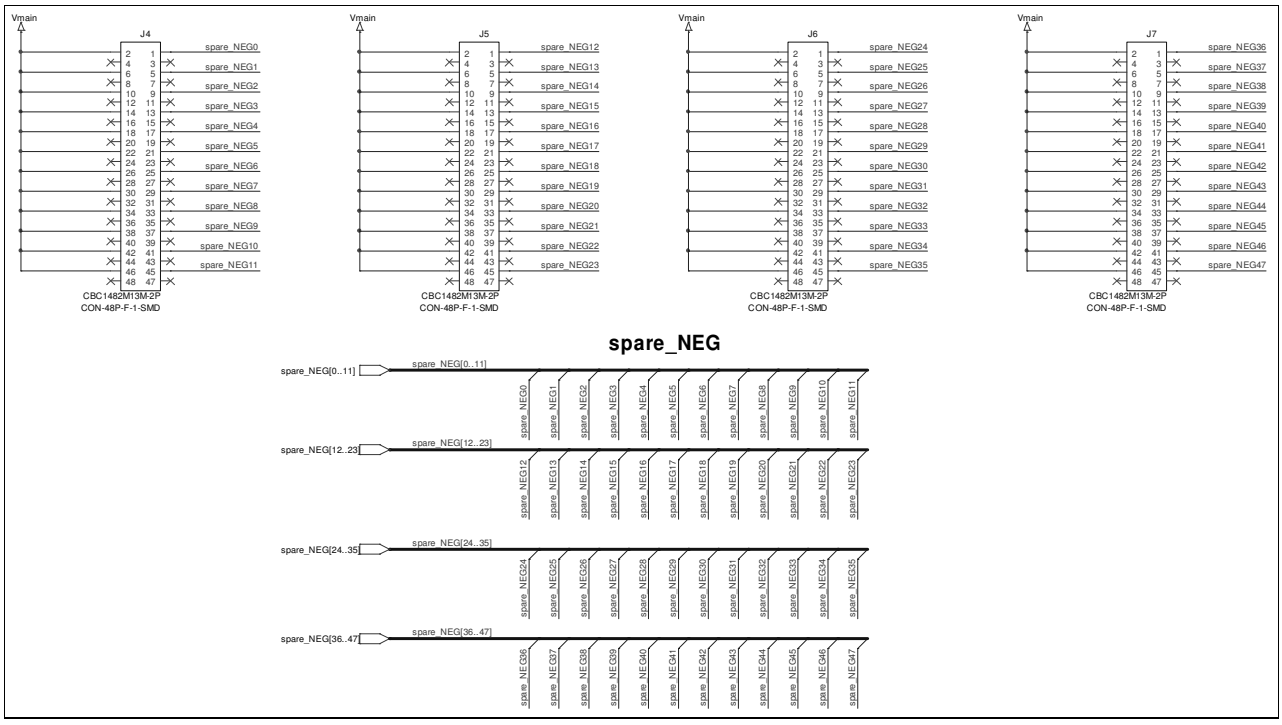


**Figure 9: Vport Out (Port's Interface)**

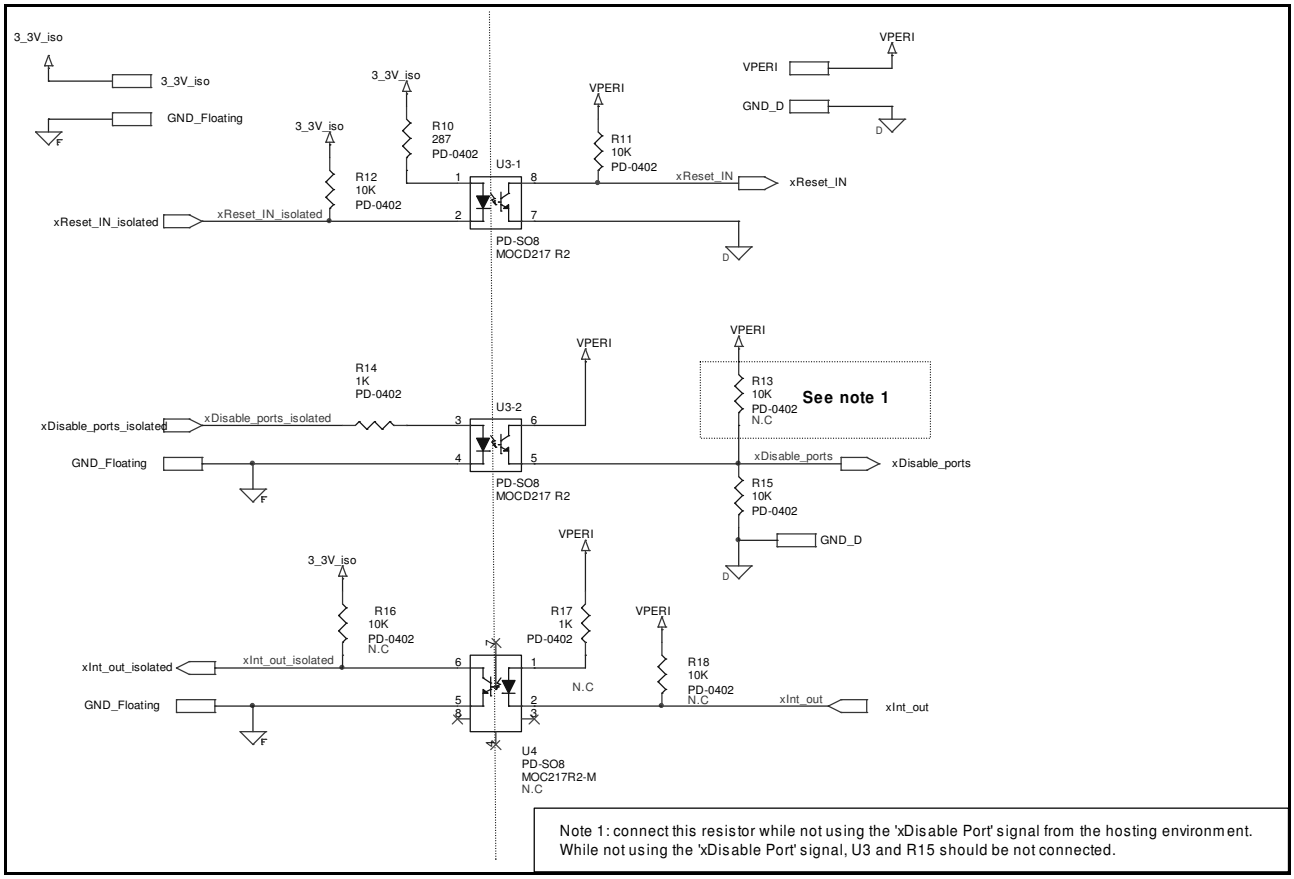


**Figure 10: Control and Indication Isolation Circuitry**

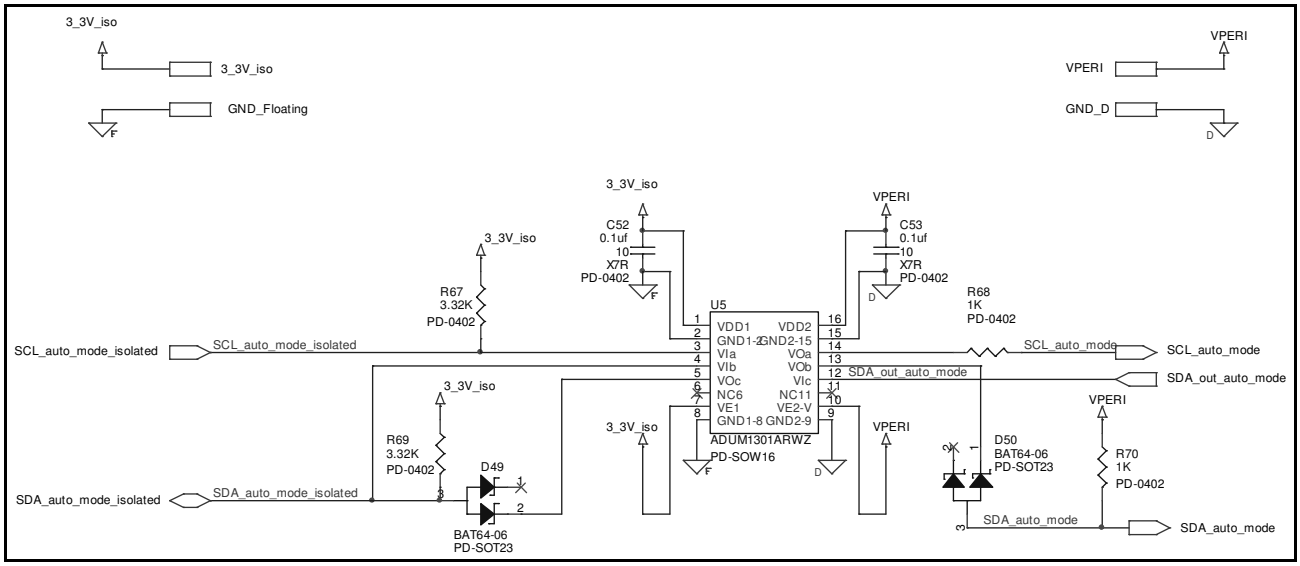


**Figure 11: I²C Isolation Circuitry**

# Bill of Materials for PoE System

**Table 3: Main Components**

| Block | QTY | Reference | Description | PCB Footprint | Manufacturer | Manufacturer's Part Number |
|---|---|---|---|---|---|---|
| Main | 1 | J1 | Pin Header male 1row 8pins Horizontal | CVILUX-CI52-8P-H | CviLux | CI5208P1H00 |
| | 1 | J2 | Pin Header Dual Raw Board mount 16 Pin p 2 mm TH | CVILUX-CH74-16P-V | CviLux | CH74162V100 |
| | 1 | J3 | Pin Header Dual Raw Board mount 30 Pin p 2 mm TH | CVILUX-CH74-30P-V | CviLux | CH74302V100 |
| | 1 | Q1 | TRN NPN 250V 1A 15W D-Pak SMT | PD-DPAK | Fairchild | MJD47 |
| | 1 | R1 | RES TCK FLM 1K 1% 62.5 mW 0402 SMT | PD-0402 | Bourns | CR0402-FX-1001-E |
| | 1 | R3 | Resistor, 309K, 1%, 1/16W 0402 | PD-0402 | ASJ | CR10-3093FK" |
| | 1 | R5 | RES SMT 93.1 Kohm 1% 1/16w 0402 | PD-0402 | Rohm | MCR01MZPF9312 |
| | 1 | R7 | RES 10K 62.5 mW 5% 1/4_1206 NET QUAD | PD-YC16 | Vishay | CRA06S08310K0JTA |
| | 1 | R8 | RES SMT 53.6 Kohm 1% 1/16w 0402 | PD-0402 | Yageo | RC0402FR-0753K6L |
| | 1 | R9 | Resistor, SMT 34.8K, 1%, 1/16W 0402 | PD-0402 | Rohm | MCR01MZPF3482 |

**Table 4: PoE Manager Slave Components**

| Block | QTY* | Reference | Description | PCB Footprint | Manufacturer | Manufacturer's Part Number |
|---|---|---|---|---|---|---|
| PoE Manager Slave | 3 | C54, C64, C66 | *CAP CRM 100 nF 100V 10% X7R 1206 SMT | PD-1206 | AVX | 12061C104KAT2A |
| | 1 | C55 | CAP ALU 47 uF 100V 20% 8X11.5 105C P=3.5mm T/H | D8H11_5F3_5 | Rubycon | 100PX47M T7 8X11.5 |
| | 1 | C56 | CAP CER 1nF 50V X7R 10% 0402 SMT | PD-0402 | Murata | GRM36R71H102KA01L |
| | 3 | C60, C65, C67 | CAP CER 0.1 uF 10V X7R 10% 0402 SMT | PD-0402 | Murata | GRM155R71C104KA88D |
| | 1 | C61 | *CAP CRM 1 uF 10V 10% X7R 0805 SMT | PD-0805 | Phycomp | 2222-240-15663 |
| | 1 | C63 | CAP CRM 47 nF 100V 10% X7R 0805 SMT | PD-0805 | Murata | GRM40X7R473K100 |
| | 1 | D53 | DIO DUAL 250V 225mA SMT SOT23 tr = 50nS SERIAL PH | PD-SOT23 | Philips | BAV23S |
| | 12 | R71, R73, R75, R77, R79, R81, R93, R95, R97, R99, R101, R103 | Res 500 mOhm 1/2 W 200 ppm 1210 | PD-1210 | VENKEL | LCR1210R500FSNT-MS |
| | 1 | R83 | RES TCK FLM 8.87K 1% 62.5mW 0402 SMT | PD-0402 | Yageo | RC0402FR-078K87L |
| | 2 | R84, R92 | RES TCK FLM 10K 1% 62.5mW 0402 SMT | PD-0402 | Vishay | CRCW0402-10K0 1% ET1 E3 |
| | 1 | R85 | RES 0R 62.5mW 5% 0402 SMT MTL FLM | PD-0402 | Vishay | CRCW0402-0R0 5% ET1 E3 |
| | 2 | R86, R88 | RES TCK FLM 49.9R 1% 62.5mW 0402 SMT | PD-0402 | Bourns | CR0402-FX-49R9-ELF |
| | 1 | R87 | RES TCK FLM 24.9K 1% 62.5mW 0402 SMT | PD-0402 | Yageo | RC0402FR-0724K9 |
| | 1 | R89 | RES NET 4X51R 62.5mW 5% ISOL 1206 | PD-YC16 | B. I. Tec | BCN164AB510J7 |
| | 1 | R90 | RES TCK FLM 46.4K 125 mW 1% 0805 SMT | PD-0805 | EPCOS | B54102-A2463-F460 |
| | 1 | R91 | Res TCK FLM 22.6K 1% 62.5 m W 0402 | PD-0402 | Vishay | CRCW0402-22K6 1% ET1 E3 |
| | 1 | U7 | 12-port High PoE PSE Manager | PD-LQFP-80-HS-VIA | Microsemi | PD69012 |
| | 1 | F49 | Fuse 1.5A 63V V. FST BLO 1206 SMT | PD-1206 | Bussmann | TR1/CC12PD-1.5A -R** |

* These quantities should be multiplied by the number of PD69012 (four managers in this paper)
**Special part number for Microsemi PoE application; preferential pricing for Microsemi customers.

**Table 5: Front End Components**

| Block | QTY* | Reference | Description | PCB Footprint | Manufacturer | Manufacturer's Part Number |
|---|---|---|---|---|---|---|
| Front End | 1 | C4 | Cap CRM 150 nF 100V 10%^^X7R 1206 SMT | PD-1206 | Syfer | 1206J1000154KXT |
| | 1 | D1 | DIO RECOV. REC 400V 1A SMA SILICON SMT | PD-SMA | Diodes Inc. | S1G |
| | 1 | F1 | Fuse 1.5A 63V V. FST BLO 1206 SMT | PD-1206 | Bussmann | TR1/CC12PD-1.5A –R** |
| | 1 | Q2 | Transistor Fet N-Chanel 100V | PD-SOT223 | Fairchild | Refer to "power MOSFETs" in the thermal design section ** |
| | 1 | R19 | RES TCK FLM 46.4K 125 mW 1% 0805 SMT | PD-0805 | EPCOS | B54102-A2463-F460 |

* These quantities should be multiplied by the number of output ports (48 ports in this paper)
**Special part number for Microsemi PoE application; preferential pricing for Microsemi customers.

**Table 6: Vport Out Components**

| Block | QTY* | Reference | Description | PCB Footprint | Manufacturer | Manufacturer's Part Number |
|---|---|---|---|---|---|---|
| Vport_out | 1 | J4 | Pin Header Female 2 rows 48 Pins P1.27x1.27 SMT | CON-48P-F-1-SMD | CviLux | CBC1482M13M-2P |

* These quantities should be multiplied by the number of PD69012 (four managers in this paper)

**Table 7: Control and Indication Isolation Components**

| Block | QTY | Reference | Description | PCB Footprint | Manufacturer | Manufacturer's Part Number |
|---|---|---|---|---|---|---|
| Control & Indication Isolation | 1 | R10 | Resistor, 287 Ohm, 1%, 1/16W 0402 | PD-0402 | ASJ | CR10-2870FK |
| | 3 | R11, R12, R15 | RES TCK FLM 10K 1% 62.5 mW 0402 SMT | PD-0402 | Vishay | CRCW0402-10K0 1% ET1 E3 |
| | 1 | R14 | RES TCK FLM 1K 1% 62.5 mW 0402 SMT | PD-0402 | Bourns | CR0402-FX-1001-E |
| | 1 | U3 | IC OPTOISOLATOR MOCD217 DUALCHANNEL SMT | PD-SO8 | Fairchild | MOCD217 R2 |

**Table 8: Bill of Material for I²C communication circuit (Host side 3_3V_iso = 3.3V)**

| Block | QTY | Reference | Description | PCB Footprint | Manufacturer | Manufacturer's Part Number |
|---|---|---|---|---|---|---|
| I²C isolation | 2 | C52, C53 | CAP CER 0.1uF 10V X7R 10% 0402 SMT | PD-0402 | Murata | GRM155R71C104KA88D |
| | 2 | D49, D50 | DIO SCHOTTKY 30V 200 mA COM. ANODE SOT23 DOUBLE | PD-SOT23 | Infineon | BAT64-06 |
| | 2 | R67, R69 | RES TCK FLM 3.32K 1% 62.5 mW 0402 SMT | PD-0402 | Bourns | CR0402-FX-3321-ELF |
| | 2 | R68, R70 | RES TCK FLM 1K 1% 62.5 mW 0402 SMT | PD-0402 | Bourns | CR0402-FX-1001-E |
| | 1 | U5 | IC Triple channel Digital Ins. SOIC16W | PD-SOW16 | Analog Devices | ADUM1301ARWZ |

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Revision History

| Revision Level / Date | Para. Affected | Description |
|---|---|---|
| 0.1 / 08 December. 08 | - | Initial Release – Preliminary version |
| 0.2 / 22 January. 09 | | 1. draft 3.0 modified to draft 3.3<br>2. xDisable_ports signal isolation has been changed from "Normaly Enable" to "Normaly Disable".<br>3. Sense resistors had been changed to support 500mohm or 487mohm. |
| 0.3 / 7 May. 09 | "Front End" and Bill of Material | 1. C4 capacitor value changed from 47nF to 150nF. |
| 0.4 / 11 Nov. 09 | Figure 8<br>Page 5 | Adding a protection fuse<br>Protection fuse for abnormal operating voltage |



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