Introduction

This document describes the PD690xx's Power - Management mechanism, when working in the Auto - Mode. Power-management is required for a system having a limited power budget, where the total power consumption may exceed the capability of the PSE power-supplies. In cases where PoE ports' power consumption exceeds the power-supply's capability, the power-supply may be overloaded and collapse.
The power-management is intended to prevent such scenarios. PD690xx Power management mechanism has several modes of operations as detailed below.

Terminology & Definitions

This section describes the terminology and definitions used in this document.

PSU Power Supply Unit

PM Power Management

AT Refers to IEEE802.3AT (up to 600mA per port)**.**

AF Refers to IEEE802.3AF (up to 400mA per port).

PG Power Good signal - a logical signal provided by the PSU and intended to indicate if the PSU is connected to the system, or if it functions properly.

P_{nm} The nominal capability of the PoE power supply which is typically the maximum allowed continuous power to be drawn from the power supply.

P_{all} Allocated power, refers to the amount of per port allocated power by the PD690xx.

P_{con} Consumed power - the actual consumption drawn from the port/ports.

PPL Port Power Limit - the maximum power a port is allowed to consume; this is a pre-defined (default power) value register. It can be set by the user or saved as a default value. This PPL register value is utilized by the PM mechanism **before** the Classification or Power Up phase.
After port power up, the actual Power Request and Power Budget of the PM mechanism is represented by the TPPL register described below.

TPPL Temporary Port Power Limit **-** the maximum power a port is allowed to consume. This value is set after port is started up and is valid during port power up (on-going).

This maximum power level value will come into effect for PM mechanism from the power up point to the power down point (while port is in powered and on-going phase). Although it is NOT recommended, this TPPL register value can be updated during on-going operation.

Port Priority Each port can be individually set to a specific priority by the user. The PD690xx supports three priority levels for each port:

Critical = Highest Priority Level
High = High Priority Level
Low = Lowest Priority Level

When several ports are set to the same priority in different PD690xx ICs, the priority is determined by the IC "ASIC_INI" I/O mode as follows:

- Master IC will be 1st
- Slave 1 IC will be 2nd
- Slave 2 IC will be 3rd
- -
- -
- Slave 7 IC will have the lowest priority, in cases where all ports are set to the same priority.

For example, when ports in both the Master and the Slave ICs are all set to "High", the system power budget will be first allocated to the Master IC and then to the Slave IC.

When several ports are set to the same priority in the same IC, priority is determined by the physical port number (Port0 = highest priority … Port 11 = lowest priority etc.).

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Functional Description

Typical PoE system is based on one master PD690xx IC and optionally one or more PD690xx slaves ICs.
System power allocation is done and controlled by the master, according to priority settings on IC level.

Each IC (Master and Slave) manages its own ports according to its local port priority and its power budget – allocated by the Master.
This power allocation is based on the following mechanism:

1. Each IC sends a Power Allocation Request to the Master IC per Priority Group (Critical, High or Low), according to port classification, or port pre-defined static power setting (see Power Management modes section/ page 3).
2. The Master IC collects all ICs power requests (including its own local ports). Then it generates a Power Allocation table based on the system power budget for each IC and per priority group.
3. This Power Allocation Table includes a Power Budget level per priority and it is communicated back to all ICs (through the SPI bus).
4. Based on these power allocation registers (3 x registers for 3 priorities), each Slave IC powers up its local Ports.
5. Each IC continuously monitors its local ports' power consumption and confirms that it is within the Power Allocation (per priority) limits.

Example:
A PoE System having 1 x Master IC and 2 x Slave ICs. It has total a power budget of 100watt (see Figure 1).

Master IC Power Request –

20 watt for Critical Priority ports
0 watt for High Priority ports
15 watt for Low Priority ports

Slave 1IC Power Request –

10 watt for Critical Priority ports
20 watt for High Priority ports
0 watt for Low Priority ports

Slave 2IC Power Request –

0 watt for Critical Priority ports
15 watt for High Priority ports
10 watt for Low Priority ports

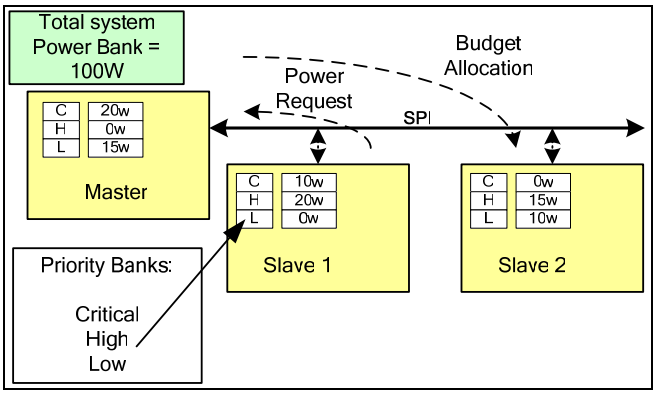

Figure 1: An Example for Power Allocation Process between Slaves and Master IC

Master IC – calculates the total power requests per priority level:

- 30 watt for all Critical Level ports
- 35 watt for all High Level ports
- 25 watt for all Low Level ports

The Master IC builds up a power allocation table as illustrated in Figure 2:

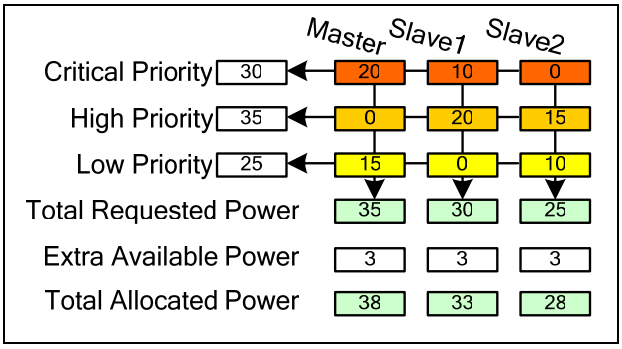

Figure 2: An Example of Power Allocation Table

Total requested power is 90 watt. Since the total power budget is 100watt, there is an additional 10 watt still available to be allocated back to the ports.

This extra power is equally divided between all ICs, as illustrated in Figure 2 (10/3 = ~3 watt).

From this point, each IC can power up its local PoE ports, while continuously monitoring its local power.

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PM Operational Phases _____

There are three operational phases during power management as follow:

1. Port start-up
2. On-going operation
3. Power disconnection due to over-power

Port-Startup:

Each device (IC) continuously monitors and detects the power requested for each PD after the detection and classification phases.
When a new PD sends a request for power up (start up), a new cycle of “Power Request” is sent to the Master IC, with a new port power requested value.
If System power budget is greater than the total requested power (there is extra power to allocate) - the Master allocates power to this specific slave IC and allows it to power up the PD.
Typically, during on-going system operation, only one port can be started up per power management cycle per IC.

In cases where additional PD is connected to the slave, it is powered in the next startup cycle.
The critical priority ports are turned-on first, followed by the high priority ports and then the low priority ports are turned-on.
In cases where a port is NOT started up due to limited power (the Master does not allocate power to a certain IC), this specific port status will be switched to "port off due to PM" (see Port Status Register in the PD690xx Register Map User Guide, Cat. No. 06-0061-056).
The Master will not allocate power to a new PD, when the available system budget is less than the total power requested by the PDs.

Note!
The Master allocates power to each PD according to PD's class and according to the slave's operational mode (AF or AT mode).
The following table defines the power consumption per class:

	AT Mode	AF Mode
Class 0	30W	16W
Class 1	4W	4W
Class 2	7W	7W
Class 3	16W	16W
Class 4	30W	NA

Note: Typical port startup cycle period is 670mSec.

On-going Operation:

After the port successfully passes the startup phase, its maximum power consumption level is limited to the maximum threshold value, as set in the Port Power Limit “TPPL” register.

During on-going port operation, the port power consumption threshold may be modified by changing the TPPL register's value.
The TPPL Register's content can be changed via the Host MCU (see Register 134C to 1362 in this document).

If the TPPL value is reduced by a communication command, this extra power will be allocated BACK to the Master IC in the next PM allocation cycle.

If the TPPL value is increased by a communication command, this extra power request will be transmitted to the Master IC in the next PM allocation cycle.
In cases where there is NOT sufficient power to be allocated by the Master, this request will be avoided and ignored.

Power Disconnection:

A port might be turned Off (powered down or disconnected) due to overload or due to PD disconnection.
On top of that - power may be turned-off due to power-management considerations (e.g. when total power consumption exceeds the available budget as represented by the TPPL register).

For Example – a port may be powered down in cases where system power budget register's value in the Master IC is reduced due to power source failure (see Emergency Power Management Appendix).

This may also happen due to reduced budget register communicated by the Host.

In this case – when total power budget is reduced, the Master IC will update and reduce the power allocation table for all ICs (affecting Low priority ports first).

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Power Management modes

There are two operational modes for the PM mechanism:

1. Dynamic mode
2. Static mode

Note: PM operational mode also depends on AF and AT configurations (refer to "Terminology & Definitions" section on page 1)

Dynamic Mode – The power requested and allocated to the port is based on the actual port's (real time) power consumption (assuming that port is not overloaded).

TPPL=Pcon

Static Mode - The power requested and allocated to the port is defined by the user before startup, or based on the detected class (assuming that port is not overloaded).

AF: TPPL=PPL or Class (the lowest value)
AT: TPPL=PPL

Note: PM mechanism cycle, based on Master IC communication, to sample and allocate power to all seven slaves – is completed every 1Sec.

Note: In cases where a pre-standard PD is connected to the port, its port power level will be set according to class 0.

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Power Management Registers

R/W = Read / Write Register
R = Read Only Register

Register/Flag Name	Description	Bit Number	Address (Hex)	Width (bits)	Read/ Write	Default Value
SysFlags/ IcutMaxFlag	Sets Icut Max Mode: 0 - sets Icut according to TPPL (Icut=TPPL/Vmain) 1 - sets Icut to max value, regardless of TPPL (AF=375mA, AT=644mA)	4	1160	16	R/W	1
SysFlags/ PM_Mode	Static / Dynamic power allocation mode (calculation mode of power management). 0 - Static (according to class or PPL) 1 - Dynamic (according to real consumption)	6	1160	16	R/W	1
SysFlags/ Class0EqAF	When class 0 is detected, then port power allocation is set to PPL or AF threshold: 0 - class 0 is detected as PPL 1 - class 0 is detected as AF (15.4W)	10	1160	16	R/W	0
SysFlags/ Class123EqAF	When class 1/2/3 is detected then port power allocation is set to PPL or AF class table: 0 - class 1/2/3 is detected as PPL 1 - class 1/2/3 is detected as AF (4/7/15.4W)	11	1160	16	R/W	0
StartupCR/ StartupHiPrOverride	If startup power is insufficient for the current port, check if the next ports can be started up. 0 - Next ports shall not be powered and port is marked as "port off due to PM". 1 - Check if startup power is sufficient for lower priority ports.	6	1190	16	R/W	0
Port_PM_ Indication	Bit per port indication of power management. ("port off due to PM".) This register is of the Clear on Read type. 0 - port not marked for PM 1 - port Off due to PM	0-15	129C	16	R	0

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Register/Flag Name	Description	Bit Number	Address (Hex)	Width (bits)	Read/ Write	Default Value
IcutMaxAt	Max Icut value for AT ports Resolution 4.88mA.	0-7	12A8	16	R/W	0x84 (644mA)
LocalTotalRealPowerCons	Slave - Real Time total power consumption Resolution 0.1Watt	0-15	12AA	16	R	0
LocalTotalCalcPowerCons	Slave - Calculated total power consumption (class). Resolution 0.1Watt	0-15	12AC	16	R	0
LocalCriticalPriPowerCons	Slave - Calculated power consumption of critical priority ports. Resolution 0.1Watt	0-15	12AE	16	R	0
LocalHighPriPowerCons	Slave - Calculated power consumption of high priority ports. Resolution 0.1Watt	0-15	12B0	16	R	0
LocalLowPriPowerCons	Slave - Calculated power consumption of low priority ports. Resolution 0.1Watt	0-15	12B2	16	R	0
Port[0-11] PowerCons	Port [0 to 11] – Real port power consumption. Resolution 0.1Watt	0-15	12B4 12B6 12B8 12BA 12BC 12BE 12C0 12C2 12C4 12C6 12C8 12CA	16	R	0
SysTotalCriticalCons	Calculated system power consumption of critical priority ports. Resolution 0.1Watt	0-15	12D6	16	R	0
SysTotalHighCons	Calculated system power consumption of high priority ports. Resolution - 0.1Watt	0-15	12D8	16	R	0
SysTotalLowCons	Calculated system power consumption of low priority ports. Resolution - 0.1Watt	0-15	12DA	16	R	0
SysTotalCalcPowerCons	Sum of the calculated power consumption by the whole system. Resolution - 0.1Watt	0-15	12E2	16	R	0
SysTotalRealPowerCons	Sum of the real power consumed by the whole system. Resolution - 0.1Watt	0-15	12E8	16	R	0

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Register/Flag Name	Description	Bit Number	Address (Hex)	Width (bits)	Read/ Write	Default Value
ActiveSlaveList / CurrentActive Slaves	Current active slaves. Bit per slave from 1 – 7.	0-7	12EA	16	R	0
ActiveSlaveList / InitialActive Slaves	Detected active slaves at system initialization. Bit per slave from 1 – 7.	8-15	12EA	16	R	0
Port[0 to 11] _Cnfg/ PortMode	Port [0 to 11] type definition. 00 - AF 01 - AT	4-5	131A 131C 131E 1320 1322 1324 1326 1328 132A 132C 132E 1330	16	W	01
Port[0 to 11] _Cnfg/ PortPriority	Port [0 to 11] priority level 00 - Critical 01 - High 10 – Low 11- Reserved	6-7	131A 131C 131E 1320 1322 1324 1326 1328 132A 132C 132E 1330	16	W	00
TotalPowerConsSlave[0-7]	Total real power consumption of slaves [0 to 7] Resolution - 0.1Watt	0-15	12EC 12EE 12F0 12F2 12F4 12F6 12F8 12FA	16	R	0
Port[0-11]_PPL	Port [0 to 11] power allocation limit. Resolution - 0.1Watt	0-15	1334 1336 1338 133A 133C 133E 1340 1342 1344 1346 1348 134A	16	R/W	0x140 (32Watt)

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Register/Flag Name	Description	Bit Number	Address (Hex)	Width (bits)	Read/ Write	Default Value
Port[0-11]_TPPL	Temporary port [0 to 11] power allocation limit. Resolution - 0.1Watt	0-15	134C 134E 1350 1352 1354 1356 1358 135A 135C 135E 1360 1362	16	R/W	0
SysPower Budget[0-7]	Pre defined system power budget allocation for the Master IC, for all eight states according to Power Good Pins (PG) [000 to 111] Power budget resolution – LSB = 0.1Watt	0-15	138C 138E 1390 1392 1394 1396 1398 139A	16	R/W	3456w 432w 300w 220w 200w 150w 120w 100w
PowerBudget[0-7]	Power budget allocation from the Master to Slave IC - for state [000 to 111] of the Power Good lines. Resolution - 0.1Watt	0-15	136A 136C 136E 1370 1372 1374 1376 1378	16	R	0x1158 (444W)

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Emergency Power Management Appendix (Power Banks)_____

PoE system can be powered by up to three separate power supplies (see Figure 1).

It is recommended that each power supply will be able to generate a logic signal, indicating its' operate/fail status.
Two logical features can be provided from the PSU:

1. xPower Good signal (default) -

PG = '0' logical – indicating operational power supply
PG = '1' logical – indicating failed power supply
(in this mode, R7 should not be connected and R6 should be connected).

2. Power Good signal -

PG = '1' logical – indicating operational power supply
PG = '0' logical – indicating failed power supply
(in this mode, R6 should not be connected and R7 should be connected).

The Master allocates power to the system in accordance with the overall available power. This total system power budget depends on the Power Good input signals, coming from the power supplies, as demonstrated in the table below.

With three power supplies having up to three different output levels, up to eight power banks can be derived from their combinations. The utilized pins are specified below:

Pin Number	Signal	Remarks
#18	PG0_PoE_manager	Power Good 0
#19	PG1_PoE_manager	Power Good 1
#20	PG2_PoE_manager	Power Good 2

Note: If the PG pin is not used, it must be connected to, either GND or 3.3v (Vperi).

Figure 1 describes the connections between the power supplies' logic signals and the PoE managers.

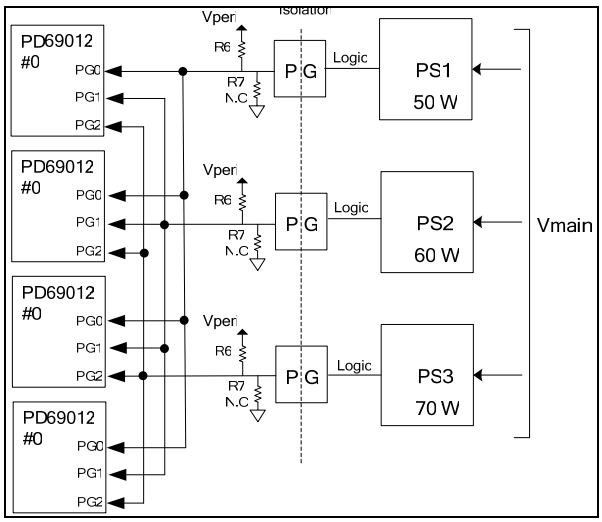

Figure 1: Power Good

For isolation requirements destined for Emergency Power Management, refer to Technical Note-134, Cat. No. 06-0014-081, "Isolation Requirements" Section.

Power Banks Setting:
Power banks should be predefined according to the actual PS which will be connected to the system.
There are eight available power banks; a bank is selected by the system according to the state of the three PG pins.
The following example is based on Figure 1:

Pnm1 =50watt
Pnm2 =60watt
Pnm3 =70watt
PG = '0' logical – indicating operational power supply
PG = '1' logical – indicating failed power supply

Bower banks should be set as follows:

Power Bank	PG3 , PG2 , PG1
PB0 is set 50+60+70= 180W	0 , 0 , 0
PB1 is set 60+70= 130W	0 , 0 , 1
PB2 is set 50+70= 120W	0 , 1 , 0
PB3 is set 50W	0 , 1 , 1
PB4 is set 50+60= 110W	1 , 0 , 0
PB5 is set 60W	1 , 0 , 1
PB6 is set 70W	1 , 1 , 0
PB7 is set 0W	1 , 1 , 1

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Revision History

Revision Level / Date	Para. Affected	Description
1.0 / 11 January 2009	-	Initial Release

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