Stellamar Introduces All Digital, Fully Synthesizable Analog-to-Digital Converters

for Microsemi FPGAs

June 2011

Introduction

Programmable digital devices, led by FPGAs, have exploded in popularity as costs have come down and performance has increased. Additionally, shrinking product life cycles are making higher volumes more difficult and driving an increase in FPGA usage over ASICs. This also leads to an increase in FPGA usage in high-reliability and system-critical applications. A recent article in the EE Times, *Programmable ICs: The Next Innovation Engine*, identifies and describes the most fundamental challenges to continuing the growth path of FPGAs. Challenge #1 in this article is mixed signal circuit integration. Specifically, the article mentions that ADCs, DACs and power circuits will need to be integrated to drive the next wave of FPGA evolution.

The next wave of the FPGA evolution is further complicated because as our end products become more complex, analog design efficiency becomes more important to the overall system. Additionally, the more sensory our end products become, the more ADCs are needed. As these end products become more portable, the efficiency of those ADCs becomes more important. Designers have often wondered if the underlying analog ADC design could ever be as efficient as digital design. Now it can be.

Originally, Stellamar set out to replicate in the ADC world what the sigma-delta DAC did for the DAC world. Most traditional DACs gave way to the sigma-delta version because of its mostly digital nature and ease of integration. This has been a much larger challenge on the ADC side. If the same could be done for ADCs, the industry would have a robust solution for the integration of ADCs into FPGAs. It was this challenge, precisely, that sparked innovation to create the most flexible, cost effective way to implement analog functions in digital fabric.

An A2D without the A

At Stellamar, the all digital ADC requires no analog block design. Only a few passive components are necessary. Specialized proprietary signal processing enables analog sigma-delta ADC performance to be replicated with all digital library cells. This proprietary technology allows digital ADCs to reap all the benefits that digital design has over analog design:

- 50% lower power on average
- 68% smaller area on average
- Process technology independence
- Reduced risk and cycle time
- Digital integration and synthesis
- Easier radiation-hardened design

These simple block diagrams (Figure 1 and Figure 2 on page 3) represent some differences.

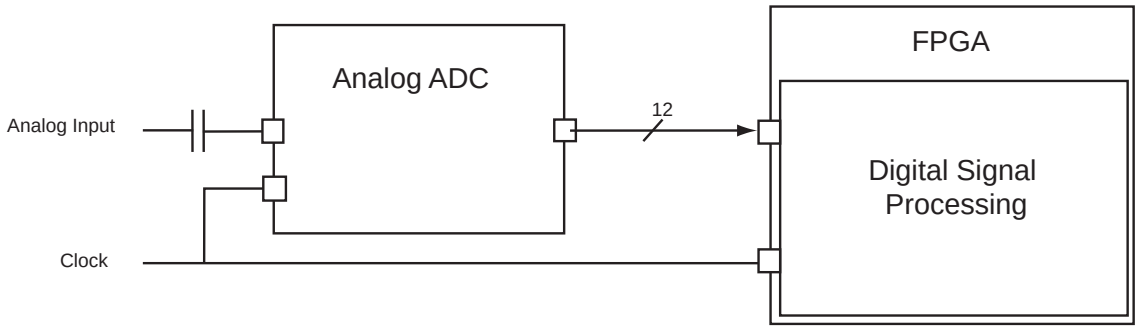

Figure 1: **Traditional ADC Interface**

In the traditional analog ADC approach, the designer must select an external ADC part to use an ADC with FPGAs. The good news is that creating the ADC is usually a vendor's responsibility. This specialization of labor can achieve very high tolerances and performance. The bad news is that these ADCs are usually external and large. Multiple pins are needed to connect to an FPGA. By not controlling the ADC development, designers trade off optimization for reduced design cycles. The vendor's solution is most likely an overdesigned part for the system. This may be fine for some ordinary applications that are not size/power constrained, but this tradeoff is suboptimal when designing for aerospace and other high-reliability applications

With the Stellamar All Digital approach, a designer does not have to use external ADCs, which can take up critical board space. The ADC is right on the digital fabric, and is much easier to implement through digital synthesis. The digital ADC only uses two pins and a couple discrete components, depicted in Figure 2. Now you have an ADC embedded in the digital fabric of your FPGA, which is properly optimized for your application, and you have also reduced board space, complexity and testing time, while increasing mean time between failures (MTBF). This approach is much easier to implement and test, which can greatly enhance your ability to meet time-to-market.

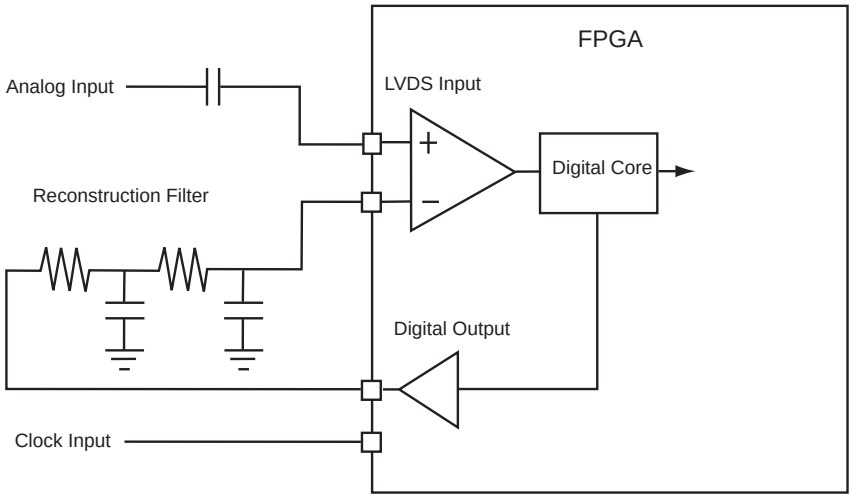

Figure 2: **Stellamar All Digital ADC Interface**

For additional ADC functionality in the conventional approach, either more ADC chips would be added, or an analog multiplexer would have to be added. With the All Digital ADC solution, a designer could just add more digital ADC IP blocks to take advantage of size and power savings.

Figure 3 and Figure 4 are typical frequency response plots for an ADC with a bandwidth of 20 kHz. The plots show an output with two different amplitudes of a 15 kHz input frequency. The first has an amplitude of 1.8 Vpp while the second is 60 dB lower, with an amplitude of 1.8 mVpp.

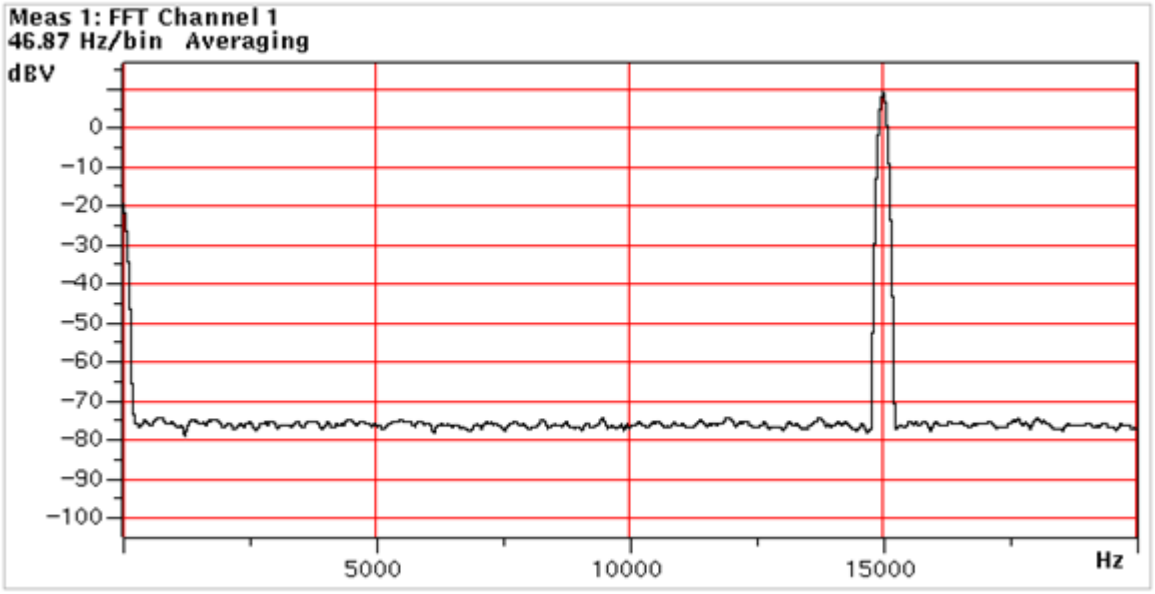

Figure 3: **Input frequency 15 kHz, Input Amplitude 1.8 Vpp**

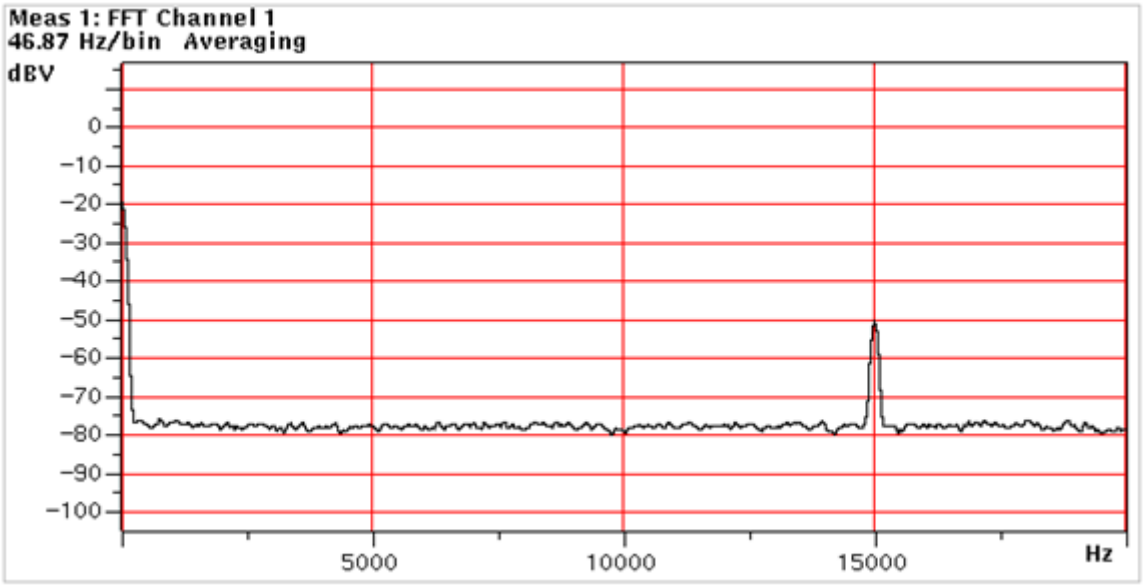

Figure 4: **Input frequency 15 kHz, Input Amplitude 1.8 mVpp**

Performance and Applications

A digital ADC is suitable for FPGA applications. Current performance of this All Digital Solution is up to 14 bits of resolution and 100 kHz bandwidth. Bandwidth depends on the selected resolution. Development efforts continue to support higher performance. Current performance is suitable for a host of applications including the following:

- Sensors—temperature, pressure, voltage, current, acceleration
- Touch screen integration
- Voice and high quality voice
- Wireless headsets
- Hearing aids
- Medical devices including ultrasound
- Motor control
- Radiation hardened aerospace needs

Example utilization for an 11-bit 4 kHz bandwidth digital ADC would be 2,624 tiles and 12 block RAMs.

Deliverables

Microsemi-based FPGA evaluation boards are currently in development. The intellectual property (IP) retargeted to Microsemi FPGAs is available for purchase, and shows 11 bits of resolution over a 20 kHz bandwidth for standard resolution, and 14 bits over 500 Hz for higher resolution applications. A purchased digital ADC block can be specifically optimized just about anywhere below those thresholds. Resolution and sample rates are driven by customer requirements. Stellamar will work with the customer to deliver a customized IP database that best suits those requirements. The IP database will also allow the customer to target desired technology. With the IP database, Stellamar provides a detailed implementation guide, and offers customer support through implementation.

FPGA Implementation Example

FPGAs may be used in mission-critical applications, especially in industrial monitoring and aerospace where an ASIC is not an economical solution. For example, FPGAs are used extensively in commercial and military satellites. Since FPGAs and ADCs come in both commercial and radiation-hardened varieties, together they provide a much needed service that can be customized without the cost of producing an ASIC. The problem is that in both commercial and military applications, the ADCs are external to the digital fabric, taking up space and power and impacting reliability. These critical factors are all high on the priority list when a satellite is designed. In system health monitoring, measuring voltage, current, temperature, pressure, etc., may be forgone due to weight, space and cost considerations. With an all digital ADC from Stellamar, designers can now use the FPGA digital fabric, thus reducing board space, weight and power and increasing reliability while still providing the same functionality. Furthermore, additional monitoring would be enabled without increasing weight and power. The reduction of weight and power and increased reliability amounts to lowering not only the cost of the satellite itself but the insertion costs as well. With increased reliability, the mean time before failures (MTBF) will increase, resulting in longer satellite lifetime.

Radiation Hardening

Since the design of radiation-hardened ADCs is extremely difficult, expensive and lengthy (typically over two years), only few radiation-hardened ADCs are developed that target the applications requiring the highest conversion speed. The same ADCs are used as well for lower speed applications, such as voltage measurements and pressure/acceleration sensors on the system. This means that power is being wasted and system performance is not optimized. If you have a Microsemi radiation-tolerant ProASIC®3 device (for example) already on the board, why not use the remaining 2–3% of the gates to run an optimized radiation-hardened digital ADC, and leave the big boy powered off? You have not increased the number of parts, or board space, and now you're optimized for power, and have a configurable ADC to repurpose for other applications.

Conclusion

Designers requiring ADC integration in a Microsemi FPGA now have a simple, flexible and complete solution. With a Stellamar digital ADC, most of the common bottleneck issues caused by ADC integration are removed. The result is a Digital ADC that can be easily embedded in any FPGA, and can be reprogrammed for different performance requirements. This ADC will also be much smaller and less power hungry for low power portable applications and critical aerospace needs. In the near future, engineers will be better able to integrate and synthesize other components previously thought to only remain in the analog domain. The Digital ADC is the first step.

Visit www.stellamar.com or email info@stellamar.com for more information.

By Allan Chin and Luciano Zoso

Allan Chin has over 30 years of design experience with high performance digital and mixed signal systems. Allan has made significant and recognized accomplishments in the design and engineering of sophisticated electronic systems and assemblies. His broad expertise covers many areas of IC design, including system requirement definition, chip development, mixed signal simulation, verification, prototyping and lab testing. Allan started his career at Honeywell, where he worked on flight and main engine control systems for the space shuttle. Allan also co-developed the digital video encoder chip while at Motorola/Freescale. During his career, Allan has held various management positions leading design teams at Motorola/Freescale, Mentor Graphics and Honeywell. Allan has a B.S. in Electrical Engineering from Marquette University, Milwaukee, Wisconsin, and holds nine patents. Allan can be reached at allan.chin@stellamar.com.

Luciano Zoso is an accomplished engineer and inventor with over thirty years of experience in digital signal processing. He has successfully applied his expertise in the areas of voice band modems, sigma-delta converters, multi-standard digital video encoders and decoders, stereo encoders, and GPS receivers as well as sensors. His experience ranges from system-level design and simulation to full implementation. Luciano started his career as a researcher at CSELT, research center of the Italian phone company in Torino, Italy. There he developed advanced data communication systems and pioneered a design methodology for high order sigma-delta converters. After his work at CSELT, Luciano moved to the R&D department of Hayes Microcomputer Products in Atlanta. He then worked with Allan at Motorola/Freescale, where he was responsible for system design of VLSI chips for audio/video and communications applications. There Luciano co-developed the digital video encoder chip with Allan. Luciano is also responsible for the Echo Canceller currently used in landline and satellite communications, and he also created the GPS receiver currently used in cell phones. Luciano has a Dr. Ing. Degree in electronics engineering from Politecnico di Torino in Italy. He holds eleven patents in signal processing. Email Luciano at luciano.zoso@stellamar.com.

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