HALT Evaluation of SJ BIST Technology for Electronic Prognostics

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Abstract—This paper presents the design, test, and results of a highly accelerated life test (HALT) evaluation of a soft-core called Solder Joint Built-in Self-Test™ (SJ BIST™), a method for detecting faults caused by solder-joint fractures in monitored input/output (I/O) pins of field programmable gate array (FPGA) devices, especially those in ball grid array (BGA) type of packages. Modern electronics utilize large FPGAs packages attached to electronic boards by means of solder joints, such as solder balls, between the package and the board. Thermomechanical stresses – primarily heat and vibration – cause fatigue damage and eventual fracture failure of one or more balls, which causes intermittent operational faults leading to catastrophic failures in critical systems. Such intermittent faults are difficult to reproduce on a test bench and many field returns of electronic modules with intermittently failing solder balls are diagnosed with code “no trouble found/could not reproduce.” The SJ BIST soft-core offers a solution because it detects faults in monitored pins caused by fractured solder joints of programmed FPGAs on deployed electronic boards.

At the end of the three-month HALT, selected FPGAs were subjected to die- and pry and cross-section examination and comparison to the collected data. Analysis confirmed that SJ BIST did report the occurrence of faults on damaged pins, and SJ BIST did not report any false negatives. The HALT confirmed the efficacy, accuracy, and reliability of SJ BIST as both a prognostic and diagnostic tool for FPGAs in BGA type of packages.

Keywords—solder joint; solder balls; FPGA; BIST; field programmable gate array; HALT; BGA

I. INTRODUCTION

Under NAVAIR1 funding BAE Systems, Johnson City, NY designed and ran a highly accelerated life test (HALT) using Solder Joint Built-in Self-Test™ (SJ BIST™)2 from Ridgetop Group, Inc., Tucson, Arizona. The primary objectives of the jointly-defined HALT were to evaluate the efficacy, accuracy, and reliability of SJ BIST to detect faults caused by fractured solder joints of input/output (I/O) pins of ball-grid-array (BGA) devices such as field programmable gate arrays (FPGAs). The secondary objective was to confirm or deny the assertion that I/O pins nearest a corner of a BGA device were likely to fail sooner than other pin locations. The SJ BIST HALT successfully detected faults caused by the following: wiring errors in the board, loss of power to the board, damaged cables, and fractured solder joints. There were no false alarms. The overall evaluation is the HALT confirmed the efficacy, accuracy, and reliability of SJ BIST as both a prognostic and diagnostic tool for FPGAs in BGA type of packages. The Johnson City half of the team commented: “We believe in the SJ BIST approach and that it works.”

Modern electronics utilize large FPGAs in high-density, array-type of packages that are attached to electronic boards by means of solder joints, such as solder balls, between the package and the board. Thermomechanical stresses – primarily heat and vibration – cause fatigue damage and eventual failure of one or more balls (Fig. 1) leading to intermittent operational faults and eventual catastrophic failures. Such intermittent failures are difficult to reproduce on a test bench and many field returns of electronic modules are diagnosed with “no trouble found/could not reproduce” codes.

The SJ BIST soft-core offers a solution because it detects fracture faults in monitored pins of FPGAs on programmed, deployed electronic boards.

Figure 1. Damaged and undamaged solder balls.

II. DESIGN OF EXPERIMENT

The design of experiment included the system configuration and control, the test evaluation boards (TEBs), the physical mounts, and the HALT regime. In addition to hardware,
firmware and software was written to synchronize the HALT cycles and the collection of data produced by the SJ BIST firmware. The block diagram of the SJ BIST HALT system is shown in Fig. 2.

A. System Configuration

The HALT system configuration is comprised of six test evaluation boards (TEBs) mounted in a combined thermal-vibration test chamber. Each board is populated with four Xilinx® FGG900\(^3\) (lead-free) 900-pin FPGAs running an SJ BIST program, which is loaded from a programmable read-only memory (PROM) programmed via JTAG (Joint Test Action Group) interface standardized as IEEE 1149.1 Test Access Port and Boundary Scan. The SJ BIST program monitors pairs of I/O pins connected to capacitors. A BAE-written chamber program controls the cycling of the boards, the application of vibration steps during each thermal dwell, and the sending of a “Sample” command to a Ridgetop-written program. SJ BIST fault data from each FPGA on each board is logged at each HALT cycle to a laptop Personal Computer (PC) using an RS-232 interface and a serial port (Universal 1600-8) as a hub.

B. Board Layout – Programming Interface

Fig. 3 shows the layout of the programming interface of the TEBs. Firmware is loaded into a controller PROM-FPGA pair to (1) control the programming for each device under test (DUT) FPGA on a TEB and (2) to control the collection of data from the DUTs.

C. Board Layout – Data Interface

Fig. 4 shows the data interface between the DUTs and the controller FPGA. Data is serially output from the controller FPGA using the RS-232 interface.

D. Board Cabling and Mounting

Fig. 5 shows a single-board, pre-HALT cabling setup used to verify the board design and correct operation of SJ BIST in the FPGAs; Fig. 6 shows a mounting fixture (1 of 2) with three boards.

E. HALT Regime

Table I shows the specifications for the three-hour thermal cycles. The induced vibration was random: power spectral densities (PSDs) equal to 0.005 g\(^2\)/Hz. The frequency range was 20 Hz to 600 Hz. Then the induced vibration was linearly decreased (0.0005 g\(^2\)/Hz at a fixed frequency of 2.000 Hz). This vibration step started 20 minutes after the start of each dwell and lasted for 20 minutes.

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\(^3\) SPARTAN® XC3S4000™ FGG900EGQ080 D3124927A
F. SJ BIST Operation

For each selected group of 2 pins, SJ BIST writes a ‘10’ bit pattern through a first I/O port of a two-pin group to charge and discharge a capacitor attached to that group. The second I/O port of the group is used to read the ‘1’ bit immediately after it is written. When the resistance of the first I/O port becomes too large, the charge on the capacitor will be insufficient to be read as a ‘1’ bit (see Fig. 7). In the next clock cycle, the ‘10’ is written using the second I/O port and the first I/O port is used to read the ‘1’ bit.

G. HALT Pin Pairs (Groups)

The two-pin soft-core for SJ BIST was used to create a firmware program that monitored 32 groups of two pins: 64 pins total. The monitored groups are shown in Fig. 8, and the group and pin numbers are shown in Table II.

III. HALT RESULTS

A three-month HALT was run from 16 November 2009 and continued through 16 February 2010. Because of preliminary checks, the first actual HALT cycle was logged as number four.

A. Cycle 4 (28 October 2009): Verify Electrical

Five of the 24 FPGAs were found to be nonresponsive prior to starting the HALT: Board 2, FPGAs 0 and 1; board 5, FPGA 0; and board 6, FPGAs 0 and 1. Because of time and budget constraints, we elected to not fabricate replacement boards. The logged data for HALT cycle 4 (HC4) confirmed the null responses from those FPGAs.

In addition to reporting a null response from FPGA 0 and 1, the data log (see Fig. 9) for board 2 showed pin group 0 of FPGA 2 had a hard error on both pins. This same error occurred on FPGA 2 on all boards. The data log also indicated that both pins in group 23 of that FPGA were open: subsequent cycles indicated that group experienced intermittent faults. The “POWER ON” record indicates this is the first log after the board was powered on.
Fig. 9 is a graphical view of the HALT status: ⬜ = no response from the indicated FPGA, ⬜ = solid error(s) in the indicated pin group; ⬜ = intermittent faults in the indicated pin group, ⬜ = no data written, and ⬜ = over 100 intermittent faults in the indicated pin group. The eight outlined groups are those nearest a corner of a DUT.

Fig. 10 is a graphical view of the HALT status: ⬜ = no response from the indicated FPGA, ⬜ = solid error(s) in the indicated pin group; ⬜ = intermittent faults in the indicated pin group, ⬜ = no data written, and ⬜ = over 100 intermittent faults in the indicated pin group. The eight outlined groups are those nearest a corner of a DUT.

B. HALT Cycles 5 – 23 (20 November): Verify Logging

Continuous HALT cycling began 16 November and on 20 November the logged data for cycles 5 through 23 were sent to Tucson for analysis to verify the firmware and software to collect and log data were working correctly. Fig. 11 shows intermittent faults occurring in six additional pin groups.

C. HALT Cycles 24 – 72 (30 November): Over Current

On 25 November, it was noticed the 5A 5VDC power supply was going into current-limiting mode. We decided to reduce the oven temperature to 85°C (see Fig. 12) until we could replace the original with a larger power supply. When we examined the logged data records, and we determined the previous damage to boards 2 and 6 had increased as shown in Table III, Table IV, and Fig. 13:

D. HALT Cycles 73 – 257 (29 January 2010)

The HALT was suspended on 30 November until the 5VDC power supply was replaced 5 December. A power outage in Johnson City on 15 December shutdown the HALT power supplies, a condition that was not noticed until 21 December.
The logged data records ending 13 January were sent to Tucson for examination: nine new error and fault conditions were noted as shown in Table V and Fig 14. The team in Tucson asked the team in Johnson City to examine the cables: the RS-232 cables exhibited high-heat damage to include brittle and broken insulation, and interior material liquefied and oozing (see Fig. 15). The HALT was again suspended on 29 January pending replacement of the RS-232 cables. Board 0 was returned to Tucson for physical examination: there was no visible sign of damage.

**TABLE V. NEW ERRORS AND FAULTS: HALT CYCLE 204**

<table>
<thead>
<tr>
<th>HC 204</th>
<th>Logged Records</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Board 0, no response from the controller</td>
<td>missing all records</td>
</tr>
<tr>
<td>2 Board 1, FPGA 2 stopped responding</td>
<td>NULL FPGA RESPONSE: 2</td>
</tr>
<tr>
<td>3 Intermittent power off-on</td>
<td>010320050505050505</td>
</tr>
<tr>
<td></td>
<td>POWER ON: 0103210505050505</td>
</tr>
<tr>
<td>4 Board 2, FPGA 2 stopped responding</td>
<td>NULL FPGA RESPONSE: 2</td>
</tr>
<tr>
<td>5 Board 3, FPGA 0, bad dummy record</td>
<td>0300200000000000</td>
</tr>
<tr>
<td></td>
<td>instead of 0300020050505050</td>
</tr>
<tr>
<td>6 Board 3, FPGA 1 through 3, high fault counts</td>
<td>for example:</td>
</tr>
<tr>
<td></td>
<td>248 and 208 faults 0301000500000000</td>
</tr>
<tr>
<td></td>
<td>149 and 172 faults 0301010509050505</td>
</tr>
<tr>
<td></td>
<td>32 and 38 faults 0301020502000000</td>
</tr>
<tr>
<td>7 Board 5, FPGA 1, moderate counts: 25 and 39</td>
<td>0501000501090207</td>
</tr>
<tr>
<td></td>
<td>16 and 14 0501010501000000</td>
</tr>
<tr>
<td></td>
<td>2 and 4 0501020502000000</td>
</tr>
<tr>
<td>8 Board 5, FPGA 2 stopped responding</td>
<td>NULL FPGA RESPONSE: 2</td>
</tr>
<tr>
<td>9 Board 5, FPGA 3, fairly high counts: 160 and 4</td>
<td>0503000501000000</td>
</tr>
<tr>
<td></td>
<td>161 and 7 0503010501010007</td>
</tr>
<tr>
<td></td>
<td>14 and 3 0503020500000003</td>
</tr>
</tbody>
</table>

The log records for 29 January showed three additional error conditions: boards 2 and 5 stopped responding and FPGA 3 on board 3 showed high fault counts. Only boards 1 and 6 showed operational FPGAs (see Fig. 16): five operational FPGAs out of 24.

**Figure 13. HALT status at end of cycle 72 (30 November).**

**Figure 14. HALT status at end of cycle 204 (13 January 2010).**

**Figure 15. Heat damaged RS-232 cables.**

**E. HALT Cycles 287 – 324 (16 February)**

The HALT was resumed 9 February after the RS-232 cables were replaced (cycle 258) with logging resumed that day starting with cycle number 287. Examination of the logged records indicated that three boards were once again responding: board 2, FPGA 3 (no faults); board 3, FPGAs 1, 2 and 3 (no faults); and board 5, FPGAs 1, 2, and 3 (high fault counts on all three FPGAs). 12 operational FPGAs out of the 20 on the remaining five boards (board 0 had been returned for inspection).

We ended the HALT on 16 February (cycle 322): the logged records at the end of the HALT were identical to those at the restart on 9 February (cycle 287): no additional errors or faults occurred. Fig. 17 shows the status.

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4 Cable swapping did not change the high fault counts: board five is definitely damaged – might be the controller FPGA on that board.
After the HALT ended, we did a limited number of dye and pry and cross-section examinations.

A. Dye and Pry

For the dye and pry examination (37 images), we selected board 2, FPGA 0, which was reported as null response from the very start of the HALT. Fig. 18 shows the one of the corners (A30) and clearly shows a failed pin next to the four corner (ground) pins, and three of the four ground pins fractured. At all four corners, there was at least one ball next to the corner that was fractured.

Looking at the middle clock pin shown in Fig. 18, the appearance of the ball indicates it was not securely attached to the board land – there is a lack of solder damage from the pry. This might have caused a loss of the clock, which might explain the non-responsiveness of that FPGA.

B. Cross Sectioning

We cross sectioned 48 pins and examined 103 images. We concluded the following: pins that SJ BIST reported as having faults were fractured (no false alarms), an example of two pins C1 from group 31, board 6, FPGA 3 and G1 from group 30, board 6, FPGA 3 are shown in Fig. 19. Both balls are fractured, and referring to Fig. 17, SJ BIST detected high number of faults. With one possible exception (see Fig. 21), no fractures were found in pins SJ BIST reported as healthy. Fig. 20 shows two pins monitored by SJ BIST and for which no faults were reported: those pins were not fractured.

V. INTERMITTENT NATURE OF SOLDER-JOINT FAULTS

In addition to the possible contact point shown in Fig. 21, a fault might not occur for any number of other reasons: (1) The cross sectioning might have hidden a partial contact point (see
Fig. 22; (2) Vibration stresses might not have caused the fractured surfaces to open: conformal coating might dampen the effect of a vertical strain on device; and (3) The fault duration might be too short: the minimum fault duration is one-half of a clock cycle (20ns for this HALT). Guaranteed fault detection requires the fault to last at least 2 clock periods (80ns) and have an effective open resistance of 100Ω or more.

VI. SUMMARY, CONCLUSION, AND LESSONS LEARNED

A. Summary and Conclusion

Faults caused by the following were detected: wiring errors in the board, loss of power to the board, damaged cables, and fractured solder joints. There were no false alarms. Of the seven faulty 2-pin groups, five were as near as possible to an outer corner of an FPGA; one group was only four pin rows away; and the seventh was nearest a corner of the interior ground pins. The objectives of the HALT were more than met and SJ BIST is a proven effective tool for detecting write faults in programmed FPGAs on electronic boards.

B. Lessons Learned

Some of the lessons we learned about using SJ BIST for HALTS are the following:

- Reduce the write-read for each group from two clock periods to four clock periods. This reduces the I/O current requirement by one-half.
- Only monitor 8 pins interior pins instead of 32: two at each corner of the inner periphery and use the other 24 pins to monitor the outer periphery.
- Design and develop a real-time graphics display of the faults – similar to that shown in Fig. 18.
- Ensure all commercially-obtained cable harnesses are rated for 100°C.
- At 125°C, the required I/O current is much higher than at 100°C – perhaps double the rated maximum of the FPGA.

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