



**SmartFusion<sup>®</sup> SoC FPGAs**  
System-on-Chip



SmartFusion® System-on-Chip (SoC) devices integrate an FPGA, an Arm® Cortex®-M3 processor and programmable analog, offering full customization, IP protection and ease-of-use. Based on Microchip's proprietary Flash process, SmartFusion SoCs are ideal for hardware and embedded designers who need a true system-on-chip that gives more flexibility than traditional fixed-function Microcontrollers (MCU), without the excessive cost of soft processor cores on traditional FPGAs.

**Hard 32-bit  
Arm Cortex-M3 Processor**

**Proven ProASIC®3  
FPGA Fabric**

**Full-Featured  
Programmable Analog**



## Key Benefits of SmartFusion SoCs

### Full Design Customization

- Create a product with exactly the features you need
- Innovate and differentiate for a competitive edge
- Incorporate last-minute changes with an on-chip FPGA
- In-application Programming (IAP) capability for field upgrades
- Experiment with hardware acceleration for select algorithms in FPGA fabric

### Intellectual Property (IP) Protection

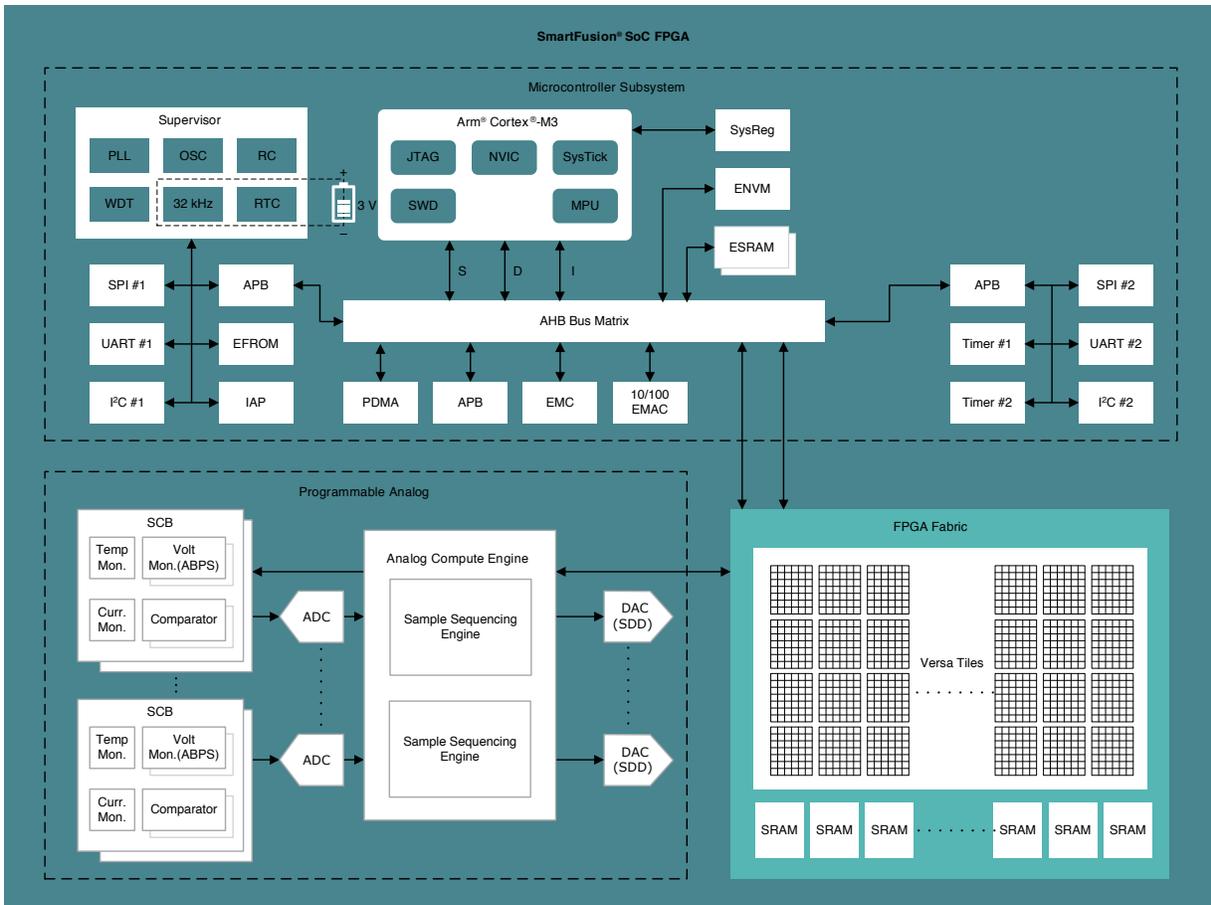
- Interface between microcontroller and FPGA not exposed at board level
- No bitstream exposed at power-up
- Encrypted In-System Programming (ISP) with 128-bit AES via JTAG
- FlashLock® controls access to the security setting on the device
- Protection against overbuilding with customer programmable device key

### Ease-of-Use Increases Productivity

- A single platform for your entire line of products
- Integrated design environment for both FPGA and embedded designers
- Simple GUI-based configuration of complex programmable analog
- Industry leading compile and debug from Keil, IAR and GNU
- Real-Time Operating System (RTOS) and middleware components from Micrium, RoweBots, Emcraft and more

# SmartFusion Architecture

SmartFusion SoC FPGA offers 2K and 6K LE families with hard 100 MHz 32-bit Arm Cortex-M3. SmartFusion SoC FPGAs are ideal for hardware and embedded designers who need a true SoC solution that gives more flexibility than traditional fixed-function MCUs without the excessive cost of soft processor cores on traditional FPGAs.



## No-Compromise

### Microcontroller Subsystem (MSS)

- Hardware industry-standard 100 MHz, 32-bit Arm Cortex-M3 CPU
- Multi-layer AHB communication matrix with up to 16 Gbps throughput
- 10/100 Ethernet MAC with RMII interface
- Two of each: SPI, I<sup>2</sup>C, UART, 32-bit timers
- Up to 512 KB Flash and 64 KB of SRAM
- External Memory Controller (EMC)
- 8-channel DMA controller
- Up to 41 MSS I/Os with Schmitt trigger inputs
- 25 I/Os can be used as FPGA I/Os

### Programmable Analog

- High-performance analog Signal Conditioning Blocks (SCB) with voltage, current and temperature monitors
- Analog Compute Engine (ACE) offloads CPU from analog initialization and processing of Analog-to-Digital Conversion (ADC), Digital-to-Analog Conversion (DAC) and SCBs
- Integrated ADCs and DACs with 1% accuracy
- 12-/10-/8-bit mode ADCs with 500/550/600 Ksps sampling rate
- Up to ten 15 ns high-speed comparators
- Up to 32 analog inputs and 3 outputs

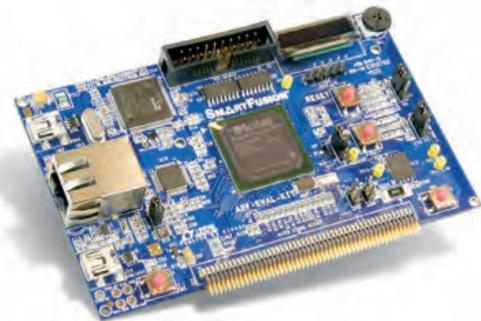
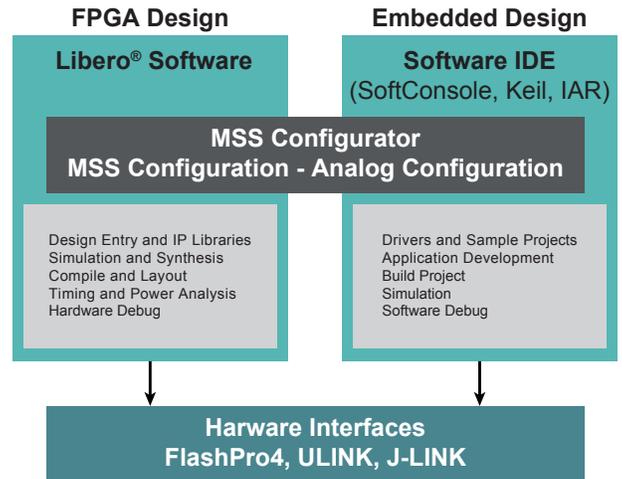
### No-Compromise FPGA Fabric

- Based on proven ProASIC3 architecture
- 200,000 to 500,000 system gates with 350 MHz system performance
- Embedded SRAMs and FIFOs
- Variable aspect ratio 4,608-bit SRAM blocks
- $\times 1$ ,  $\times 2$ ,  $\times 4$ ,  $\times 9$  and  $\times 18$  organizations
- True dual-port SRAM (including  $\times 18$ )
- Up to 128 FPGA I/Os supporting LVDS, PCI, PCI-X and LVTTTL/LVC-MOS standards

Designing with SmartFusion SoCs involves three different types of design: FPGA design, embedded design and analog design. These roles can be filled by three different designers, two designers or even a single designer, depending on company structure and project complexity. Microchip has developed design tools and flows to meet the needs of these three types of designers so they can work together smoothly on a single project.

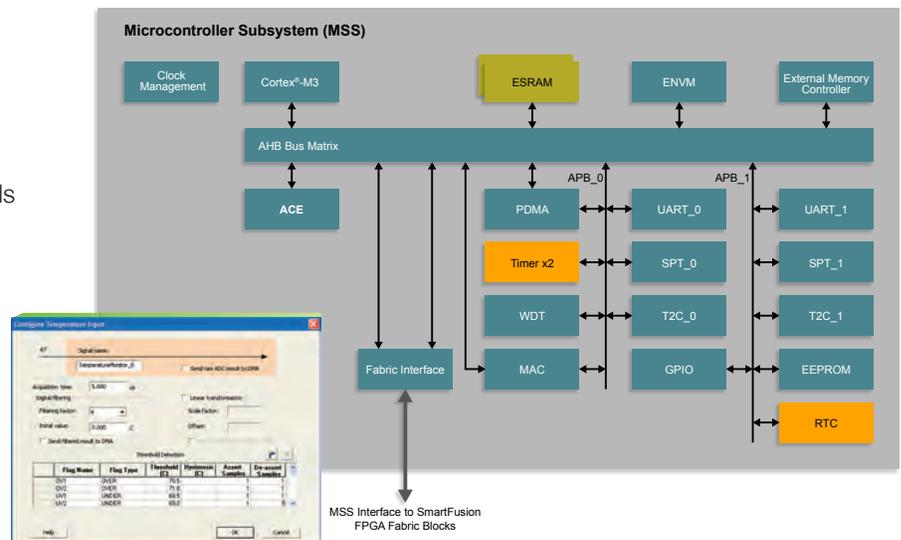
- **FPGA Design**—Libero® SoC Design Suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with low-power Flash FPGAs and SoC. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management and debug capabilities.
- **Embedded Design**—Microchip offers FREE SoftConsole Eclipse-based IDE, which includes the GNU C/C++ compiler and GDB debugger. Microchip also offers evaluation versions of software from Keil and IAR, with full versions available from respective suppliers.
- **Analog Design**—The MSS configurator provides graphical configuration for current, voltage and temperature monitors, sample sequencing setup and post-processing configuration, as well as DAC output.

The MSS configurator creates a bridge between the FPGA and embedded designers so device configuration can be easily shared between multiple developers.



## MSS Configuration

- Configure the MSS peripherals and I/Os during embedded system design.
- Create or view hardware configuration in FPGA design flow.
- Create or import hardware configuration in embedded design flow.
- Automatically generate drivers for peripherals or soft IP.
- Configure programmable analog components.
- Connect FPGA fabric designs and IP to MSS.

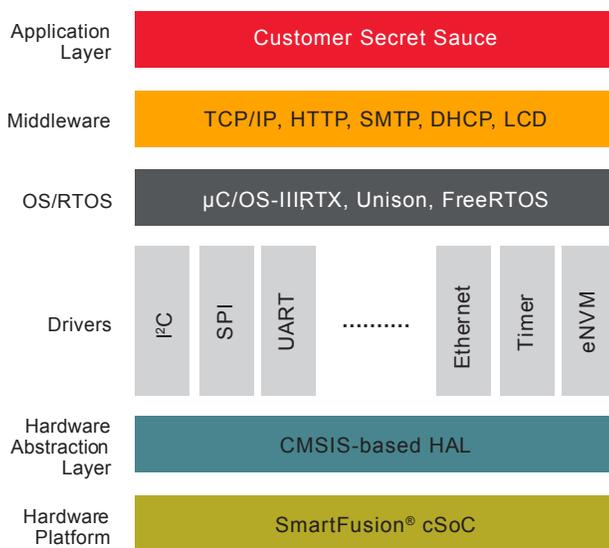


# SmartFusion Ecosystem

Microchip has a long history of supplying comprehensive FPGA development tools and recognizes the benefit of partnering with industry leaders to deliver optimum usability and productivity to customers. Taking the same approach with processor development, Microchip has partnered with key industry leaders in the microcontroller space to provide the robust SmartFusion ecosystem.

Microchip is partnering with Keil and IAR to provide software IDE support to SmartFusion system designers. The result is a robust solution that can be easily adopted by existing embedded developers. The learning path is straightforward for FPGA designers.

As an Arm processor was chosen for SmartFusion SoCs, you can benefit from the extensive Arm ecosystem. By building on supplied HAL and drivers, third party vendors can easily port RTOS and middleware for the SmartFusion devices.



The diagram above shows the SmartFusion stack with examples of drivers, RTOS and middleware from Microchip and partners. By leveraging the SmartFusion stack, designers can decide at which level to add their own customization to their design, thus speeding time to market and reducing overhead in the design.

Software IDE	SoftConsole	Keil MDK	IAR Embedded Workbench®
Free Versions from Microchip	Available from the Microchip website	32K Code Limited	32K Code Limited
Available from Vendor	N/A	Full version	Full Version
Compiler	GNU GCC	RealView® C/C++	IAR ARM Compiler
Debugger	GDB Debug	µVision Debugger	C-SPY® Debugger
Instruction Set Simulator	No	µVision Simulator	Yes
Debug Hardware	FlashPro4	ULINK®2 or ULINK-ME	J-LINK™ or J-LINK Lite
Trace Capability	No	ULINKpro	JTAGjet-Trace

## Operating System

### Micrium

Offers their µC/OS-III™ and µC/OS-II™ to support SmartFusion devices and includes a TCP/IP stack.

### Keil

Includes the RTX Kernel in their standard MDK software and sources can also be purchased in an additional module along with TCP/IP.

### RoweBots

Delivers their ultra tiny Linux® compatible RTOS Unison, consisting of a set of modular software components.

### Emcraft

Developed the first uCLinux® offering for SmartFusion, along with their own embedded development platform.

### FreeRTOS

Microchip has ported the FreeRTOS Kernel to SmartFusion and demonstrates this as a webserver reference design, included with both the SmartFusion evaluation and development kits.

## Industrial Automation

The range of peripherals offered for the Cortex-M3 processor and the flexibility of SmartFusion FPGA fabric make the device ideal for industrial automation. The SmartFusion Development Kit supports Ethernet, EtherCAT, CAN, UART, I<sup>2</sup>C and SPI hardware, while firmware can be used for various other interface standards such as Modbus<sup>®</sup> and PROFIBUS for industrial networking. With the availability of programmable analog for sensing and analog outputs, SmartFusion SoCs can also be used in industrial control applications, including gateways, sensing, actuators and I/O devices. The list below describes how the various sections of the device could be used in industrial automation.

### Microcontroller Subsystem

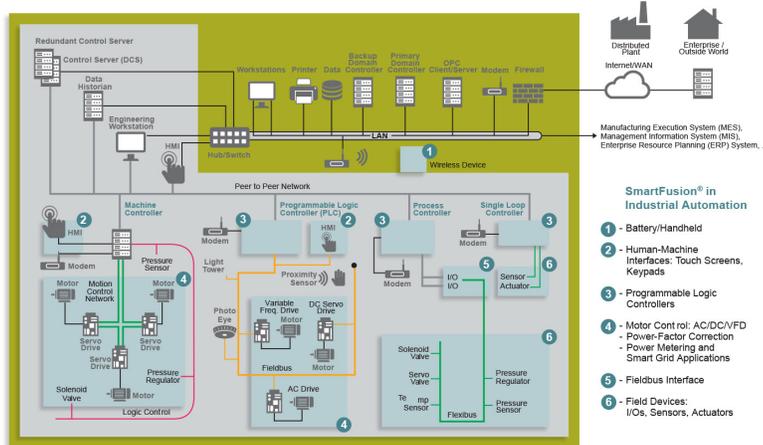
- Arm Cortex-M3 running Fieldbus protocol stack
- Ethernet MAC – standard protocols

### FPGA Fabric

- Multiple RS485 capable UARTs
- PROFIBUS, Modbus, WorldFIP, P-NET
- High speed Manchester encoding/decoding
- CAN

### Analog

- ADC for sensing
- DAC for excitation



Source: NIST

# General Purpose Solutions

## System Management

System management continues to gain importance in the design of all electronic systems, since smaller process geometries drive more multi-volt devices and are more susceptible to voltage and temperature fluctuations. System management tasks focus on maximizing system uptime, identifying and communicating alert conditions and logging data and alarm conditions. This can be combined with in-system diagnostics and prognostics, not only to help debug systems that have failed, but also to identify potential failures before they arise. Thus, using a SmartFusion device as a system manager provides the designer maximum implementation flexibility.

- Use the sample sequence engine in the ACE to manage system health data collection.
- Use the post-processing engine in the ACE to manage alert condition flag generation.
- Cortex-M3 only needs to make requests to the ACE and respond to interrupts; no processing cycles needed.
- Use FPGA gates for control algorithms when needed.
- Communicate through I<sup>2</sup>C, UART, SPI or Ethernet for updates and reporting.

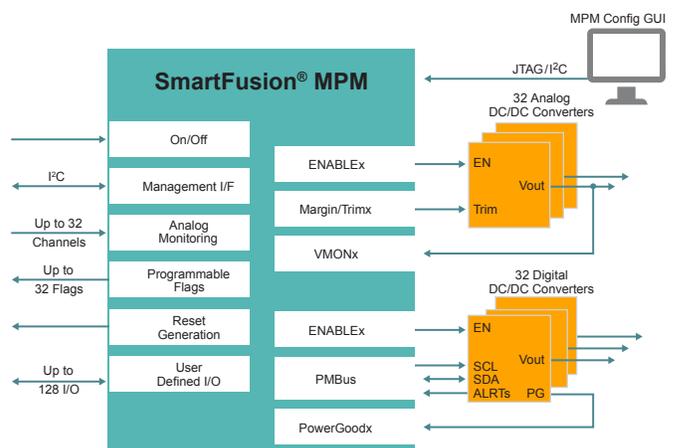
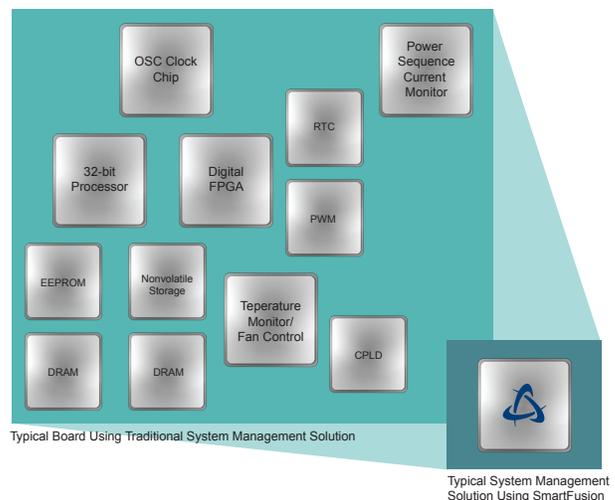
## Power Management

Microchip's system management solution significantly reduces the cost and complexity of board-level power management by integrating power converter functions including sequencing, trimming, margining, monitoring and control as well as system management functions like reset generation, event logging and "green" power algorithm support. Targeted to the SmartFusion SoC, there is an abundance of uncommitted analog and FPGA resources available to the user allowing the creation of a true custom solution.

Microchip's Mixed Signal Power Manager (MPM) reference design version 4.0 further distances itself from the competition by now including support for PMBus based POL converters. No other power management solution seamlessly supports a mix of analog and PMBus based power converters. Now you can sequence, monitor and manage a mixed set of DC/DC converters including LDOs, analog style and the highly efficient PMBus based converters from a single management device.

- Manage up to 64 DC/DC Converters
- Full support for analog and digital POL converters
- Sequence, monitor, margin, trim converters

Leveraging the considerable processing power of the ACE leaves the Cortex-M3 and FPGA gates available for running the actual application or communicating with the outside world. This not only eliminates the need for multiple ASSP devices to perform system management, but prevents system management from being an unnecessary burden on the Bill-of-Materials (BOM) cost. Selecting SmartFusion devices for system management provides flexibility and reliability at the lowest Total Cost of Ownership (TCO).

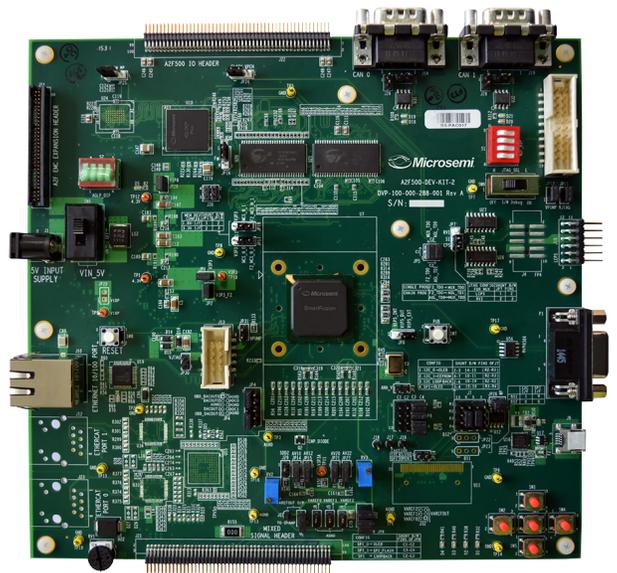


## Hardware Platform Management

nVent Schroff with their Pigeon Point products, a Microchip partner, helped refine the architecture of SmartFusion devices for hardware platform management. The following SmartFusion-based Board Management Reference (BMR) solutions for the ATCA and VPX board as well as AMC module controller are examples of offerings from nVent Schroff:

- BMR-A2F-ATCA: IPM Controllers (IPMCs) for ATCA boards
- BMR-A2F-AMC: Carrier IPMCs for ATCA AMC carrier boards
- BMR-A2F-AMCm: Module Management Controllers for AMC modules
- BMR-A2F-VPX: IPM Controllers (IPMCs) for VPX boards

nVent Schroff with its Pigeon Point products is the dominant supplier of hardware and firmware solutions for the mandatory hardware platform management controllers that are part of every Telecommunications Computing Architecture board or module and are optional for VITA46/VPX boards.



### Key Features of the Hardware Management Solutions

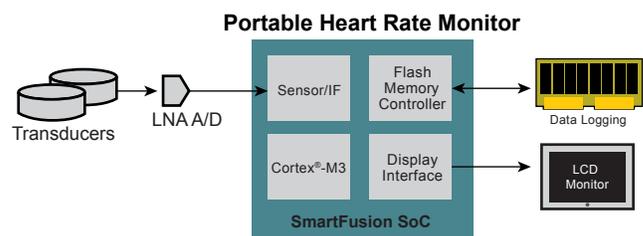
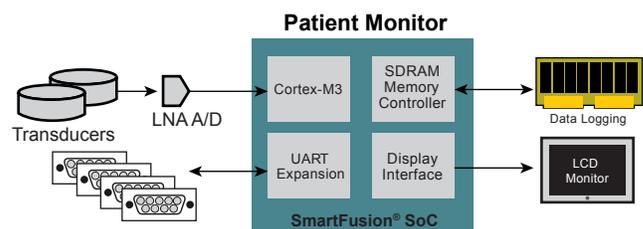
- Advanced Ethernet attachment via built-in Ethernet MAC, supporting serial port access and fast firmware upgrades over LAN
- Optimizations for xTCA/VPX management via the flash FPGA fabric, with the option to integrate additional board- and module-specific functionality
- Advanced analog monitoring using SmartFusion programmable analog
- Complete offloading from the Cortex-M3 of xTCA/VPX-aware analog threshold processing via ACE
- Integration of flexible power management functions eliminating the use of external power devices
- Benchtop implementations for familiarization and as a known good reference during bring-up of a new xTCA/VPX board or module

## Medical Systems

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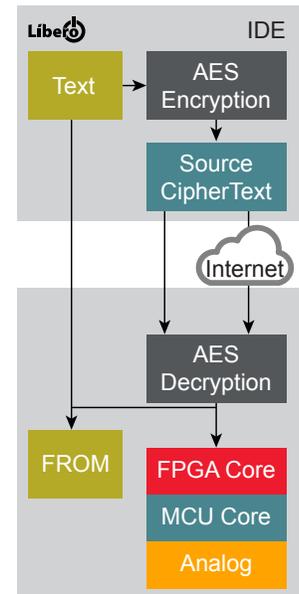
## Design and Data Security

Microchip's Flash SoCs and FPGAs have always been known for their design security and IP protection. SmartFusion devices bring an even higher level of security to embedded systems.

- Microcontroller and FPGA interface not exposed at board level
- No bitstream to transfer at boot-up
- FlashLock protects against tampering and reprogramming
- AES-encrypted in-system programming
- Protects against overbuilding with programmable device key

Microchip is the first major FPGA company to address the threats caused by side-channel analysis. Side-channel attacks such as Differential Power Analysis (DPA) can endanger the security of the design IP configured into a SoC or FPGA and the security of the end application itself.

Microchip has obtained a license from Cryptograph Research, Inc. (CRI) for the DPA patent portfolio, consisting of more than fifty patents. Contact Microchip sales to order devices that include a license to implement IP based on these patents.



## Intellectual Property for SmartFusion SoCs

SmartFusion devices are composed of hard Intellectual Property (IP) blocks, such as an Arm Cortex-M3 processor, UART, SPI, I<sup>2</sup>C and 10/100 Ethernet interface, as well as standard peripherals, such as ADC, DAC, timers, watchdog timer (WDT) and RTC. Beyond these hard cores you can select from Microchip's IP Catalog within SmartDesign to add additional free IP to the FPGA fabric of your SmartFusion device, or choose from a wide range of partner cores. Microchip has more than 180 intellectual property products designed and optimized to support communications, consumer, military, industrial, automotive and aerospace markets. Microchip IP solutions streamline your designs, enable faster time-to-market and minimize design costs and risk. The table below shows some examples of the IP available. A complete list of cores is available on the Microchip SoC Products Group website: <https://www.microsemi.com/product-directory/design-resources/5092-ip-cores>

General Purpose		Cryptography	Communication	MIL-STD-1553B	DSP IP Core
Core 16550	CoreUART	CoreAES128	CorePCIF	Core1553BRM	CoreFFT
CoreGPIO	CoreI2C	CoreDES	CoreSDR/DDR	Core1553BRT	CoreFIR
CoreTimer	CoreSPI	Core3DES	Core429	Core1553BRT-EBR	CoreDDS
CoreSDR	CorePWM	Fast SHA-256 Hash1	IniCAN2	Core1553BBC	

1. For more information, see the Helion Technology partner page: [www.microsemi.com/soc/products/partners/companioncore/helion.aspx](http://www.microsemi.com/soc/products/partners/companioncore/helion.aspx).
2. For more information, see the Inicore partner page: [www.microsemi.com/soc/products/partners/companioncore/inicore.aspx](http://www.microsemi.com/soc/products/partners/companioncore/inicore.aspx).

Microchip IP cores can be accessed through Libero SoC via the SmartDesign IP catalog. Drivers for the processor supported IP cores are available through the Firmware Catalog and are extracted automatically for SmartFusion designs through the MSS Configurator dialog.

For more details on the Microchip IP Core offerings, please refer IP DirectCores webpage: <https://www.microsemi.com/products/fpga-soc/design-resources/ip-cores/direct-cores>



# SmartFusion Family Product Table

SmartFusion® Devices		A2F200	A2F500
FPGA Fabric	System Gates	200,000	500,000
	Tiles (D-flip-flops)	4,608	11,520
	RAM Blocks (4,608 bits)	8	24
Microcontroller Subsystem (MSS)	Flash (Kbytes)	256	512
	SRAM (Kbytes)	64	64
	Cortex®-M3 with Memory Protection Unit (MPU)	Yes	Yes
	10/100 Ethernet MAC	Yes	Yes
	External Memory Controller (EMC)	26-bit address, 16-bit data	26-bit address, 16-bit data <sup>1</sup>
	DMA	8 Ch	8 Ch
	I <sup>2</sup> C	2	2
	SPI	2	2
	16550 UART	2	2
	32-bit Timer	2	2
	PLL	1	22
	32 KHz Low Power Oscillator	1	1
	100 MHz On-Chip RC Oscillator	1	1
	Main Oscillator (32 KHz to 20 MHz)	1	1
	Programmable Analog	ADCs (8-/10-/12-bit SAR)	2
DACs (12-bit sigma-delta)		2	34
Signal Conditioning Blocks (SCBs)		4	54
Comparators <sup>3</sup>		8	104
Current Monitors <sup>3</sup>		4	54
Temperature Monitors <sup>3</sup>		4	54
Bipolar High Voltage Monitors <sup>3</sup>		8	104

1. Not available on A2F500 for the PQ208 package. 2. Two PLLs are available in CS288 and FG484 (one PLL in FG256 and PQ208). 3. These functions share I/O pins and may not all be available at the same time. 4. Available on FG484 only. PQ208, FG256, and CS288 packages offer the same programmable analog capabilities as A2F200.

## Package I/Os: MSS + FPGA I/Os

Device	A2F200				A2F500			
	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Direct Analog Input	8	8	8	8	8	8	8	12
Shared Analog Input <sup>1</sup>	16	16	16	16	16	16	16	20
Total Analog Input	24	24	24	24	24	24	24	32
Total Analog output	1	2	2	2	1	2	2	3
MSS I/Os <sup>2,3</sup>	22	31	25	41	22	31	25	41
FPGA I/Os	66	78	66	94	66 <sup>4</sup>	78	66	128
Total I/Os	113	135	117	161	113	135	117	204
Temperature Grade <sup>5</sup>	C, I	C, I	C, I	C, I	C, I	C, I	C, I, M	C, I, M

1. These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors. 2. 16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for the MSS. These I/Os support Schmitt triggers and support only LVTTTL and LVCMOS (1.5/1.8/2.5, 3.3V) standards. 3. 9 MSS I/Os are primarily for 10/00 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTTL and LVCMOS (1.5/1.8/2.5, 3.3V) standards. 4. EMC is not available on the A2F500 PQ208 package. 5. Military temperature grade (-55°C to +125°C) devices are offered in some density and package combinations as noted.

## Support

Microchip is committed to supporting its customers in developing products faster and more efficiently. We maintain a worldwide network of field applications engineers and technical support ready to provide product and system assistance. For more information, please visit [www.microchip.com](http://www.microchip.com):

- Technical Support: [www.microchip.com/support](http://www.microchip.com/support)
- Evaluation samples of any Microchip device: [www.microchip.com/sample](http://www.microchip.com/sample)
- Knowledge base and peer help: [www.microchip.com/forums](http://www.microchip.com/forums)
- Sales and Global Distribution: [www.microchip.com/sales](http://www.microchip.com/sales)

## Training

If additional training interests you, Microchip offers several resources including in-depth technical training and reference material, self-paced tutorials and significant online resources.

- Overview of Technical Training Resources: [www.microchip.com/training](http://www.microchip.com/training)
- MASTERS Conferences: [www.microchip.com/masters](http://www.microchip.com/masters)
- Developer Help Website: [www.microchip.com/developerhelp](http://www.microchip.com/developerhelp)
- Technical Training Centers: [www.microchip.com/seminars](http://www.microchip.com/seminars)

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**China - Shenyang**  
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**China - Suzhou**  
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**China - Xiamen**  
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**India - Pune**  
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